

# Stackup Planning, Part 6: Impedance Variables

## Beyond Design

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Interconnect impedance is a trade-off between the variables, including trace width, trace (copper) thickness, dielectric thickness, and dielectric constant. If you need to include differential impedance, trace clearance also comes into play. For minimum crosstalk, the coupling must also be considered. Plus, one needs to bear in mind the exact materials that are stocked by your preferred PCB fabricator. Determining the correct configuration to achieve the desired impedance is not as simple as clicking an impedance goal-seeking button. But rather, one should weigh up all the pros and cons of changing each variable and make an informed decision.

Impedance is the key factor that controls the stability of a design; it is the core issue of the signal integrity methodology. The substrate is the most important component of the assem-

bly and needs to be planned correctly to maintain consistent impedance across layers, avoid unintentional signal coupling, and reduce electromagnetic emissions. In this month's column, I continue with Part 6 of my stackup planning series and look at the correct process of stackup impedance planning and the consequences of bad decisions.

Goal seeking is a function that is used to find an unknown value from a set of known values. If you know the answer, then the algorithm will fix all but one variable and hone in on the desired result. But keep in mind that there is no AI involved here. The software does not take all the possible variables into account as the designer would.

PCB fabricators know their production process extremely well, and their manufacturing

expertise is invaluable to produce a high-performance substrate. However, they are not signal integrity gurus; most know very little about high-speed digital design. Why leave critical impedance selection decisions to them when the product designer has far more knowledge about the requirements of controlled impedance? The people who do not understand impedance control like goal-seeking because they can push a button and get a quick answer, albeit the wrong configuration in most cases.

Let's take a look at the impedance variables and how they interact.

## 1. Trace Width

There are three main considerations for trace width selection:

- Minimum manufacturable width, which is generally 4 mils. 3 mils can be achieved, but yields drop, and costs increase.
- Minimum spacing between BGA balls; in most cases, 4 mils will get you through.
- Current handling, which is not an issue for digital design. For power distribution, the trace may need to be thick to accommodate the required current.

Trace width increases as impedance decreases (Figure 1). Start with the highest impedance technology first, which is typically 50-ohm single-ended, 100-ohm differential set at 4 mils.

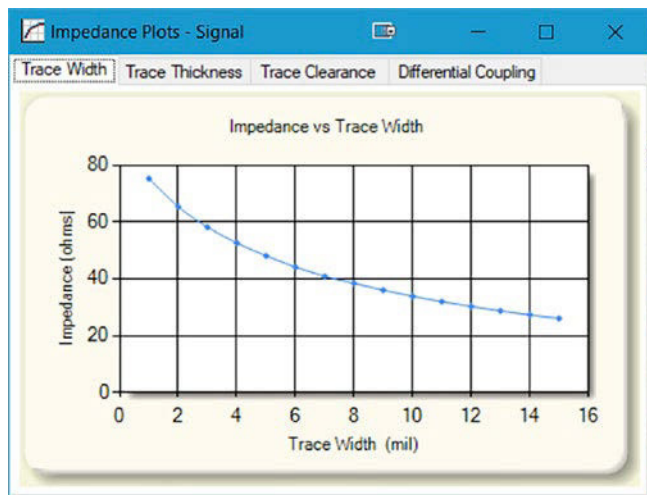


Figure 1: Impedance vs. trace width (iCD Stackup Planner).

## 2. Trace (Copper) Thickness

The main considerations for trace copper thickness selection (Figure 2) include:

- Copper on either side of a core material must be the same thickness.
- Copper plating (typically 1 mil) is added to outer microstrip copper foil hence traces due to the through-hole barrel plating.
- Current handling capability at low frequencies. High-frequency current flows in the outer skin of the copper.

Typical values are 1 oz (1.4 mils) and ½ oz (0.7 mils). 1.4 mil is a good first choice unless you have a high layer count stackup.

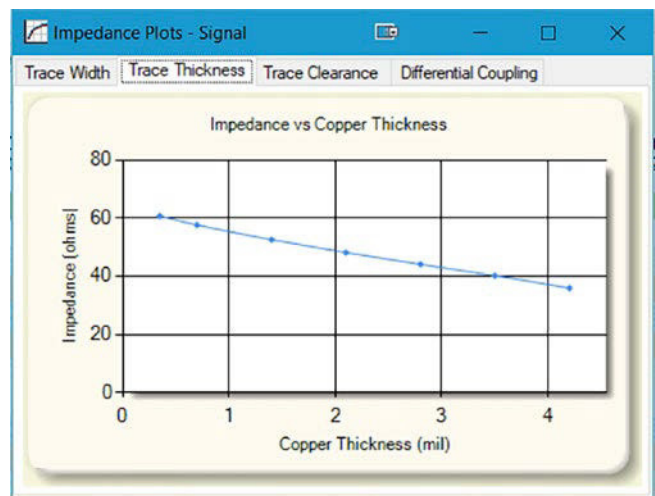


Figure 2: Impedance vs. copper thickness.

## 3. Trace Clearance (Separation)

Trace clearance determines the differential impedance:

- Differential signals that are closely coupled will operate mainly in the differential mode with some common-mode radiation from imbalances in the signals.
- If the two traces are separated enough to prevent coupling then both act as single-ended signals. A 100-ohm differential pair becomes two individual 50-ohm single-ended signals.

Begin with 4-mil clearance and expand this out to where the impedance levels off (10–12

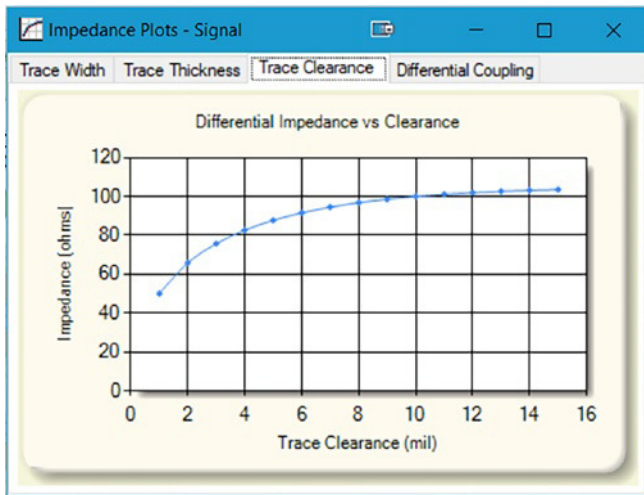


Figure 3: Impedance vs. trace clearance.

mils in Figure 3) if necessary. Close coupling will provide the most routing space.

#### 4. Trace Coupling

Although trace coupling is not strictly speaking an impedance variable, it should be considered during the planning stage. The combination of trace clearance and dielectric thickness provides the point of coupling (12 mils, in the case of Figure 4). At this point, differential pairs are no longer coupled, and individual parallel traces become vulnerable to crosstalk. Use the point of coupling to define the crosstalk trace clearance constraints.

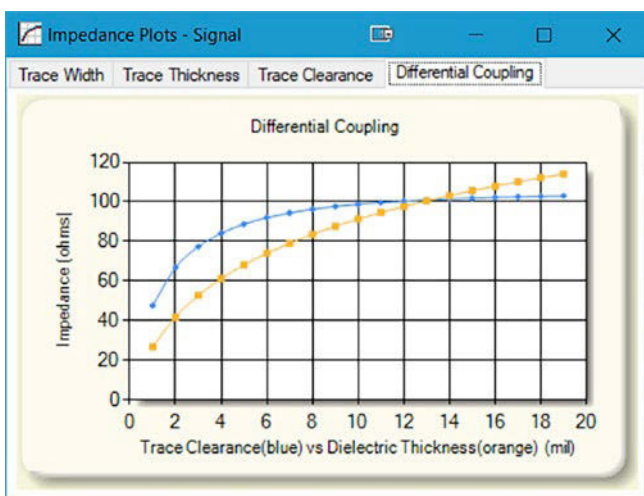


Figure 4: Impedance vs. coupling.

#### 5. Dielectric Thickness

The main considerations for dielectric thickness (Figure 5) include:

- All signal layers should be adjacent to and closely coupled to an uninterrupted reference plane. This provides the shortest loop area and the lowest inductance for the return current path.
- The minimum dielectric thickness is determined by the selected material glass style.
- A wider weave fiberglass may cause skew in differential pairs at high frequency (> 10 GHz), converting differential mode current to common mode—hence radiation.

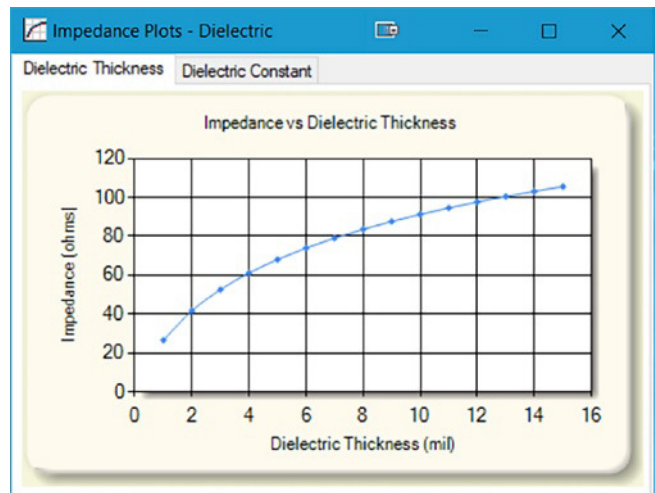


Figure 5: Impedance vs. dielectric thickness.

Glass weave skew and pile unevenness can be prevented by using two plies of 1067 glass prepreg combined. Do not use 106 or other wide gap glass styles. 1067 glass is typically 2.5–3 mils.

With regard to stripline (inner layers), the thinnest dielectric should be closest to the GND plane return path. In a dual stripline configuration, the dielectrics closest to the planes should be thin, and the dielectric between the signal traces should be thickest, which also reduces broadside crosstalk.

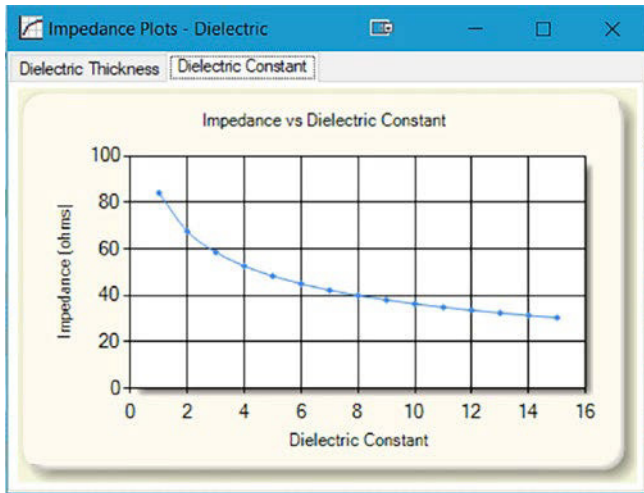


Figure 6: Impedance vs. dielectric constant.

## 6. Dielectric Constant

The main considerations for dielectric constant, or Dk, (Figure 6) include:

- A dielectric constant of 4.3 is typical.
- Low loss materials tend to have lower dielectric constants ( $\sim 3$ ).
- Microstrip (outer layer) dielectric should have lower Dk to slow the velocity of propagation of the EM wave to match the stripline speed.

d. A high dielectric constant creates the most planar capacitance, which is used to lower the impedance of the power distribution network. This is good for plane-to-plane coupling.

Start with a value of 4, but if the frequency is 10 GHz or more, use 3 as a starter.

Taking all of the above into account, one should first plan the stackup using virtual materials (Figure 7) to get in the ballpark. In other words, pick an appropriate value, and then hone in on these values with the actual materials stocked.

In this case, I am designing the stackup for three different technologies (50/100-ohm digital, 40/80-ohm DDR3, and 90-ohm USB). The dielectric constant and thickness, together with the trace width and clearance, need to provide near correct impedances for these three technologies (Table 1).

A characteristic impedance of 40–60 ohms is typically used for a digital design. However, this value becomes more critical as the edge rates become faster. Also, different technologies have their specific impedance requirements. For example, Ethernet is 100 ohms and USB 90 ohms differential, and DDR2 memory is

Layer No.	Via	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)
		Soldermask		Dielectric	3.3	0.5							
1	8	Signal	Top	Conductive			2.2	12	4	0.43	52.65	100.34	
		Prepreg		Dielectric	4.0	3							
2		Plane	GND	Conductive			1.4						
		Core		Dielectric	4.0	2							
3		Plane	VDD	Conductive			1.4						
		Prepreg		Dielectric	4.0	8							
4		Signal	Inner 4	Conductive			1.4	12	4	0.31	53.07	102.53	
		Core		Dielectric	4.0	6							
5		Plane	GND	Conductive			1.4						
		Prepreg		Dielectric	4.0	4							
6		Signal	Inner 6	Conductive			0.7	12	4	0.19	51.59	99.95	93.52
		Core		Dielectric	4.0	12							
7		Signal	Inner 7	Conductive			0.7	12	4	0.19	51.59	99.95	93.52
		Prepreg		Dielectric	4.0	4							
8		Plane	VCC	Conductive			2.2						

Figure 7: Virtual materials for microstrip, stripline, and dual stripline configurations (iCD Stackup Planner).

Target Impedance	Tol +/-%	Layer No.	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)
50/100 ohms	10	1	12	4	0.43	52.65	100.34	
50/100 ohms	10	4	12	4	0.31	53.07	102.53	
50/100 ohms	10	6	12	4	0.19	51.59	99.95	93.52
50/100 ohms	10	7	12	4	0.19	51.59	99.95	93.52
40/80 ohms	10	1	12	6.5	0.62	41.61	79.47	
40/80 ohms	10	4	8	6.5	0.44	42.9	79.88	
40/80 ohms	10	6	15	6.5	0.27	40.6	79.9	72.23
40/80 ohms	10	7	15	6.5	0.27	40.6	79.9	72.23
90 ohms	10	1	6	4	0.43	52.65	91.96	
90 ohms	10	4	6	4	0.31	52.81	91.58	
90 ohms	10	6	6	4	0.19	51.46	92.55	93.4
90 ohms	10	7	6	4	0.19	51.46	92.55	93.4

Table 1: The three different technologies using virtual materials.

50/100, while DDR3/4 is 40/80 single-ended/differential impedance. Controlling impedance simultaneously on each signal layer with a number of different technologies can become a challenge.

Unfortunately, your preferred PCB fabricator will not stock these values, so the next step is to convert the virtual materials to actual materials that are available (in the partial stackup of Figure 8). This will also give you the actual materials for the three different technologies (Table 2). This is the step that most, if not all, designers avoid, leaving it to the fab shop CAM engineer.

To do this, we first need to determine an operating frequency that the product needs to perform. Generally, we need to consider the bandwidth up to the fifth harmonic of the fundamental. If we have a clock running at 800 MHz, then 4-GHz material would be appropriate. I have chosen the ITEQ IT-180A, 5-GHz material, which is readily available from Asian fabricators and is suitable for low-cost, high-speed applications. The iCD Materials Planner can be used to narrow down the selection from the fabricator's stock.

The configuration of the PCB stackup depends on many factors. But whatever the

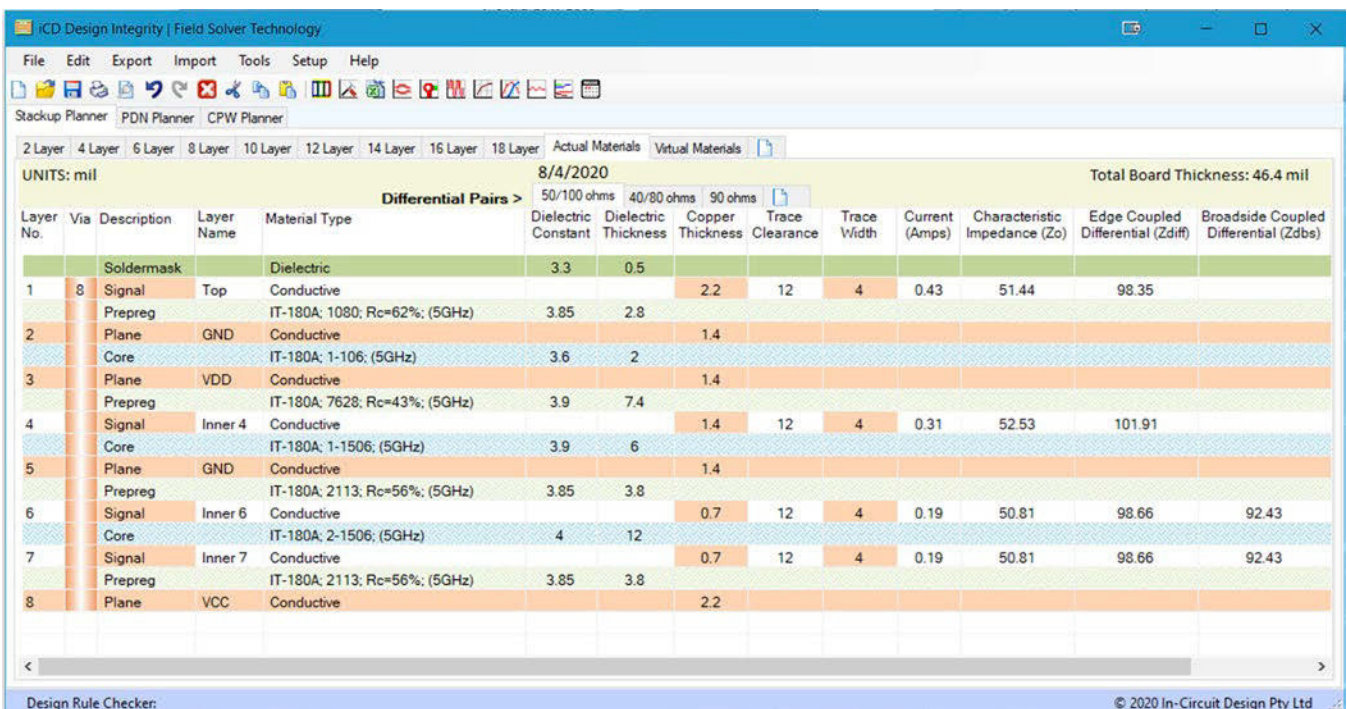


Figure 8: The actual materials using ITEQ, IT-180A (iCD Stackup Planner).

Target Impedance	Tol +/-%	Layer No.	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)
50/100 ohms	10	1	12	4	0.43	51.44	98.35	
50/100 ohms	10	4	12	4	0.31	52.53	101.91	
50/100 ohms	10	6	12	4	0.19	50.81	98.66	92.43
50/100 ohms	10	7	12	4	0.19	50.81	98.66	92.43
40/80 ohms	10	1	12	6.5	0.62	40.46	77.52	
40/80 ohms	10	4	8	6.5	0.44	42.3	79.29	
40/80 ohms	10	6	15	6.5	0.27	39.82	78.46	71.11
40/80 ohms	10	7	15	6.5	0.27	39.82	78.46	71.11
90 ohms	10	1	6	4	0.43	51.44	90.6	
90 ohms	10	4	6	4	0.31	52.29	91.58	
90 ohms	10	6	6	4	0.19	50.68	91.73	92.32
90 ohms	10	7	6	4	0.19	50.68	91.73	92.32

Table 2: The actual materials for the three different technologies.

requirements, one should ensure that the following rules are followed to avoid a possible debacle:

- All signal layers should be adjacent to and closely coupled to an uninterrupted reference plane, creating a clear return path and eliminating broadside crosstalk.
- There is good planar capacitance to reduce AC impedance at high frequencies.
- High-speed signals should be routed between the planes to reduce radiation.
- The substrate should be symmetrical with an even number of layers, which prevents the PCB from warping during fabrication and reflow.
- The stackup should accommodate a number of different technologies.
- Cost—the most important design parameter—should also be addressed.

Take charge of the impedance selection process and learn to control the variables rather than just handing the decisions over to the fab shop. This should be done very early in the design process to eliminate the need for change at a later stage, which could require the rerouting of critical nets and result in delays in the development schedule.

## Key Points

- Impedance is the key factor that controls the stability of a design.
- The substrate is the most important component of the assembly and needs to be

planned correctly to maintain consistent impedance across layers, avoid unintentional signal coupling, and reduce electromagnetic emissions.

- PCB fabricators know their production process extremely well, and their manufacturing expertise is invaluable to produce a high-performance substrate.
- Trace width increases as impedance decreases, so start with the highest impedance technology first.
- 1.4 mil is a good first choice for copper thickness unless you have a high layer count stackup.
- Differential signals that are closely coupled will operate mainly in the differential mode with some common-mode radiation from imbalances in the signals.
- If the two traces are separated enough to prevent coupling, then both act as single-ended signals. A 100-ohm differential pair becomes two individual 50-ohm single-ended signals.
- The combination of trace clearance and dielectric thickness provides the point of coupling. Use the point of coupling to define the crosstalk trace clearance constraints.
- All signal layers should be adjacent to and closely coupled to an uninterrupted reference plane. This provides the shortest loop area and the lowest inductance for the return current path.
- Glass weave skew and pile unevenness can be prevented by using two plies of 1067 glass prepreg combined.

- Low loss materials tend to have lower dielectric constants ( $\sim 3$ ).
- A high dielectric constant creates the most planar capacitance, which is used to lower the impedance of the power distribution network.
- First, plan the stackup using virtual materials, and then convert the virtual materials to actual materials that are stocked by your preferred fab shop.
- Consider the bandwidth up to the fifth harmonic of the fundamental. **DESIGN007**

### Further Reading

- B. Olney, "Beyond Design: The Key to Product Reliability," *Design007 Magazine*, June 2019.
- B. Olney, "Beyond Design: The 10 Fundamental Rules of High-Speed PCB Design, Part 2," *Design007 Magazine*, October 2018.
- B. Olney, "Beyond Design: Common Symptoms of Common-Mode Radiation," *Design007 Magazine*, May 2018.

- B. Olney, "Beyond Design: Controlled Impedance Design," *The PCB Design Magazine*, May 2015.
- B. Olney, "Beyond Design: Signal Integrity, Part 3," *The PCB Design Magazine*, December 2014.
- B. Olney, "Beyond Design: Signal Integrity, Part 1," *The PCB Design Magazine*, October 2014.
- B. Olney, "Beyond Design: Stackup Planning, Part 3," *The PCB Design Magazine*, August 2014.
- B. Olney, "Beyond Design: Practical Signal Integrity," *The PCB Design Magazine*, August 2013.



**Barry Olney** is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded at [icd.com.au](http://icd.com.au). To read past columns or contact Olney, [click here](#).

## Pattern Blazer World's Brightest LED Pattern Projector in 3D Vision Applications

Innovations in Optics, Inc. introduces the Pattern Blazer, a high-power, LED fixed-pattern projector for structured lighting and stereovision in 3D machine vision. Pattern Blazer applications include determination of object shape and orientation, contour mapping of parts, surface defect detection, depth measurements, guidelines, edge detection, and alignment. A near infrared version is suited for video identification in long-range CCTV security and surveillance.

The Pattern Blazer projects patterns with an intensity that is at least 5X to 10X greater at the same distance than other "high power" LED Pattern projectors for similar pattern size and wavelength. It can be operated in either continuous, PWM or pulsed current modes. Extremely bright patterns at long working distances enables the use

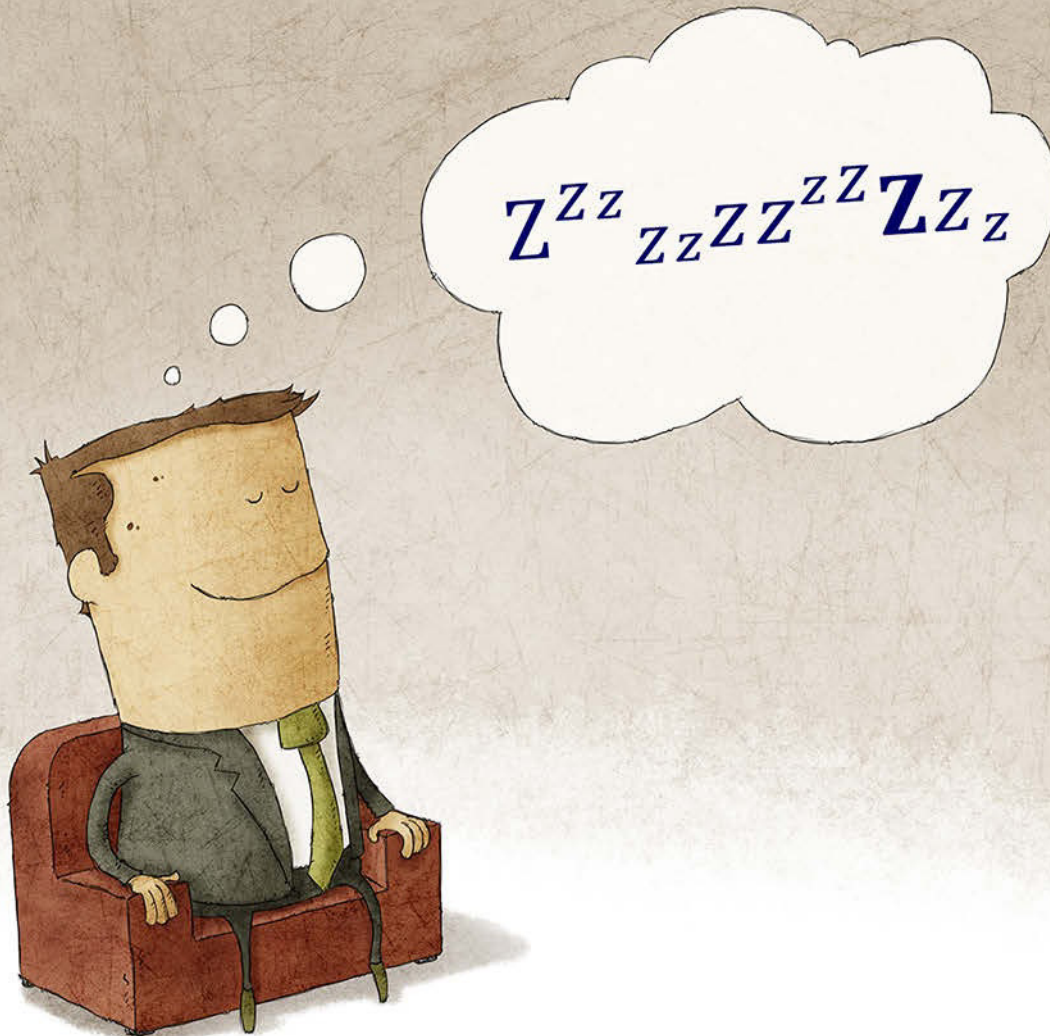
of 3D imaging in vast, well-lit areas including outdoor locations.

The Pattern Blazer features four standard LED spectral options, blue (480 nm), red (660 nm) near-infrared (860 nm), and broadband white (4800K). It uses standard C-mount machine vision lenses designed for 1" image sensors. The Pattern Blazer incorporates pinhole-free precision reticles patterned by photolithography to produce thinner lines, sharper edges, and more homogeneous illumination than lasers and without diffraction or speckle effects. Projected patterns for the Pattern Blazer include lines, grids, edges, and random dot point clouds. Other wavelength LEDs and custom patterns can be provided upon request.

(Source: Innovations in Optics Inc.)



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