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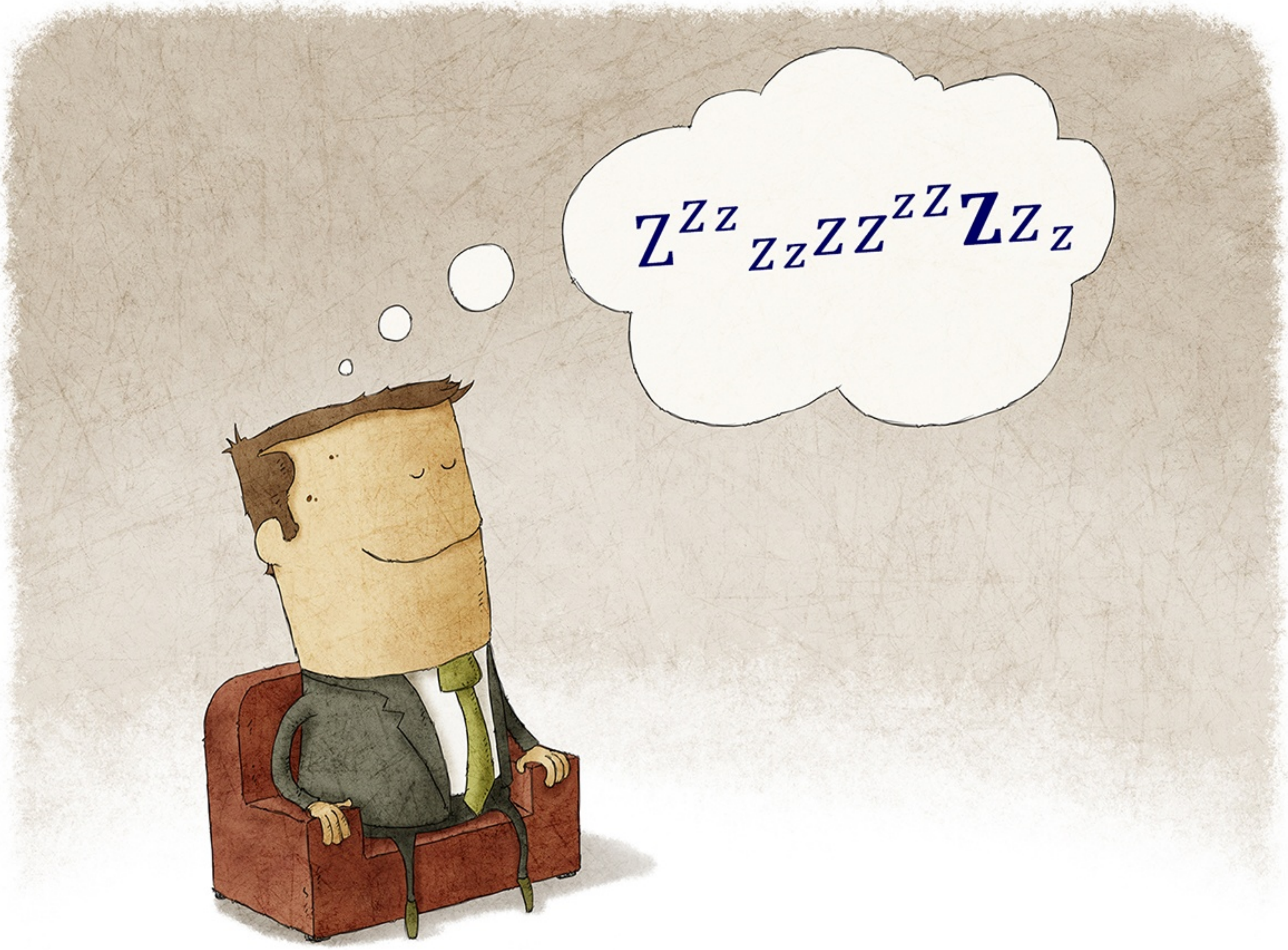

Did you know that two seemingly unrelated concepts are the foundation of a product's performance and reliability?

- Transmission line impedance and
- Power Distribution Network impedance

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Crosstalk Margins

Beyond Design

by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

What is an acceptable level of crosstalk? That depends on the technology being used, and this level has changed quite dramatically over the years, going from TTL logic devices to today's high-speed Gbps devices. The amount of power a CPU uses, and thus the amount of heat it dissipates, is the product of the voltage and the current it draws. The trend is towards lower core voltages, which conserves power. But, reducing the core voltage also reduces the noise margin. In this month's column, I will delve into the threshold of acceptable crosstalk and how to mitigate its impact on high-speed designs.

Crosstalk is caused by the coupling of the electromagnetic fields. Electric fields cause signal voltages to capacitively couple into nearby traces. Capacitive coupling draws a surge of drive current, which causes reflections on the transmission lines. Whereas, magnetic fields cause signal currents to be induced into nearby traces. Inductive coupling produces ground bounce and power supply noise. Crosstalk falls off rapidly with the square of the distance and the degree of impact is related to the aggressor signal voltage, available board real estate and thus the proximity of signal traces. Crosstalk can appear as either far-end, forward crosstalk (FEXT) or near-end, reverse crosstalk (NEXT).

Fortunately, synchronous buses, as typically used for parallel data signal transfer, benefit from an extraordinary immunity to crosstalk. Crosstalk only occurs when the signals are being switched and this crosstalk only has an impact within a small window around the moment of the clocking. The crosstalk must be specified during the setup (t_S) and hold (t_H) window at the receiver. During this interval, the crosstalk must never drive any valid signal across the receive threshold to the opposite logic state. So, providing the receiver waits sufficiently long enough for the crosstalk to settle, before sampling the bus, the crosstalk has no impact on the signal quality at the receiver. If the crosstalk arrives during the signal transitions (Figure 1), then its only impact is jitter

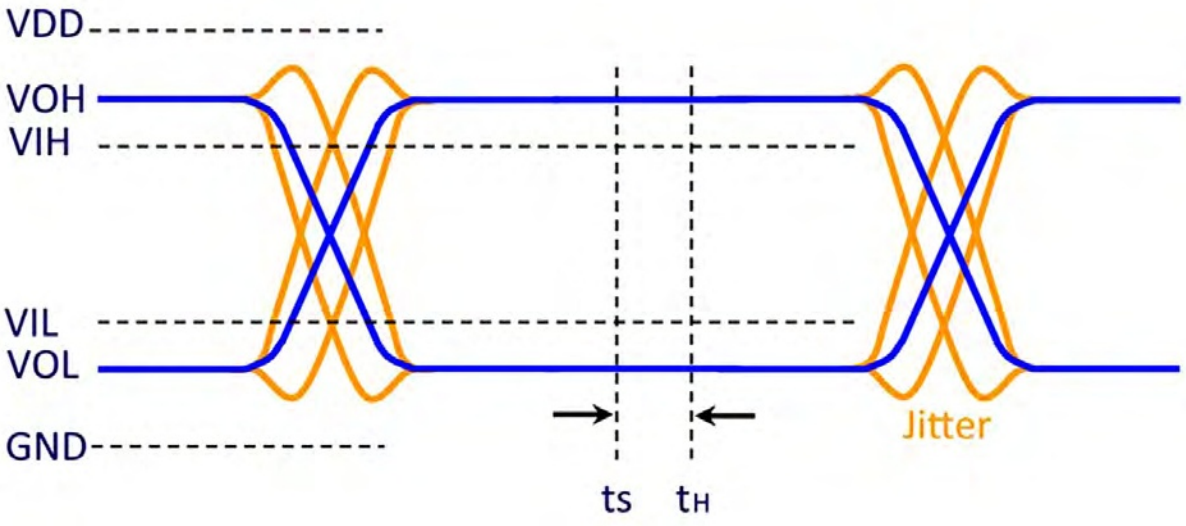


Figure 1: Crosstalk during the signal transitions only results in jitter of the eye.

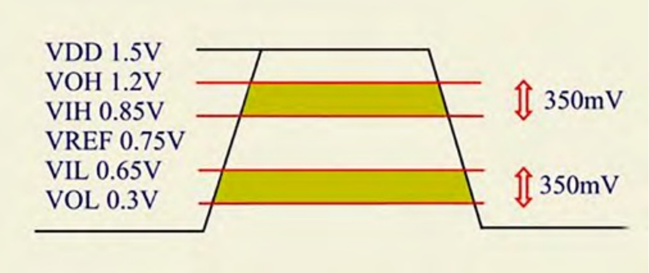


Figure 2: Noise margin for DDR3 memory.

on the eye. However, this only applies to signals within the same group. Asynchronous and unrelated signals, on the other hand, remain sensitive to crosstalk at all times.

Unfortunately, due to the ever-increasing speed of digital signals, one may not have the luxury of waiting so long to sample the bus. And as the supply voltage drops from say 3.3V to 1.5V, then the allowable noise margin more than halves making the circuit designer's decisions regarding crosstalk even more crucial. Crosstalk creates noise that erodes the noise margin. This noise may not be so great that it alone will cause a bit failure, but it can be enough to push the total noise over the edge.

For DDR3 memory devices for instance, the following values are taken from the JEDEC Specification JESD79-3E:

The maximum crosstalk value is the difference between the expected voltage at the receiver and the receiver threshold. In this case the maximum crosstalk is 350mV. This is for single-ended signals. Differential technologies do not have the noise margin concerns of single-ended technologies. This is due to common mode rejection, which is the ability of the receiver to reject noise that appears coincident on both inputs. Although differential technologies are much better at rejecting input noise, they are not totally immune. Excessive noise is still an issue and can cause serious problems.

Also, the crosstalk depends on the load which may vary considerably when driving banks of memory modules. Keep in mind that the total crosstalk on each victim trace is the total crosstalk from each of several nearby aggressors, all of which sum to produce the maximum value.

Figure 3 shows the near-end and far-end crosstalk for the victim traces adjacent to the aggressor trace (1.5V @ 1GHz). In this case

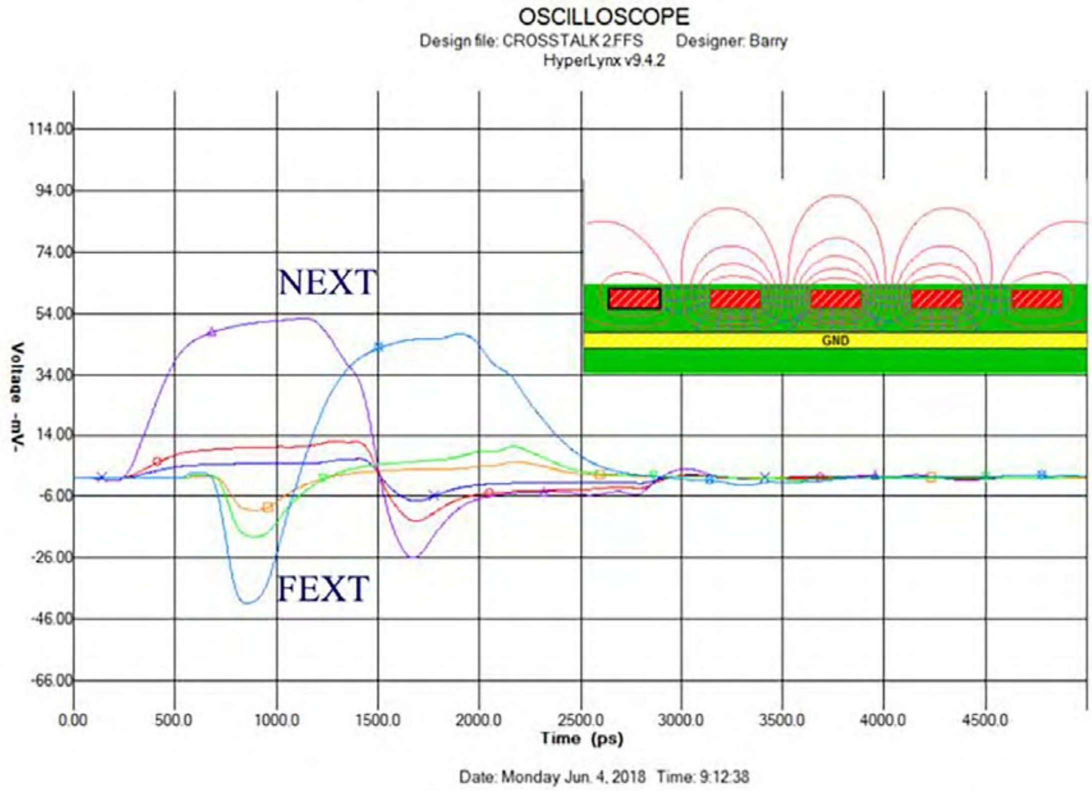


Figure 3: Near-end and far-end crosstalk for microstrip with 4/4 mil trace width/clearance.

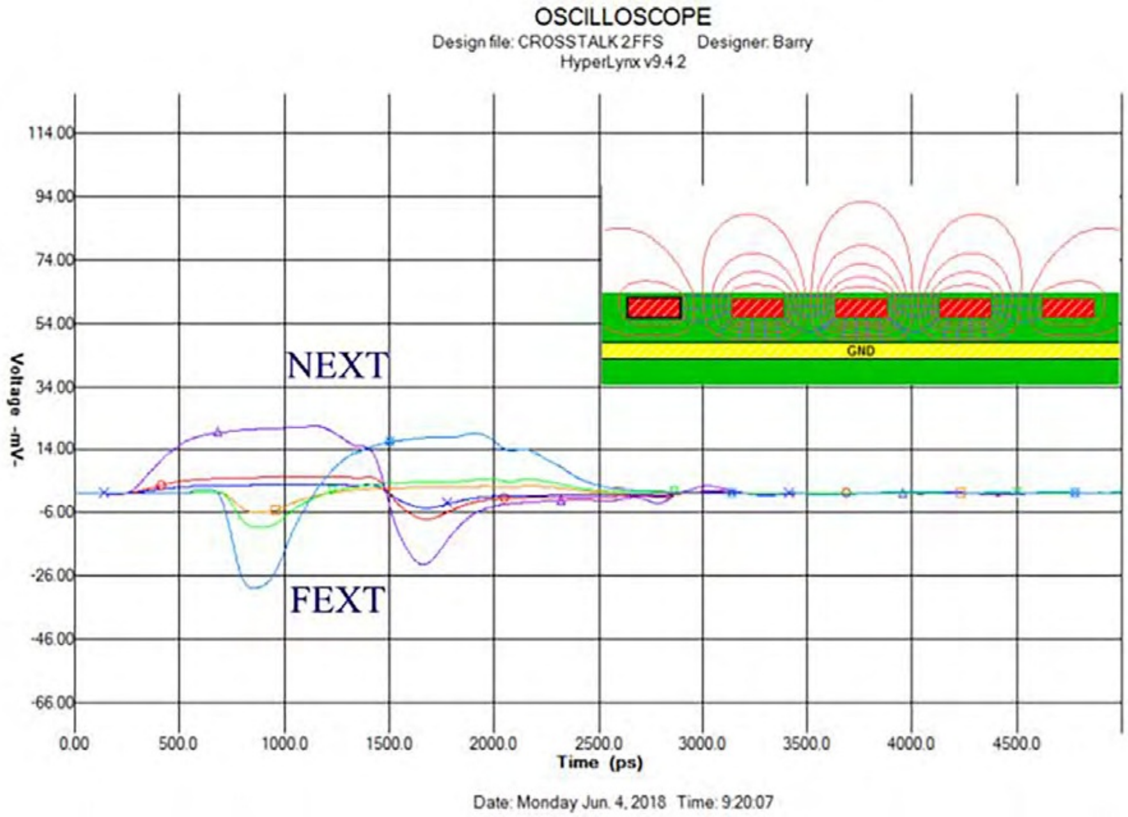


Figure 4: Near-end and far-end crosstalk for microstrip with 4/8 mil trace width/clearance.

the traces are 4 mil wide, 40 ohms impedance with a 4mil spacing. But, as the victim trace gets farther away from the aggressor the crosstalk decreases.

Figure 4 shows the near and far end crosstalk for 4 mil wide, 40 ohms impedance traces with 8 mil spacing. The further the separation the less the crosstalk. But, as previously mentioned, the total crosstalk on a victim trace is the accumulated noise injected from all nearby noise sources, so the result may be much more.

In a microstrip configuration, the mutual capacitive coupling, between adjacent traces, is generally weaker than the mutually inductive coupling, driving the FEXT co-efficient negative as can be seen in the previous simulations. However, forward crosstalk does not exist in the stripline configuration. The fine balance between inductive and capacitive coupled crosstalk produces almost no observable forward crosstalk.

Since the previous examples were of outer layer microstrip configurations, let's look at inner layer stripline crosstalk. Figure 5 shows the near-end crosstalk of a stripline construction for 4 mil wide, 40 ohms impedance traces with a 4 mil spacing. Notice how there is no FEXT component of the noise. Also, the peak to peak amplitude of the crosstalk has been considerably reduced. So all other factors being equal, here is just another good reason why one should always route high-speed signals on the inner layers of a multilayer PCB.

One factor that may have been overlooked in this methodology is the effect on the signal of the transition from layer 1 to 3. At that point on the board, any power supply noise existing between the planes enters the memory bus circuit traces. This may be a major source of crosstalk, depending on the effectiveness of the power distribution network (PDN) decoupling. Excessive PDN noise at the jump location could completely swamp out the differences in crosstalk due to trace layout. This also presents another good reason why PDN analysis and optimization is so important.

To evaluate crosstalk, I typically run a preliminary batch mode simulation in Mentor

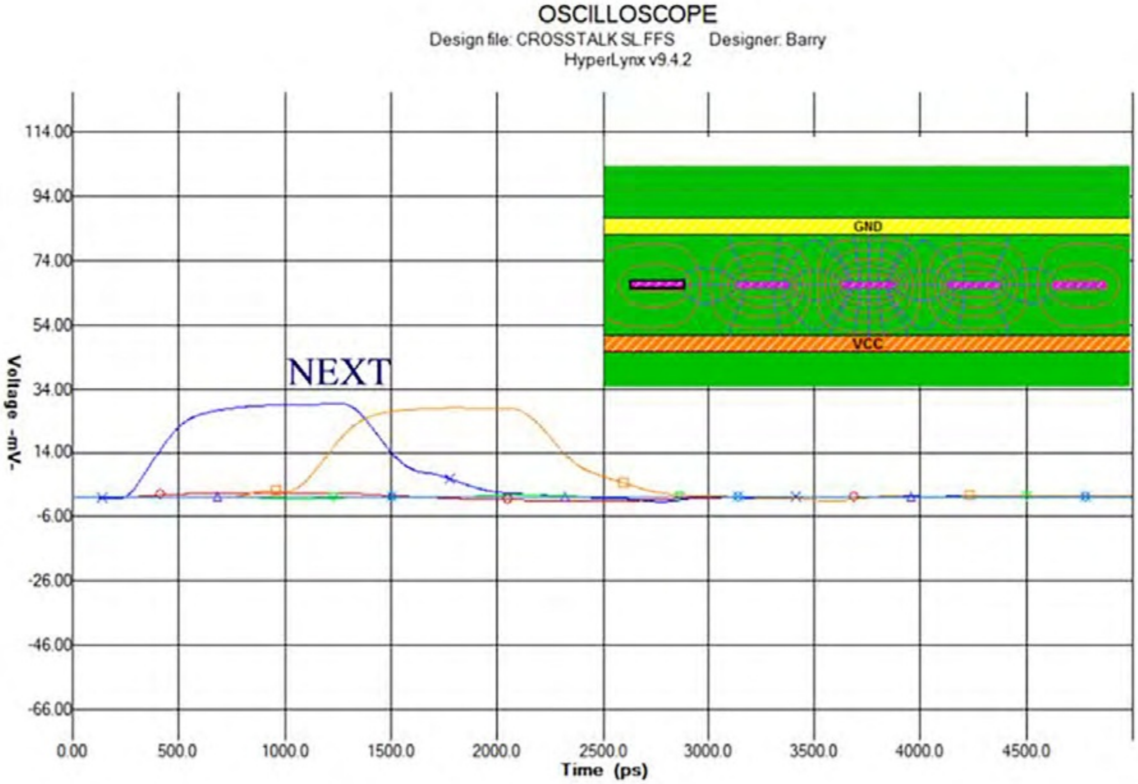


Figure 5: Crosstalk for stripline with 4/4 mil trace width/clearance.

Graphics HyperLynx. Default IC characteristics, crosstalk of 150mV maximum and EMC to FCC Class B are setup in the simulator. The batch mode simulation automatically scans large numbers of nets on the entire PCB, flagging signal integrity, crosstalk and EMC hot spots. Reported crosstalk violations can be evaluated by further interactive simulation if required. Setting the simulator to 150mV maximum crosstalk, on all signals, may seem excessively low, considering the above, but it makes sure we pick up any coupling that may be detrimental to signal integrity when accumulated. I also apply this constraint to synchronous buses to identify the impact of the total crosstalk from all aggressors. It is much easier, and cost effective, to eliminate the source of the noise than to fix the problem further down the product development process.

Both forward and reverse crosstalk can be arbitrarily reduced by separating the aggressors from the victim traces or by reducing the height of the dielectric above/below the planes. The latter also requires a reduction in trace width to maintain the impedance. Keep in mind that the fab costs generally increase below 4 mil trace width. So if real estate is a premium, as it generally is on dense, high-speed designs then reducing the dielectric height may be a good solution. We cannot completely eliminate crosstalk but as PCB designers, it is our job to ascertain how to control, manage and live with the consequences of our decisions.

Key Points:

- Reducing core voltage also reduces the noise margin.
- Crosstalk is caused by the coupling of the electromagnetic fields.
- Crosstalk falls off rapidly with the square of the distance and the degree of impact is related to the aggressor signal voltage and proximity.
- Synchronous buses benefit from an extraordinary immunity to crosstalk. It only has an impact within a small window around the moment of the clocking.

- If the supply voltage drops from 3.3V to 1.5V, then the allowable noise margin more than halves.
- Differential technologies do not have the noise margin concerns of single-ended technologies. This is due to common-mode rejection.
- The total crosstalk on a victim trace is the accumulated noise injected from all nearby noise sources.
- Forward crosstalk does not exist in the stripline configuration. The amplitude of the crosstalk is also considerably reduced.
- The simulator should be set to 150mV maximum crosstalk on all signals. However, crosstalk from within the same group, on synchronous buses, can be ignored unless the frequency is extremely high.
- Both forward and reverse crosstalk can be reduced by separating the aggressors from the victim traces or by reducing the height of the dielectric above/below the planes.

References:

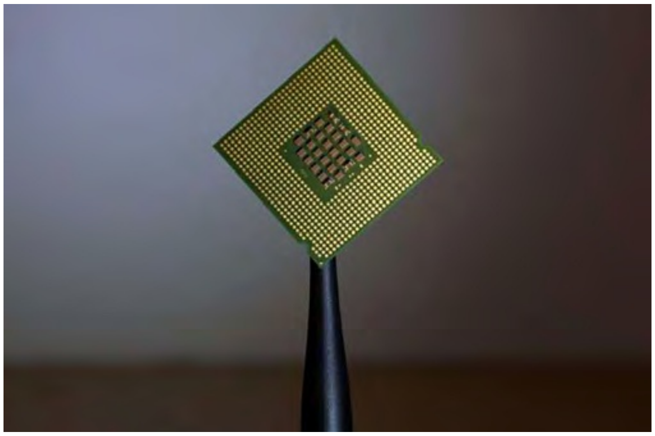
1. Barry Olney's Beyond Design columns: Controlling the Beast, A New Slant on Matched Length Routing, Board-Level Simulation and the Design Process: Plan B – Post Layout Simulation.
2. High-Speed Signal Propagation, by Howard Johnson.
3. All simulations performed in HyperLynx LineSim.

Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN and CPW Planner. The software can be downloaded from www.icd.com.au. To contact Olney, or read past columns, click here.

The Future of Electronics is Chemical

Molecular electronics, which aims to use molecules to build electronic devices, could be the answer. But until now, scientists haven't been able to make a stable device platform for these molecules to sit inside which could reliably connect with the molecules, exploit their ability to respond to a current, and be easily mass-produced.

An international team of researchers, including Macquarie University's Associate Professor Koushik Venkatesan, have developed a proof of concept device which they say addresses all these issues. The team exploited the fact that metallic nanoparticles can provide reliable electrical contacts to individual molecules, allowing them to transport charge through a circuit.



"Imagine a miniaturised transistor made up of several single molecules," says Koushik. "That's the promise of molecular electronics–devices that are smaller, faster, have more memory and are cheaper to make."

Koushik is confident their research will open up the bottleneck for this molecular-based technology to move forward.

"This fundamental research is extremely exciting as it points the way to practically 'wiring molecules' by exploiting the fact that Koushik and his colleagues have made a metallic nanoparticle provide a reliable electrical contact to individual molecules," says Professor Alison Rodger, Head of the Department of Molecular Sciences at Macquarie University.

"It is amazing to think that this work leads the way to true molecular-sized electronic circuits."

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