

# Utilizing a Field Solver for Stackup Planning

## Beyond Design

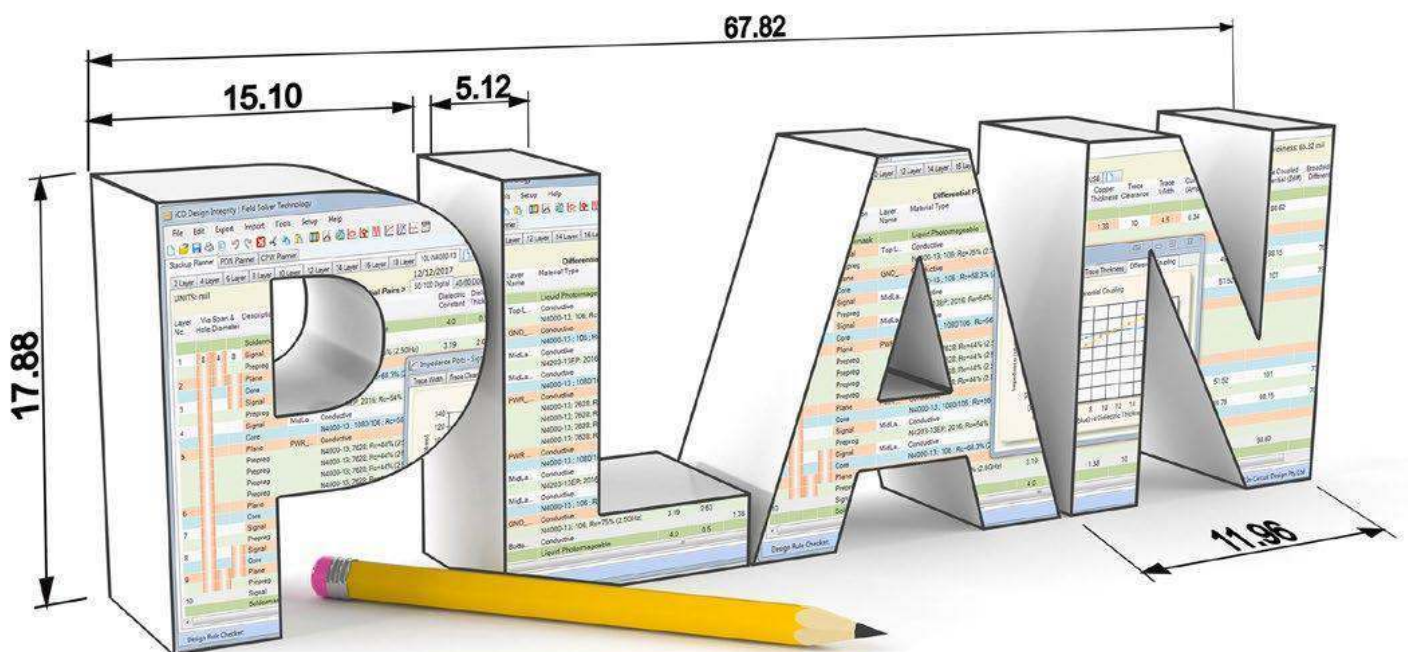
by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

In a previous column, I deliberated on why the 2D field solver is an essential tool for all high-speed PCB designers. But like all tools, one needs to know how best to apply its unique features to enhance your design process. Obviously, calculating transmission line impedance, in its various forms, is the prime function but field solvers can also provide additional information to ensure good design practice long before the layout begins.

Many PCB designers believe that it is the fabrication shop's role to calculate all the required impedances at the end of the process to best suit the materials that they stock. But by then,

it's too late; the horse has already bolted. It is difficult and time-consuming to go back and change the constraints once the board is complete.

So, where do we start to build the perfect stackup for our project? Initially, virtual materials are used to get the rough numbers. Then the impedance is fine-tuned once the actual materials are substituted. Every digital board will require 50-ohm impedance and generally a 100-ohm differential pair. This is our target impedance. However, multiple technologies are often used on complex designs which need to be accommodated on the same layer.



Keep these tips in mind when planning the board stackup:

- All signal layers should be adjacent to and closely coupled to an uninterrupted reference plane, which creates a clear return path and eliminates broadside crosstalk.
- There is good planar capacitance to reduce AC impedance at high frequencies. Closely coupled planes reduce AC impedance at the top end and dramatically reduce electromagnetic radiation.
- High-speed signals should be routed between the planes to reduce radiation.
- Reducing the dielectric height will result in a large reduction in your crosstalk without having a negative impact on available space on your board.
- The substrate should accommodate several different technologies. For example, 50/100 ohm digital, 40/80 ohm DDR3/4 and 90 ohm USB.

Unfortunately, not all these rules can be accommodated on a four- or six-layer board simply because we have to use a buffer core in the center to realize the total board thickness of 62 mils. However, as the layer count increases, these rules become more critical and should be adhered to.

Given the luxury of more layers:

- Electromagnetic compliance (EMC) can be improved or more routing layers can be added.
- Power and ground planes can be closely coupled to add planar capacitance, which is essential for GHz plus design.
- The power distribution networks (PDNs) can be improved by substituting embedded capacitance material (ECM) for the planes.
- Multiple power planes/pours can be defined to accommodate the high number of supplies required by today's processors and FPGAs.

- Multiple ground planes can be inserted to reduce the plane impedance and loop area.

Although power planes can be used as reference planes, the ground is more effective, as local stitching vias can be used for the return current transitions rather than stitching decoupling capacitors, which add inductance. This keeps the loop area small and reduces radiation. As the stackup layer count increases, so does the number of possible combinations of the structure. But if one sticks to the basic rules then the best performing configurations are obvious.

So, the big question everyone asks is about determining layer count. A good place to start is looking at a reference design with similar characteristics and then adding two layers. I say to add two additional layers because reference designs are typically squeezed onto as few layers as possible. But if one wants to avoid routing signals on the outer microstrip layers and reduce signal propagation skew and electromagnetic emissions, the extra layers will be needed.

Experienced PCB designers get a feel for it after a while, but a good way to check whether you have enough layers is to autoroute the board. With no tweaking, the autorouter needs to complete at least 85% of the routes to indicate the selected stackup is routable. The performance of the autorouter also impacts the completion rate. You may have to re-evaluate the placement a couple of times to get the best results. In general, eight layers is a good starting point for DDR type designs. Remember, it is much easier to increase the number of layers than to reduce them, so start with the minimum.

A field solver can be used to determine the unknown variables for an established impedance goal (Figure 1). Impedance plots use multiple passes of the field solver to plot the curve of impedance vs. dielectric thickness. In this case, a 3-mil prepreg is required to achieve

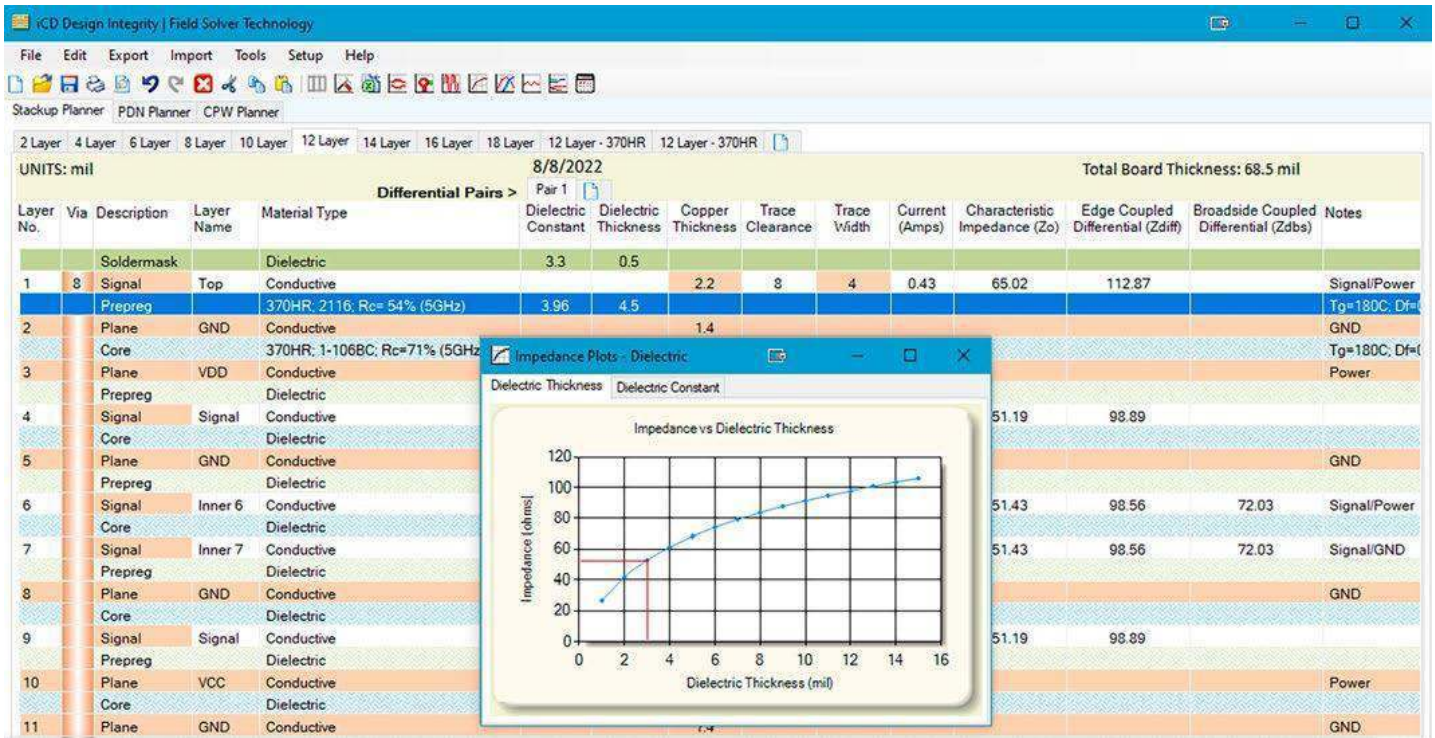


Figure 1: A field solver can be used to determine the required dielectric thickness (simulated in the iCD Stackup Planner).

50 ohms impedance. Dielectric constant, trace thickness, width and clearance can also be established in this way.

For DDR type designs, I like to start with closely coupled plane pairs on the second and third layers from the top and bottom (Figure 2).

Unfortunately, standard decoupling capacitors have little effect over 1 GHz and the only way to reduce the impedance of the PDN above this frequency is to use tightly coupled power/ground plane pairs or, alternatively, on-die capacitance. These plane pairs should be positioned

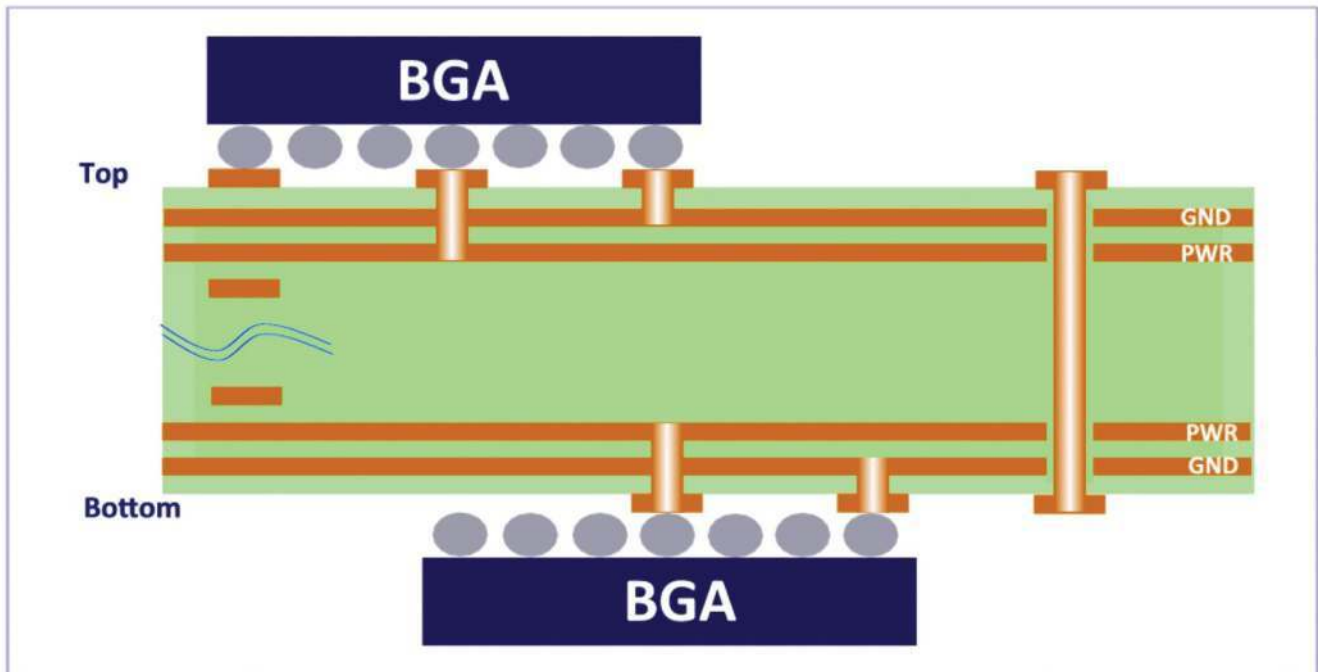


Figure 2: Tightly coupled plane pairs reduce loop inductance.





Figure 5: Relative signal propagation of microstrip and stripline, simulated in iCD Design Integrity.

The electric fields surrounding the microstrip exist partially within the dielectric material(s) and partially within the surrounding air. Since air has a dielectric constant of one, which is always lower than that of FR-4 (typically 4.3), mixing a little air into the equation will speed up the signal propagation. Even if the trace widths are adjusted on each layer, so that the impedance is identical, the propagation speed of microstrip is always faster than stripline, typically 13–17% (Figure 5). The speed of propagation of digital signals is independent of trace geometry and impedance.

If you are aware of this issue, then the trace delays can be matched to compensate for the varying flight time, so that at the nominal temperature, all signals running on either microstrip or stripline will arrive at the receiver simultaneously.

Unfortunately, drivers do not have the same impedance as the transmission line (typically 10–35 ohms) so terminations are used to balance the impedance, match the line, and minimize reflections. Reflections occur whenever the impedance of the transmission line changes along its length. This can be caused by unmatched drivers/loads, layer transitions,

different dielectric materials, stubs, vias, connectors and IC packages. By understanding the causes of these reflections and eliminating the source of the mismatch, a design can be engineered with reliable performance.

As shown in Figure 6, using a 12 mA LVCMOS 1.8V driver of a Spartan 6 FPGA, an 18.7-ohm series resistor is required to match the driver to the 51.67 ohm trace on the outer layer. This is automatically derived from the IV curves of the Spartan

6, IBIS model by the iCD Termination Planner (Figure 6). Correct termination is extremely important as it reduces transmission line reflections that can cause multiple issues for the design integrity.

So, apart from the accurate determination of single-ended, differential and broadside couple impedance, a field solver can offer further insight to enhance the signal and power integrity of a design.

## Key Points

- Although power planes can be used as reference planes, the ground is more effective.
- To calculate the layer count, look at a reference design with similar characteristics and then add two layers.
- With no tweaking, the autorouter needs to complete at least 85% of the routes to indicate the selected stackup is routable.
- It is much easier to increase the number of layers than to reduce them.
- A field solver can be used to determine the unknown variables for an established impedance goal.

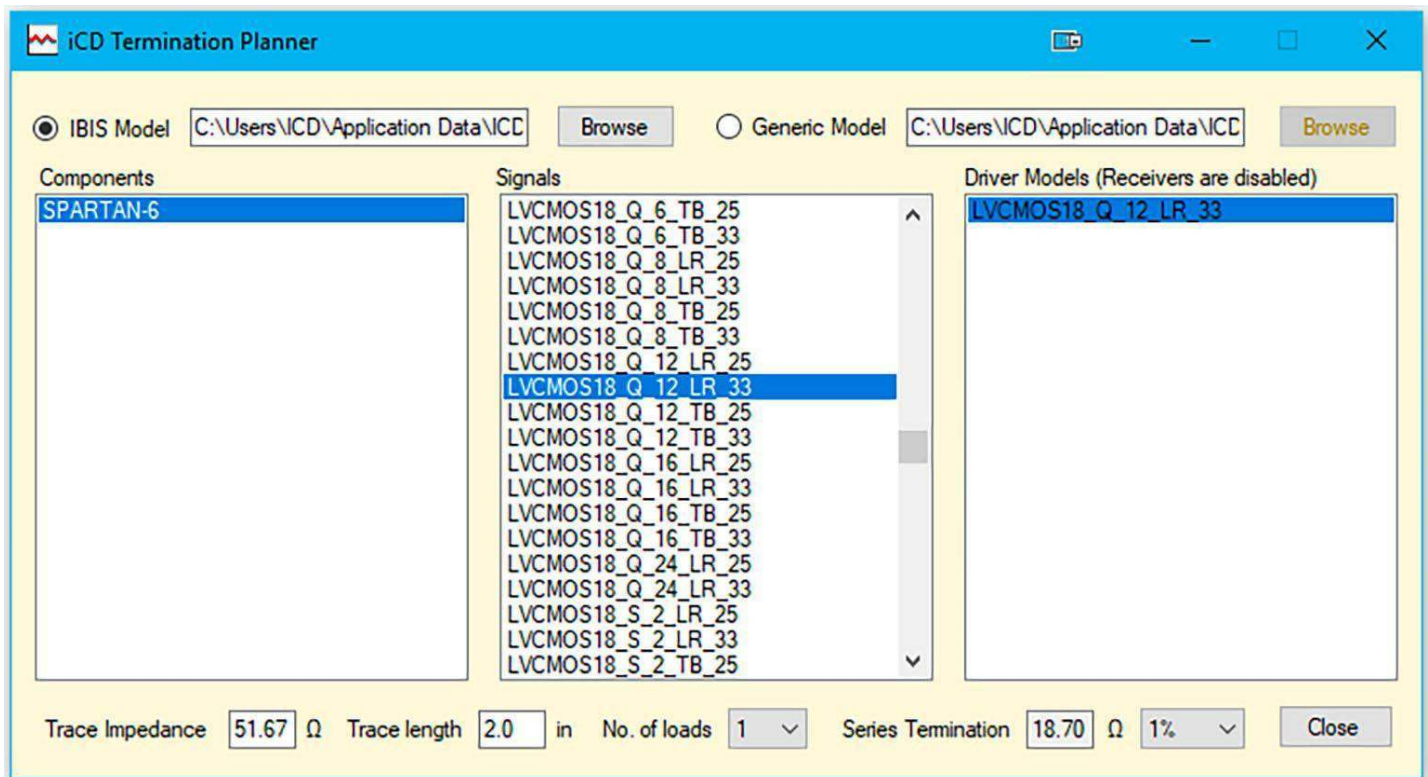


Figure 6: Matching the Spartan 6 driver to the transmission line. (Source: iCD Termination Planner)

- For DDR type designs, start with closely coupled plane pairs on the second and third layers from the top and bottom. These plane pairs should be positioned in the stackup close to and directly below/above the IC.
- The ability to extract the plane pair data and via size from the stackup to a PDN planner allows one to see the plane resonance and the impact it has on the AC impedance of the PDN.
- The AC impedance of the PDN should be kept below the target impedance up to the fifth harmonics of the fundamental.
- Plane resonance can be dampened by adjustments to the dielectric constant and thickness as well as plane size to avoid anti-resonance peaks.
- If critical signals are routed on the outer microstrip layers, then there will be a large discrepancy in timing due to the variance in flight time through different materials of the outer microstrip and inner stripline layers.

- The propagation speed of microstrip is always faster than stripline—typically by 13-17%.
- The speed of propagation of digital signals is independent of trace geometry and impedance.
- Drivers do not have the same impedance as the transmission line, so terminations are used to balance the impedance. **DESIGN007**

#### Resources

1. Beyond Design by Barry Olney: Signal Flight Time Variance in Multilayer PCBs; Stackup Planning Parts 1-6; The Fundamental Rules of High-Speed PCB Design Part 2; The Impact of PDN Impedance on EMI.



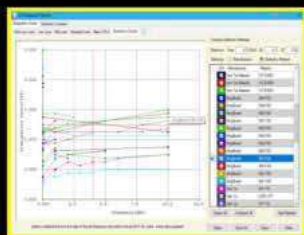
**Barry Olney** is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software

incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded at [www.icd.com.au](http://www.icd.com.au). To read past columns, [click here](#).

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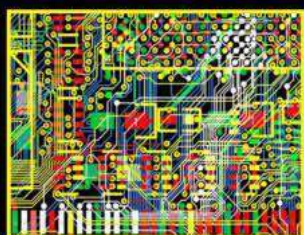


### A Comprehensive Report Includes:

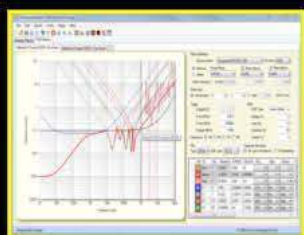
Material Selection for Cost/Performance to Required Frequency and Bandwidth, Design Constraint Review



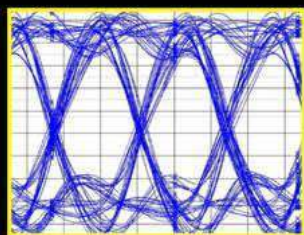
Stackup Impedance Analysis, Single-ended, Differential Pairs and CPW Blind and Buried Via Definition, Reference Plane Assignment Validation



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