

iCD Design Integrity

Incorporates the iCD Stackup and PDN Planner software. Offers PCB Designers unprecedented simulation speed, ease of use & accuracy at an affordable price

Dielectric Materials Library
30,700 Rigid & Flex Materials to 100GHz

Termination Planner
Extracts V Curves from IBIS Models
Calculates Series Terminator of the Distributed System including Loads

iCD Stackup Planner
Field Solver Accuracy, Characteristic Impedance, Edge & Broadside Coupled Differential Impedance

Layer No.	Via Spacer	Material	Thickness	Dielectric Constant	Loss Tangent	Trace Thickness	Trace Width	Current (Amps)	Characteristic Impedance (Ohm)	Edge Coupled Differential (dB)	Broadside Coupled Differential (dB)
1	4	FR4	0.127	4.5	0.02	0.05	12	0.08	42.58	81.23	
2		FR4	0.127	4.5	0.02	0.05	12	0.08	42.58	81.23	
3		FR4	0.127	4.5	0.02	0.05	12	0.08	42.58	81.23	
4		FR4	0.127	4.5	0.02	0.05	12	0.08	42.58	81.23	
5		FR4	0.127	4.5	0.02	0.05	12	0.08	42.58	81.23	
6		FR4	0.127	4.5	0.02	0.05	12	0.08	42.58	81.23	
7		FR4	0.127	4.5	0.02	0.05	12	0.08	42.58	81.23	
8		FR4	0.127	4.5	0.02	0.05	12	0.08	42.58	81.23	
9		FR4	0.127	4.5	0.02	0.05	12	0.08	42.58	81.23	
10		FR4	0.127	4.5	0.02	0.05	12	0.08	42.58	81.23	

iCD Stackup Planner - Offers Engineers & PCB Designers unprecedented simulation speed, ease of use and accuracy at an affordable price

- Industry Leading 2D (BEM) Field Solver precision
- Characteristic impedance, edge-coupled & broadside-coupled differential impedance
- Relative Signal Propagation with 'Matched Delay Optimization'—ideal for DDRx design
- Termination Planner - series termination based on IBIS models & distributed system
- Unique Field Solver computation of multiple differential technologies per signal layer
- Extensive Dielectric Materials Library—over 30,700 rigid & flexible materials up to 100GHz
- Interfaces—Allegro, Altium, Excel, HyperLynx, OrCAD, PADS, Zmetrix TDR, Zuken & IPC-2581B

iCD PDN Planner - Analyze multiple power supplies to maintain low AC impedance over entire frequency range dramatically improving product performance

- Fast AC impedance analysis with plane resonance and projected EMI
- Definition of plane size, dielectric constant & plane separation
- Extraction of plane data from the integrated iCD Stackup Planner
- Definition of voltage regulator, bypass/decoupling capacitors, mounting loop inductance
- PDN EMI Plot with FCC, CISPR & VCCI Limits. Frequency range up to 100GHz
- Extensive Capacitor Library—over 5,650 capacitors derived from SPICE models

"iCD Design Integrity software features a myriad of functionality specifically developed for high-speed design."
- Barry Olney



When Do Traces Become Transmission Lines?

by Barry Olney

IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

At low frequencies, traces and components on a PCB behave simply as lossless lumped elements—as taught in Circuit Theory 101. But as the frequency increases, the copper trace and adjacent dielectric(s) become a transmission line, the skin effect forces current into the outer regions of the conductor and frequency dependant losses impact on the quality of the signal.

The PCB trace now behaves as a distributed system with parasitic inductance and capacitance characterized by delay and scattered reflections. The behavior we are now concerned about occurs in the frequency domain rather than the familiar time domain. This is the real world of high-speed design.

Ideally, square wave signals are just that—perfect square waves with an evenly, sloping rising and falling edge. However, in the real world, things are quite different. Figure 1, illustrates the rising edge of a square wave, in the ideal case (low frequency), compared to the real world (high frequency). The transmission line effects create under and overshoot resulting in ringing in the signal. If this ringing crosses the voltage input high threshold (VIH), at the receiver, then it may cause false triggering.

The Fourier theorem states that every function can be completely expressed as the sum of sines and cosines of various amplitudes and frequencies. The Fourier series expansion of a square wave is made up of a sum of odd harmonics. Figure 2 shows the conversion of a square wave from the time domain to the frequency domain and the resultant amplitudes of the frequency components. If the waveform has an even mark-to-space ratio, then the even har-

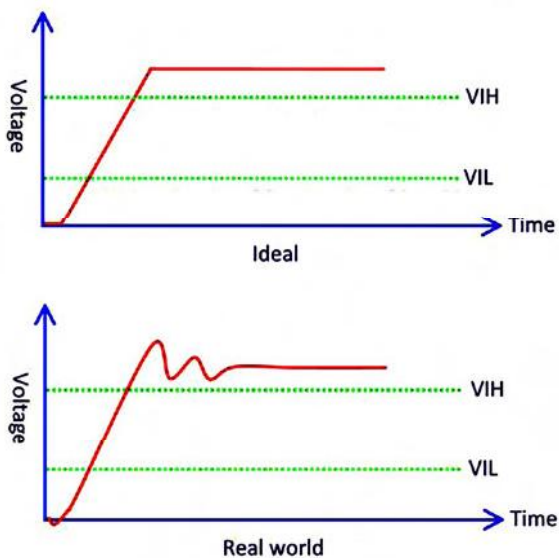


Figure 1: Ideal vs real-world rising edges.

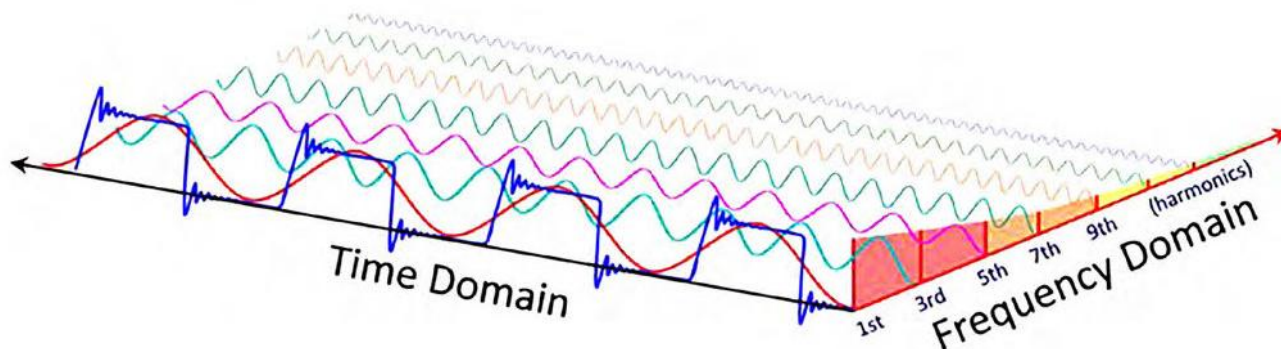


Figure 2: Harmonics of a square wave converted from the time domain to the frequency domain.

monics cancel. The high-frequency content of a square wave is significantly affected by the rise time of the waveform. Also, as the frequency increases, the amplitude decreases. In the real world, one needs to consider the maximum bandwidth of a signal, including harmonics, rather than assume the perfect square wave fundamental frequency model.

Surprisingly, even at very low frequency, an old-fashioned telegraph line is a transmission line simply because the wire length is comparable to the signal rise time. In recent years, edge rates have become much faster, to the point where short traces, on a PCB, are a small multiple of the edge rates propagating through them. As such, one should consider these PCB traces to be transmission lines and analyze their signal integrity.

In general, all drivers whose trace length (in inches) is equal to or greater than the rise time (in nanoseconds) should be considered critical and treated as high-speed transmission lines. It is the signal rise/fall time, rather than the signal clock frequency, that determines the critical signal speed. However, a steep rise/fall time may be slowed by loading the signal line with a damping/back-matching resistor close to the source.

Impedance is the key factor that controls the stability of a design—it is the core issue of both the signal and power integrity methodology. At low frequencies, a PCB trace is almost an ideal circuit with little resistance, and without capacitance or inductance. Current follows the path of least resistance. But at high frequencies, alternating current circuit characteristics dominate causing inductance and capacitance to become prevalent. Current then follows the path of least inductance. The impedance of an ideal, lossless transmission line is related to the capacitance and inductance:

$$Z_0 = \sqrt{L/C}$$

But this is very simplistic and the impedance should be simulated by a field solver to obtain accurate values, of impedance, for each signal layer of the substrate. The impedance of the trace is extremely important, as any mismatch along the transmission path will result

in a reduction in quality of the signal and possibly radiation of noise. For perfect transfer of energy, the impedance at the source must equal the impedance at the load. However, this is not usually the case and terminations are generally required, at fast edge rates, to limit ringing.

50 to 60 ohms characteristic impedance is often used in high-speed designs. Lower impedance values cause excessive dI/dt crosstalk and can double the power consumed to create a heat dissipation problem. Higher impedances not only produce high crosstalk, but also produce circuits with greater electromagnetic emissions and sensitivity. However as core voltages drop, rise times become faster and frequency increases, and a lower impedance is more desirable. For example, DDR3/4 memory buses use 40 ohm characteristic and 80 ohm differential impedance.

Figure 3 details the actual input impedance measured with a vector network analyzer (VNA), looking into a one inch transmission line with the other end open. This looks remarkably similar to the AC impedance of a plane cavity's resonance, which also has no termination. However, the plane pair has more area and therefore much more capacitance and less inductance than a trace, making the resonance lower in frequency and providing a very low impedance path. So, planes simply act as big, fat, unterminated transmission lines.

This transmission line was designed to have a characteristic impedance of 50Ω but the frequency dependant losses impact on the quality of the signal. The frequency domain transmitted and reflected data is respectively referred to as insertion and return loss. The characteristic impedance (Z_0), that is commonly used to specify trace impedance, is defined as the instantaneous impedance of a lossless transmission line.

The most fundamental signal integrity analysis involves defining the board stackup, including appropriate dielectric constants and layer thicknesses, and determining the appropriate trace width (and clearance for differential signals) that corresponds with the target characteristic and differential impedance for the traces. However, selecting the right impedance, and other transmission line characteristics, are essential to generating accurate results.

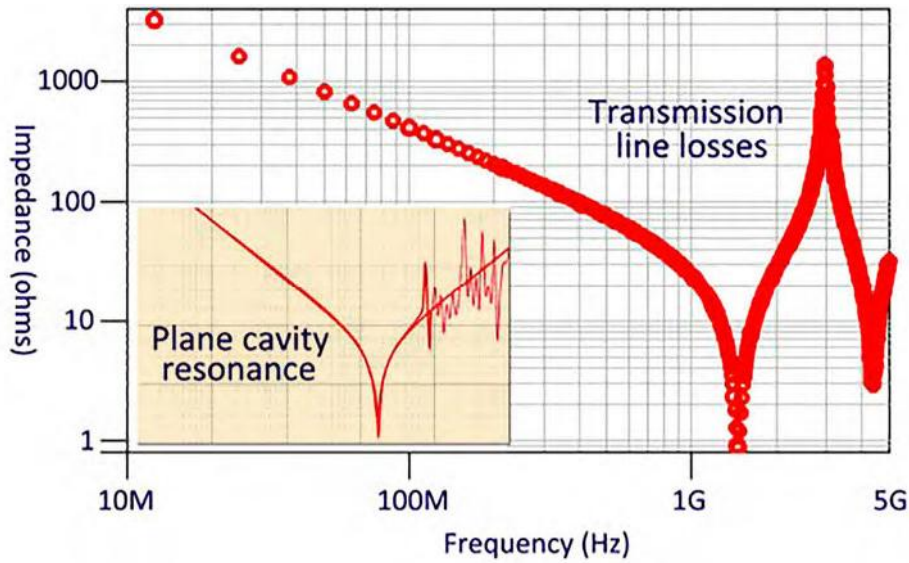


Figure 3: A 50Ω, 1-inch trace measured with a vector network analyzer (source: Eric Bogatin).

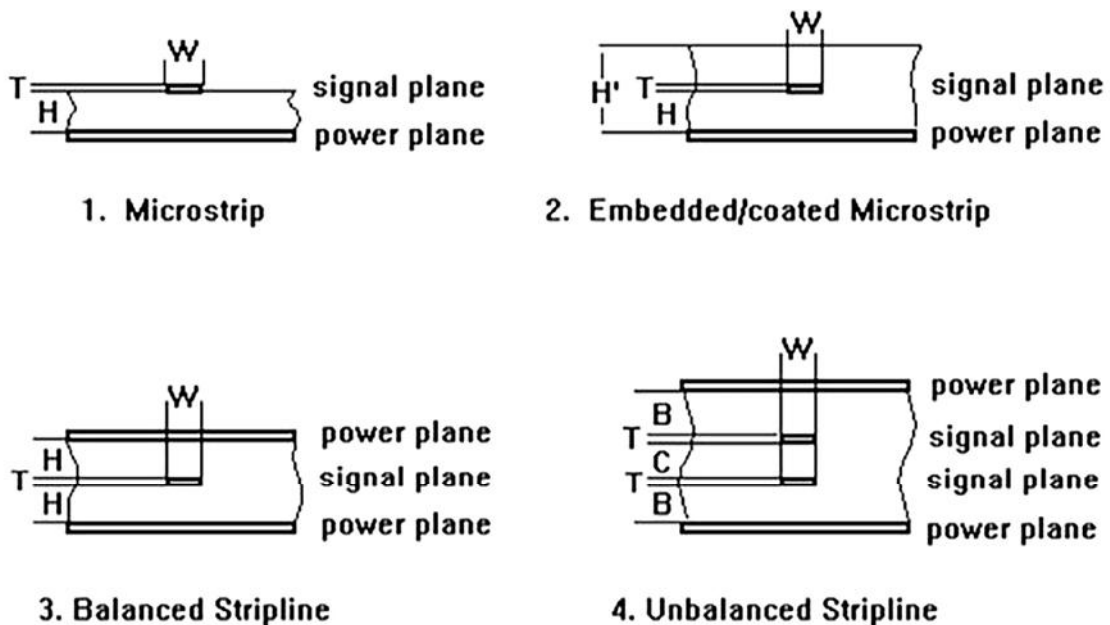


Figure 4: The four main configurations of impedance structures (source: IPC-2251).

Multilayer PCBs are ideally suited for providing interconnection wiring that is specifically designed to provide desired levels of impedance control. Techniques commonly referred to as microstrip and stripline are employed for impedance control. There are four basic types of transmission line constructions, as shown in Figure 4:

1. Microstrip
2. Embedded microstrip (with solder mask or conformal coating)
3. Balanced stripline (aka symmetric stripline)
4. Unbalanced or dual embedded stripline (aka asymmetric stripline)

It is important to note the variation in dielectric constant (ϵ_r or D_k) that different materials can exhibit. For instance, air has an $\epsilon_r = 1$, whereas an aluminum stiffener may have an $\epsilon_r = 10$ and then there are barium oxides that go up to 600. Standard FR-4 has an $\epsilon_r = 4$ and dielectrics specifically designed to be used for high-speed designs have a very low dielectric constant. For instance, Isola Astra-MT77 100GHz material has an $\epsilon_r = 3$. The dielectric constant has a direct impact on impedance and the signal propagation through the substrate. That is why the dielectric constant for a specific material should always be obtained from the supplier's specification (or a reliable source) that lists the ϵ_r at different frequencies. Please note that datasheets generally list the dielectric constant as D_k .

Closed-form equation-based impedance calculators have been around for many years, but unfortunately, they are extremely limited in accuracy. Many examples can be found on the internet and generally their results are just rough estimations but where they all come totally unstuck is in the calculation of dual embedded (asymmetric) stripline. IPC published impedance equations in the original IPC-D-317 and later in the IPC-2251 standard. The later was based on Brian C. Wadell's book *Transmission Line Design Handbook*, but even these quite elaborate equations are unable to cope with wide unbalances in surrounding dielectric in the stripline configuration. Since impedance is the key factor that controls the stability of a design, one should never compromise the accuracy required, for high-speed design, and the use of a precision field solver is mandatory.

I mentioned earlier that a steep rise/fall time may be slowed by loading the signal line with a damping/back-matching resistor close to the source. This also serves to match the impedance of the driver to the transmission line. Unfortunately, using mainstream PCB layout software, one really has no idea what the driver impedance is, let alone the capability to match the driver to the impedance of the transmission line. Driver impedance is typically low, com-

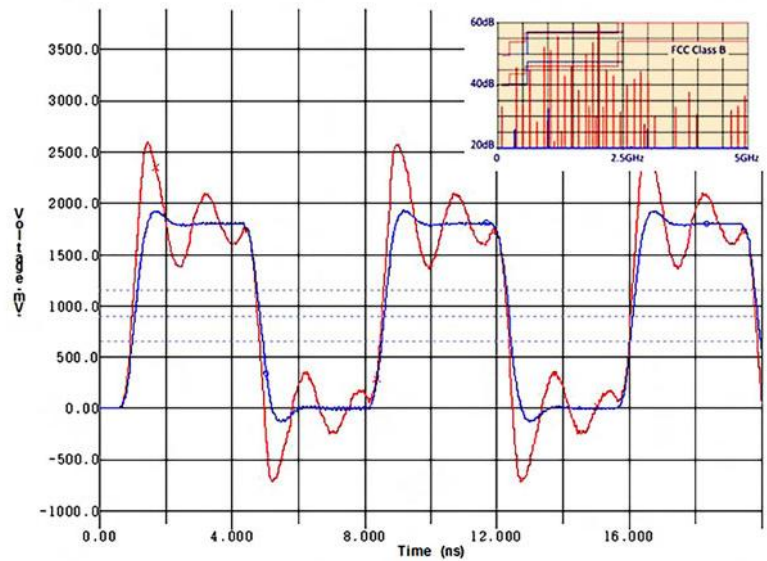


Figure 5: Ringing is reduced dramatically by adding a series terminator (simulated in HyperLynx).

pared to a typical 50 ohm transmission line, but adding a series resistor, of the correct value, solves this issue.

The need to terminate a PCB trace is based on several design criteria. The most important being an electrically long trace, when the length exceeds one sixth of the electrical length of the rising edge rate. But even if the trace is short, termination may still be required if the load is capacitive or highly inductive to prevent ringing. Series termination is excellent for point-to-point routes, one load per net. It also works well for traces that are electrically short and is used to fanout multiple loads radially from a common source (star routed) without affecting other circuits in the network. Series termination reduces ringing and ground bounce. It is the most common termination used for high-speed design.

Revisiting the real-world rise time edge rate (Figure 1), by placing a series terminator (close to the source) the ringing is reduced dramatically. This will reduce crosstalk and also knock off the radiation. In Figure 5, the red waveform is the original, ringing signal, and the blue waveform demonstrates the damping effect of a series resistor taking us back to a near ideal waveform. The insert is the projected emissions in the frequency domain.

High-speed digital design is all about controlling impedance. The impedance of the transmission lines needs to be matched and maintained at a constant value along the entire length of the interconnect. Also, the power distribution network needs to provide a low impedance path, through the planes, across the entire frequency bandwidth of the signal. These seemingly unrelated disciplines control the stability and reliability of the product. Get it right and your high-speed design is off to a great start; get it wrong and you are in for a (real) world of pain.

Points to Remember

- At high frequencies the PCB trace now behaves as a distributed system with parasitic inductance and capacitance characterized by delay and scattered reflections.
 - The transmission line effects create under and over shoot resulting in ringing in the signal.
 - The Fourier series expansion of a square wave is made up of a sum of odd harmonics.
 - A trace becomes a transmission line simply when the length is comparable to the signal rise time.
 - All drivers whose trace length (in inches) is equal to or greater than the rise time (in nanoseconds) should be considered critical and treated as high-speed transmission lines.
 - Impedance is the key factor that controls the stability of a design; it is the core issue of both the signal and power integrity methodology.
 - For perfect transfer of energy, the impedance at the source must equal the impedance at the load.
 - Terminations are generally required, at fast edge rates, to match the impedance and limit ringing.
 - As core voltages drop, rise times become faster and frequency increases, and a lower impedance is more desirable.
 - The measured input impedance of a transmission line looks remarkably similar to the AC impedance of a plane cavity's resonance which also has no termination.
- The characteristic impedance (Z_0), is defined as the instantaneous impedance of a lossless transmission line.
 - The most fundamental signal integrity analysis involves defining the board stackup, which is essential to generating accurate results.
 - Dielectrics, specifically designed to be used for high-speed design, have a very low dielectric constant.
 - Closed-form equation based impedance calculators are extremely limited in accuracy and the use of a precision field solver is mandatory.
 - A series resistor can be used to match the driver to the impedance of the transmission line.
 - Termination is required if the trace length exceeds one sixth of the electrical length of the rising edge rate.
 - High-speed digital design is all about controlling impedance. **PCBDESIGN**

References

1. Barry Olney's Beyond Design columns: [Controlled Impedance Design](#), [Impedance Matching: Terminations](#), [Signal Integrity Parts 1, 2 & 3](#)
2. [What's the Difference Between Signal Integrity and Power Integrity?](#) by Patrick Carrier
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4. [Bandwidth Basics](#), Wavelength Electronics
5. [IPC-2251](#)—Design Guide for the Packaging of High-Speed Electronic Circuit
6. [High-Speed Digital Design](#), by Howard Johnson



Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN and CPW Planner. The software can be downloaded from www.icd.com.au. To contact Olney, or read past columns, [click here](#).