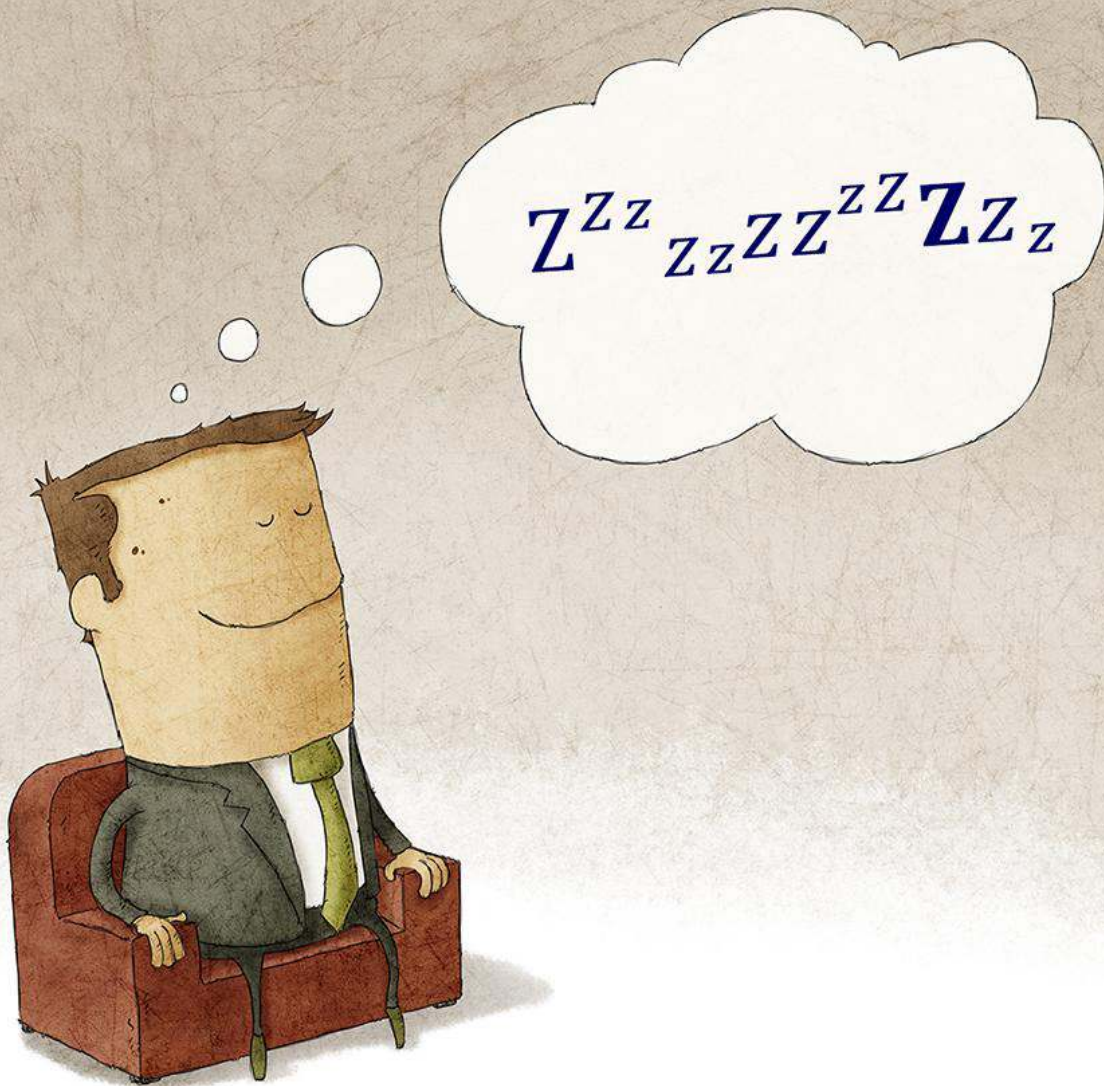


We DREAM Impedance!



Did you know that two seemingly unrelated concepts are the foundation of a product's performance and reliability?

- Transmission line impedance and
- Power Distribution Network impedance

DISCOVER MORE

iCD software quickly and accurately analyzes impedance so you can sleep at night.

iCD Design Integrity: Intuitive software for high-speed PCB design.

"iCD Design Integrity software features a myriad of functionality specifically developed for PCB designers."

– Barry Olney



Termination Planning

Beyond Design

Feature Column by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

The characteristic impedance of a transmission refers to the impedance seen by a driver looking down an infinitely long trace. Interestingly, the characteristic impedance is independent of trace length. It's a measure of the ratio of inductance to capacitance at any point along the trace. Therefore, while trace length matters for signal propagation delay, it doesn't directly impact characteristic impedance. When a transmission line is perfectly matched to the

driver and load, the signals propagating electromagnetic (EM) energy are totally absorbed by the load. This is the perfect scenario that all electronics designers strive for. However, this is rarely the case, and reflections do occur whenever the impedance of the transmission line changes along its length. Mismatched impedance causes signals to reflect back and forth along the lines, which causes ringing at the load (Figure 1). The ringing reduces the

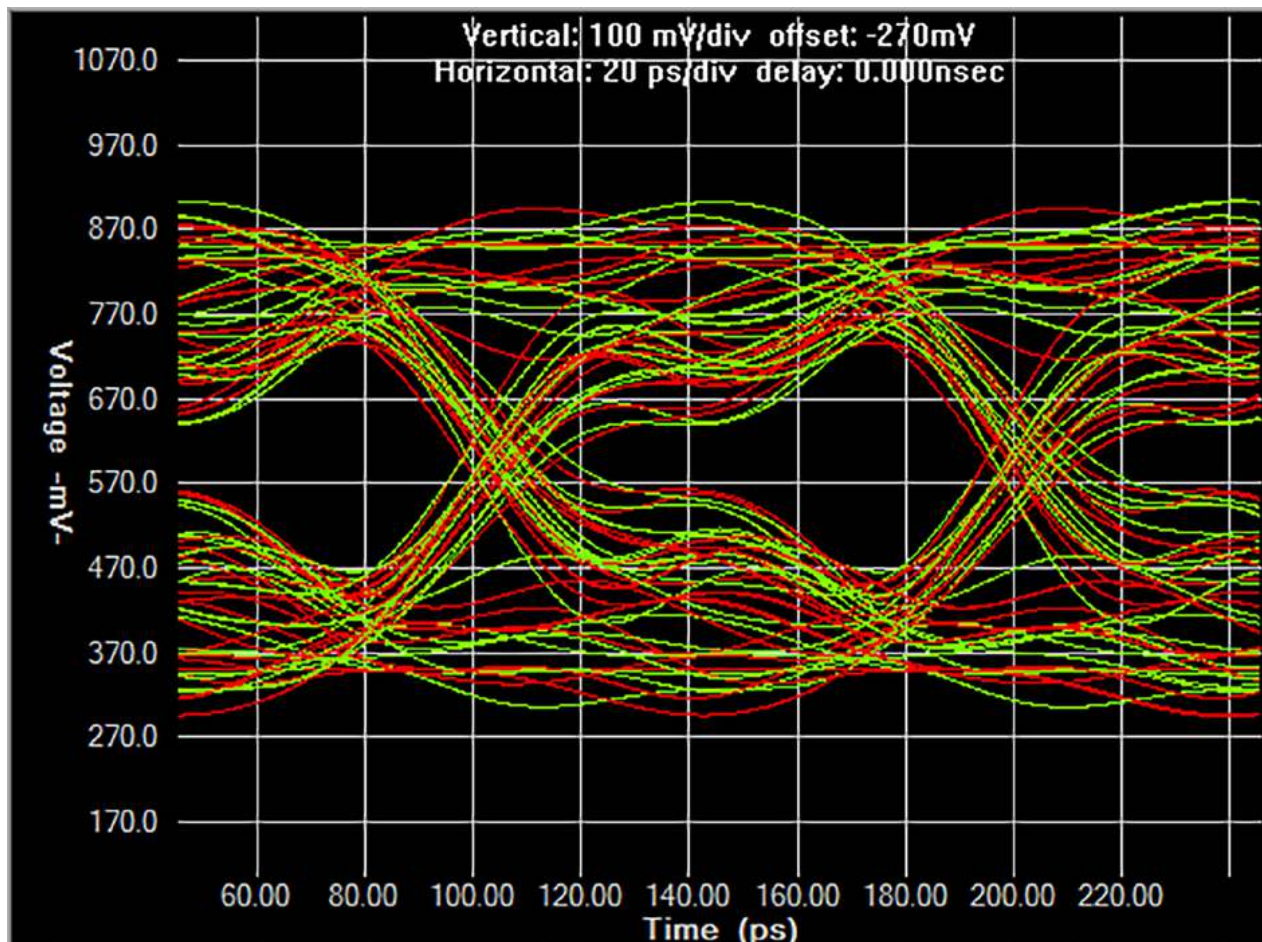


Figure 1: Reflections cause over/undershoot and jitter of the signal eye.

dynamic range of the receiver, eats into the noise budget, and can cause false triggering.

As signal rise times become faster, consideration should be given to the propagation time and reflections of a routed trace. If the propagation time and reflection from source to load are longer than the edge transition time, an electrically long trace will exist. If the transmission line is short, reflections still occur but they will be overwhelmed by the rising or falling edge and may not pose a problem. But even if the trace is short, termination may still be required if the load is capacitive or highly inductive to prevent ringing. Generally, when the trace length exceeds one-sixth of the electrical length of the rising edge rate, then termination is required.

We typically dampen reflections in high-speed PCB design by using resistive terminations (series or parallel) to match the impedance of the line to the driver. However, I have

also seen the reflections caused by using a driver strength that is too high for the load. Driver strengths typically range from 4 mA to 16 mA. A 16 mA driver is generally required for multiple loads—for instance, a DDR4 signal driving multiple SODIMM memory cards. In this case, the transmission lines are longer and the capacitive load higher, so simulation is necessary to confirm the required driver's current strength. To dampen the signal, terminations are typically placed on the memory card itself. However, if the signal is delivered to only one or two onboard memory devices, then the signal strength can usually be reduced to a minimum of 8 mA to prevent reflections.

With the driver strength set correctly, we need to determine if there is a mismatch of impedance. But how do you know the impedance of the driver and the transmission line? First, an accurate field solver is required to determine the impedance of the PCB traces (Figure 2).

The screenshot shows the iCD Stackup Planner interface with a table of layer properties and simulated trace impedances. The table includes columns for Layer No., Via Span & Hole Diameter, Description, Layer Name, Material Type, Dielectric Constant, Dielectric Thickness, Copper Thickness, Trace Clearance, Trace Width, Current (Amps), Characteristic Impedance (Zo), Edge Coupled Differential (Zdiff), and Broadside Coupled Differential (Zdbs).

Layer No.	Via Span & Hole Diameter	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)
1	8, 4, 8	Soldermask	Top	PSR-4000BV / CA-40BB LPI (1GHz)	3.3	0.5							
2		Signal	Conductive	370HR; 1080; Rc= 64% (10GHz)	3.76	2.8	2.17	20	6.8	0.63	39.87	78.19	
3		Plane	GND	Conductive			1.4						
4		Plane	VDD	Conductive			1.4						
5		Signal	Signal	Conductive			0.7	13.2	8	0.31	40.29	79.66	
6		Plane	GND	Conductive			1.4						
7		Signal	Inner 6	Conductive			1.4	15.7	6.1	0.42	40.72	80.45	56.84
8		Plane	GND	Conductive			1.4						
9		Signal	Inner 7	Conductive			1.4	15.7	6.1	0.42	40.72	80.45	56.84
10		Plane	VCC	Conductive			1.4						
11		Plane	GND	Conductive			1.4						
12		Signal	Bottom	Conductive			2.17	20	6.8	0.63	39.87	78.19	
		Soldermask	Bottom	PSR-4000BV / CA-40BB LPI (1GHz)	3.3	0.5							

Figure 2: iCD Stackup Planner simulates the trace impedance.

Then, the source impedance must be extracted from the input/output buffer information specification (IBIS) model of the driver IC. Subtracting the source impedance from the trace characteristic impedance gives the required series terminator value.

Unfortunately, drivers do not have the same impedance as the transmission line (typically 10–35 Ω) so series terminations are used to balance the impedance, match the line, and minimize reflections, particularly on long traces. Impedance matching slows down the rise and fall times, reduces the ringing (over/undershoot) of signal drivers, and enhances the quality of a high-speed signal.

Now that the impedance of the transmission line is solved, the next step is to extract the driver (source) impedance from the IBIS model of the device. But how do you extract the source impedance? IBIS models can be used to characterize I/V output curves, rising/falling waveforms and pin parasitics of the device packaging. The models' source impedance should be based on these I/V curves.

I recall a renowned signal integrity expert

once saying that it is impossible to extract the source impedance from the IBIS driver model. However, it is possible (otherwise simulators would not work), but it is a very time-intensive process, and tackling the I/V curves to determine the impedance should be left to precision software to solve (Figure 3).

One also needs to consider the on-die terminations (ODT) for high-speed memory devices. Although the termination resistors on the motherboard reduce some reflections on the signal lines, they are unable to prevent reflections resulting from the stub lines that connect to the components on the module card. As you can see, the Micron DDR4 device has various termination options, and each of these will result in a different waveform at the load.

On-die terminations can be used with some memory devices to match the transmission line and dampen the reflections. Incorporating a resistive termination within the DRAM device improves the signaling environment by reducing the electrical discontinuities introduced with off-die termination. DDR4 and DDR5

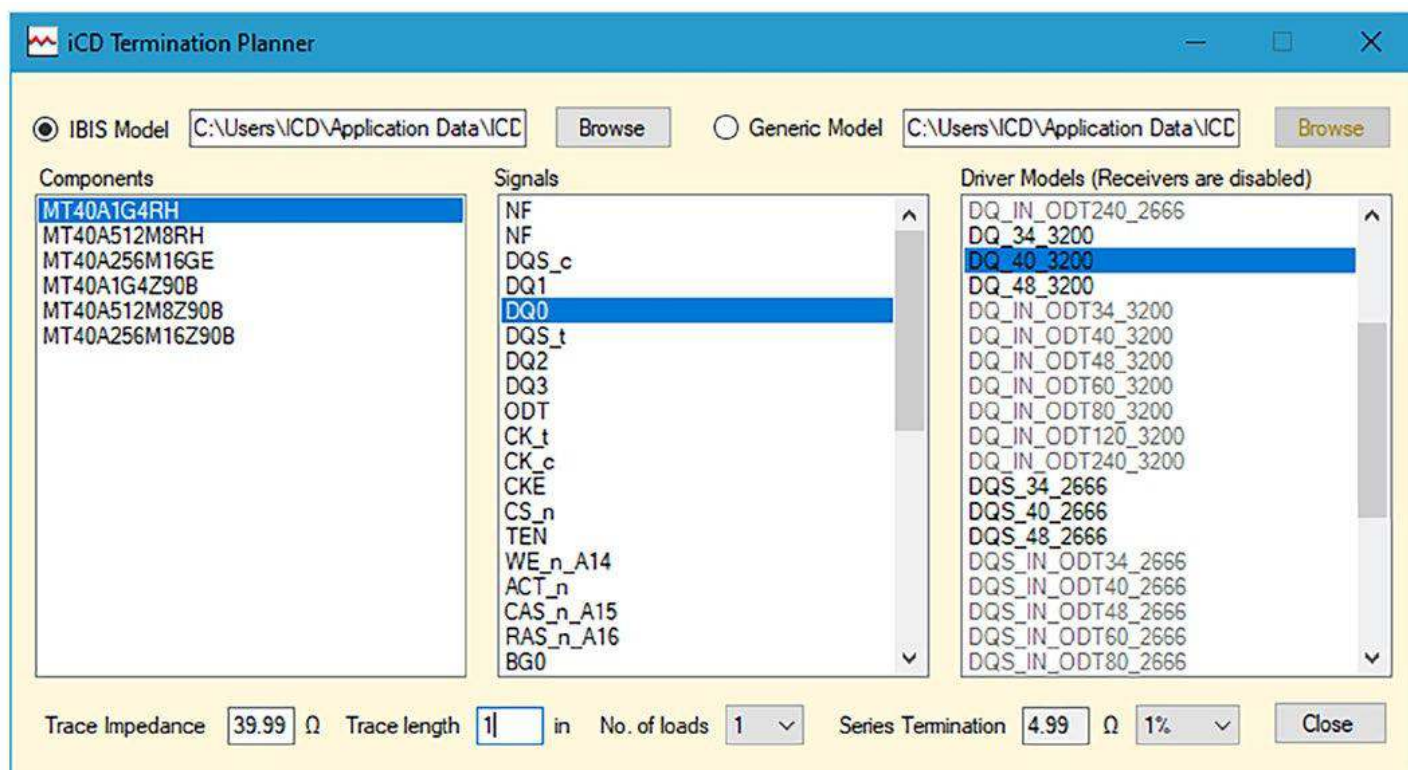


Figure 3: Micron 4 Gb DDR4-3200 SDRAM with ODT. (Source: iCD Termination Planner)

technology, like DDR3, include ODT on the data I/O pins. This feature is controlled by the ODT pin and consumes additional power when activated. The ODT and the output driver on DDR4 devices include additional mode register settings over the previous DRAM to increase system flexibility and optimize signal integrity. The ODT impedance can vary from 34-240 Ω in receive mode and 34-48 Ω in transmit mode in Figure 3. DDR4 signal-ended signals are normally routed on 40 Ω transmission lines, so for short trace lengths, with one load a 40 Ω ODT is perfect. However, since the ODT and driver strength are software-selectable, one can validate and tune the strength during the testing phase of development.

In the above case, the trace impedance is 39.99 Ω , and with one load the signal requires a 4.99 Ω series termination resistor to match the driver to the load. However, if there is more than one load (memory device), then the driving signal will need to rise faster. Hence, it will require a slightly smaller value of the series resistor.

I'm not aware of any current PCB design tool that can determine the driver source impedance and, hence, accurately calculate the required series terminator. This is normally delegated to expensive simulation software. So, in this case, having a field solver is of little use without the other half of the equation. However, the iCD Termination Planner and field solver are delivered as part of iCD's Stackup Planner offering.

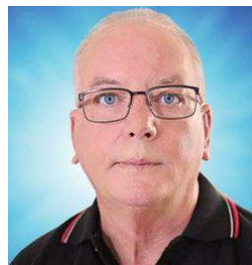
Key Points

- Characteristic impedance is independent of trace length.
- When a transmission line is perfectly matched to the driver and load, the signals propagating electromagnetic (EM) energy are totally absorbed by the load.
- Mismatched impedance causes signals to reflect back and forth along the lines, which causes ringing at the load.

- If the propagation time and reflection from source to load are longer than the edge transition time, an electrically long trace will exist.
- We typically dampen reflections in high-speed PCB design by using resistive terminations (series or parallel) to match the impedance of the line to the driver.
- Reflections are caused by using a driver strength that is too high for the load.
- Subtracting the source impedance from the trace characteristic impedance gives the required series terminator value.
- Series terminations are used to balance the impedance, match the line, and minimize reflections, particularly on long traces.
- The models' source impedance should be based on the I/V curves.
- On-die terminations can be used with some memory devices to match the transmission line and dampen the reflections.
- Having a field solver is of little use without the other half of the equation—a termination planner. **DESIGN007**

Resources

- Beyond Design: "Reflecting on Reflections," "Terminations," by Barry Olney



Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup,

PDN, and CPW Planner. The software can be downloaded at www.icd.com.au. To read past columns, [click here](#).