Beyond Design: The Target Impedance Approach to PDN Design

by Barry Olney | In-Circuit Design Pty Ltd | Australia

Today's high performance processors employ low DC voltages with high transient currents and high clock frequencies in order to minimize the power consumption and hence the amount of heat dissipated. A typical high-speed design contains ten or more individual power supplies. And unfortunately, the lower core voltages, higher currents and faster edge rates, all impact on the Power Distribution Network (PDN) design as well as signal integrity. The goal of robust PDN Planning is to design a stable power source, taking the above into account, for all the required on-board power supplies. In this month's column, I will look at the target impedance approach to PDN design.

Before you worry (or not) about post-layout PDN DC drop analysis, you first need to design an effective PDN pre-layout. Smart designers prevent problems before they arise–others waste time and resources trying to fix the mess that they inadvertently created due to lack of due diligence. Engineers and PCB designers need to visualize and understand how and where the currents flow. When I analyze a multilayer PCB, I immediately interpret the entire current loop including the return path by highlighting adjacent signal and associated plane layers. If you need to push a lot of current from one point to another, it is obvious where the hot spots will be. Increasing the plane copper thickness is a good solution, for DC and low frequency, but has little impact at high frequencies due to the skin effect. However effective placement, the use of minimal antipads and wide uninterrupted copper pours alleviates the issue before it arises.

The high clock frequencies and signal rates employed today push more of the physical board features into the 'red' zone where their relative dimensions, with respect to the wavelength of the clock, approach or exceed the quarter-wave limit. Quarter-wavelength or longer structures may become effective electromagnetic radiators; therefore the PDN has become one of the primary EMI risk factors for high-speed designers. It is generally accepted that the best way to avoid EMI radiation, from PDNs, is to ensure a resonance-free impedance profile. The resonance-free impedance profile also helps to minimize simultaneous switching noise (SSN) and jitter of high-speed signals, when the PDN serves as both a stable power source and signal reference.

In the early days, of digital electronics, there was no such thing as PDN design. Instead, the focus was on the maximum number of 100nF (and the odd 47pF) capacitors that could be placed close to the ICs power pins. Connecting a capacitor by a thick trace to a 60mil DIP power pad was easy–but try doing that with a dense BGA package. This approach was sufficient as long as the active devices did not generate significant transient noise spectrum above the Series Resonance Frequency (SRF) of the decoupling capacitors. However, higher system speeds later created the need to design the PDN systematically, to meet tighter impedance requirements.

Designers often procrastinate about whether it is better to have a thick trace routed directly from the decoupling capacitor (decap) to the BGA power pad (as in Figure 1), which eliminates the power via pair and reduces the loop area. But does this reduce the inductance? This trace has to be 25mils wide and 1mil thick to match a via of 8mils hole diameter with a 1mil barrel plating thickness (πd). The top trace has an inductance of 460pH whereas the power via pair and plane combination has a total loop inductance of 324pH. Therefore there is 30% less inductance, in this case, by directly connecting the decap to the planes (thermals should not be used on the via plane connections). Plus it is difficult, if not impossible, to route a 25mil trace to a BGA pad–particularly the internal pads. 10mil is more the norm which would dramatically increase the trace inductance. BGA power/ground vias go directly to the plane and so should the decap power/ground vias.

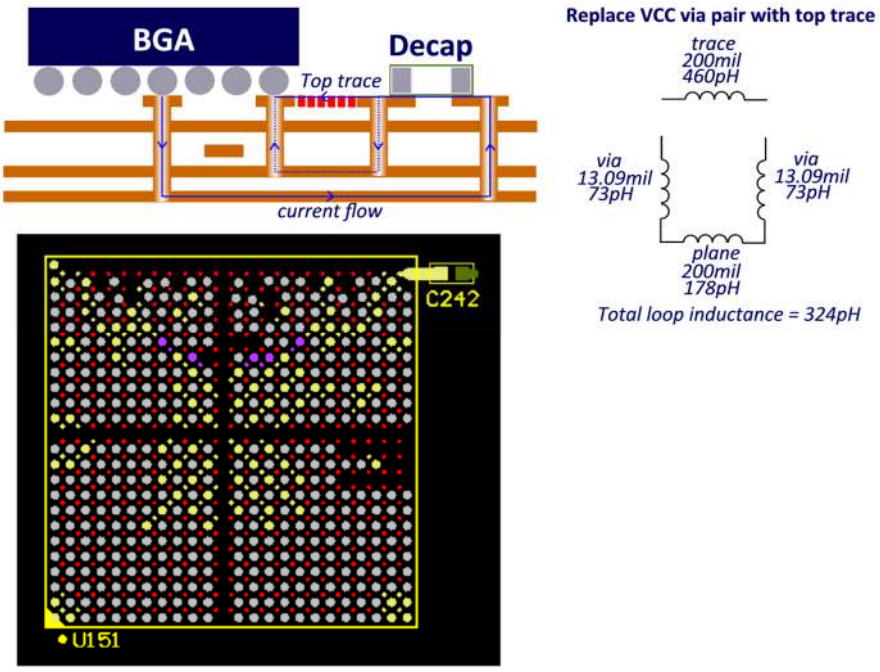

Figure 1–Trace on the top side eliminates the two vias but increases inductance

Also with high layer count stackups, the decaps should be placed around the perimeter of the IC on the same side of the board and routed directly to the planes. Placing decaps directly under the IC is also an 'obsession' of the past and may increase inductance and also impedes fanout and signal routing. Please see my previous column '[Beyond Design: PDN - Decoupling Capacitor Placement]' for further details.

Target impedance is the combination of the worst case transient current and the voltage noise specification which act together to set the maximum allowable PDN impedance with assured performance. The target impedance (*Ztarget*) is determined based on the maximum voltage rail noise (*ΔVnoise*)–VDD by the ripple voltage–and the worst case transient current (*Itransient*)–maximum current by the duty cycle.

$$Ztarget = \frac{\Delta Vnoise}{Itransient} = \frac{VDD\ x\ 5\%}{Imax\ x\ 50\%}$$

Ideally, the effective impedance of the PDN should be kept below the target impedance up to the maximum required bandwidth as in Figure 2. However, if the impedance is too far below the target, then this implies that the PDN has been overdesigned which unnecessarily increases costs with little added benefit. If your company intends building hundreds of thousands of assemblies, then the potential cost saving can be quite significant. Analyzing the PDN ensures best performance at the most cost-effective price.

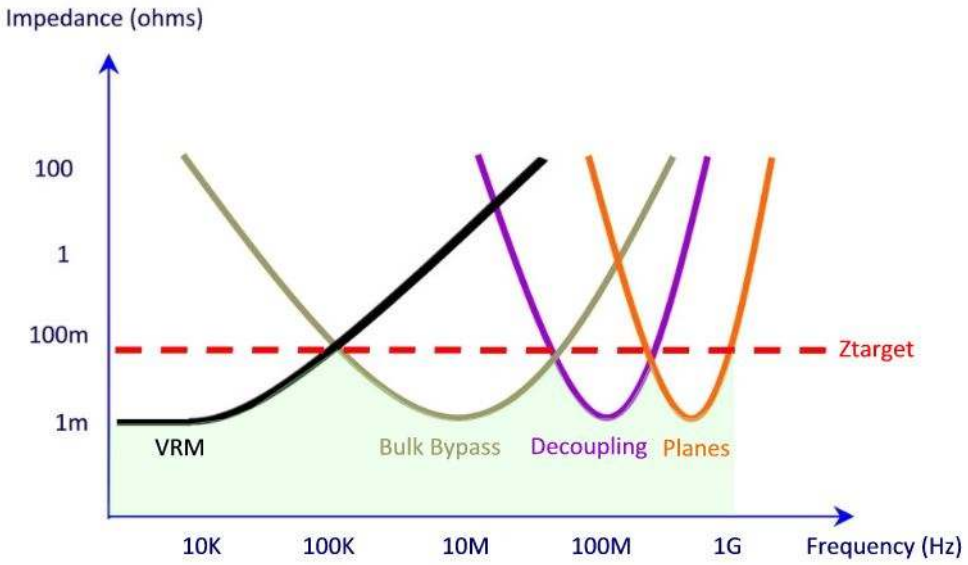

Figure 2–Fundamental Target Impedance, VRM, Capacitors and Plane Profiles

Target impedance is the most crucial metric when evaluating PDN performance. The further the PDN impedance is above the target impedance–the greater the risk of intermittent operation or even complete product failure.

In practice, accurately calculating the transient currents and the precise requirements for the target impedance can be challenging. Since we typically do not know the transient noise current excitation very accurately, it is customary instead to design the PDN to meet the required impedance profile. Also, it seems that the current portion of the target impedance equation varies from point-to-point, on the board, depending on a host of intricate relationships. One must always apply engineering judgment in translating the information available into the requirements for a cost-effective PDN design.

Fortunately, for Double Data Rate (DDR) memory, the power supply is only utilized for the memory ICs and the memory drivers/receivers of the processor. Transient currents from circuits on different clock domains are statistically independent. Meaning there is no interaction between PDN current (with the exception of any coupled noise) and therefore the DDR supply is isolated from the noise of other supplies assuming good design practice. Therefore, the target impedance calculated for the DDR PDN is sufficiently accurate.

However, within a single IC, there may be several circuit blocks that draw current from the same power rail. The same concept applies here: if the circuit blocks are independent (which is most likely the case if they are on different clock domains) then the RMS value of the transient currents can be combined. Using this concept, the target impedance for a single IC can be calculated from knowledge of the circuit blocks drawing current from the voltage rail in question. And at the PCB level, transient current drawn by several chips can be calculated statistically. This makes the target impedance a function of frequency. The circuit designer can combine the target impedances, for several chips on the same PCB power rail, by adding linearly at DC and low frequencies and statistically at higher frequencies.

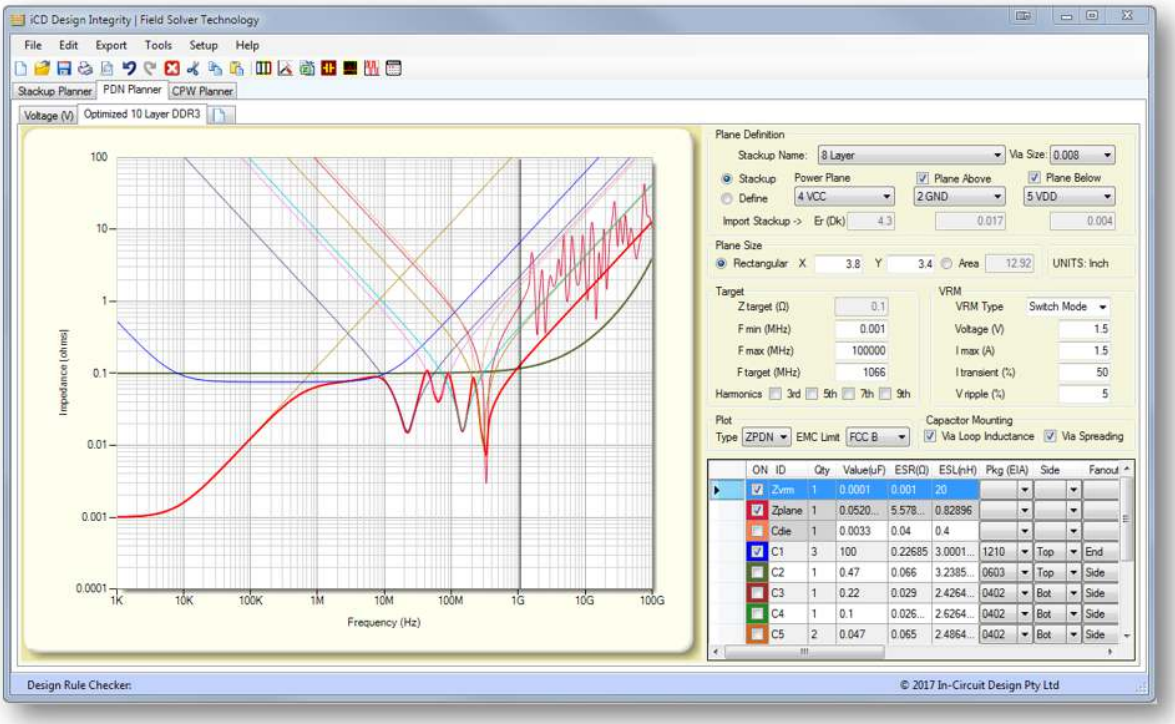

Figure 3–Optimized PDN Profile (simulated in iCD Design Integrity)

Generally, all circuits on the PCB will draw DC current at the same time and so the voltage regulator module (VRM) must be designed to accommodate the potential surges. But as the frequency approaches the 1GHz band, the probability of drawing transient currents in phase and at the same frequency greatly diminishes. As frequency goes up–peak currents become spatially isolated. The target impedance, at the different chip locations on the PCB, should reflect this in different frequency bands.

The PDN profile should be optimized (as in Figure 3) such that the effective impedance, of the combined VRM, bypass and decoupling capacitors and plane resonance, falls just below the estimated target impedance, of the PDN, up to the maximum required bandwidth.

Key Points:

- The goal of robust PDN Planning is to design a stable power source taking into account the worst case transient conditions.
- Smart designers prevent problems before they arise–others waste time and resources trying to fix problems.
- Engineers and PCB designers need to visualize and understand how and where the currents flow.
- Increasing the plane copper thickness is a good solution, to current hot spots, for DC and low frequency but has little impact, at high frequencies, due to the skin effect.
- Quarter-wavelength or longer structures may become effective electromagnetic radiators.
- The best way to avoid EMI radiation, from PDNs, is to ensure a resonance-free impedance profile.
- BGA power/ground vias go directly to the plane and so should the decap power/ground vias which reduces loop inductance by ~30%.
- Decaps should be placed around the perimeter of the IC on the same side of the board and routed directly to the planes.

- The effective impedance of the PDN should be kept below the target impedance up to the maximum required bandwidth.
- Target impedance is the most crucial metric when evaluating PDN performance.
- The circuit designer can combine the target impedances, for several chips on the same PCB power rail, by adding linearly at DC and low frequencies and statistically at higher frequencies.
- As frequency goes up–peak currents become spatially isolated.

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Target image–Modified from Melanie Boylan, Stomp Social Media Training

Bio:

Barry Olney is Managing Director of In-Circuit Design Pty Ltd (iCD), Australia. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN and CPW Planner, is a PCB Design Service Bureau and specializes in board level simulation. The software can be downloaded from www.icd.com.au