Predicting and Measuring Impedance

Beyond Design

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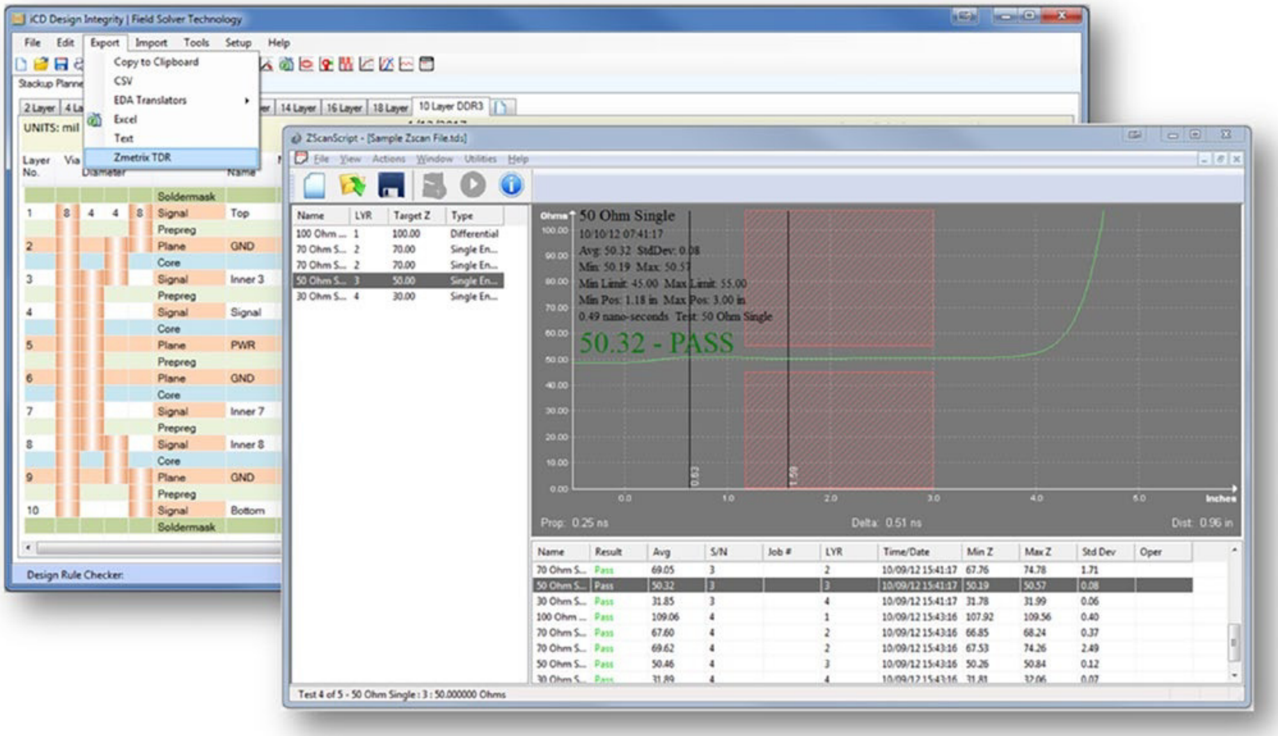
To control the impedance of high-speed signal interconnects, one first needs to predict the impedance of a specific multilayer stackup configuration. A precision field solver is arguably the most accurate way to calculate the single-ended, edge-coupled, and broadside-coupled differential impedance. Once the board is fabricated, the transmission lines need to be physically measured to determine the actual impedance to qualify the board (Figure 1).

The most common method for measuring PCB trace impedance is to use a time-domain reflectometer (TDR). This measures the impedance in the time domain. However, a far more accurate method is to use a vector network analyzer (VNA), which operates in the frequency domain. The VNA sweeps through a range of frequencies determining the impedance and signal losses at particular frequencies.

However, VNAs are expensive, delicate instruments and not as robust as a TDR (Figure 2), which allows unskilled personnel to operate

Figure 2: Zmetrix impedance test systems.



UNITS: mil

Layer No.	Via Diameter					Name
					Soldermask	
1	8	4	4	8	Signal	Top
					Prepreg	
2					Plane	GND
					Core	
3					Signal	Inner 3
					Prepreg	
4					Signal	Signal
					Core	
5					Plane	PWR
					Prepreg	
6					Plane	GND
					Core	
7					Signal	Inner 7
					Prepreg	
8					Signal	Inner 8
					Core	
9					Plane	GND
					Prepreg	
10					Signal	Bottom
					Soldermask	

Name	LYR	Target Z	Type
100 Ohm ...	1	100.00	Differential
70 Ohm S...	2	70.00	Single En...
70 Ohm S...	2	70.00	Single En...
50 Ohm S...	3	50.00	Single En...
30 Ohm S...	4	30.00	Single En...

50 Ohm Single
10/10/12 07:41:17
Avg: 50.32 StdDev: 0.08
Min: 50.19 Max: 50.57
Min Limit: 45.00 Max Limit: 55.00
Min Pos: 1.18 in Max Pos: 3.00 in
0.49 nano-seconds Test: 50 Ohm Single
50.32 - PASS

Prop: 0.25 ns
Delta: 0.51 ns
Dist: 0.96 in

Name	Result	Avg	S/N	Job #	LYR	Time/Date	Min Z	Max Z	Std Dev	Oper
70 Ohm S...	Pass	69.05	3		2	10/09/12 15:41:17	67.76	74.78	1.71	
50 Ohm S...	Pass	50.32	3		3	10/09/12 15:41:17	50.19	50.57	0.08	
30 Ohm S...	Pass	31.85	3		4	10/09/12 15:41:17	31.78	31.99	0.06	
100 Ohm ...	Pass	109.06	4		1	10/09/12 15:43:16	107.92	109.56	0.40	
70 Ohm S...	Pass	67.60	4		2	10/09/12 15:43:16	66.85	68.24	0.37	
70 Ohm S...	Pass	69.62	4		2	10/09/12 15:43:16	67.53	74.26	2.49	
50 Ohm S...	Pass	50.46	4		3	10/09/12 15:43:16	50.26	50.84	0.12	
30 Ohm S...	Pass	31.89	4		4	10/09/12 15:43:16	31.81	32.06	0.07	

Test 4 of 5 - 50 Ohm Single : 3 : 50.000000 Ohms

Figure 1: The iCD Stackup Planner coupled to the Zmetrix TDR and Zscan software.

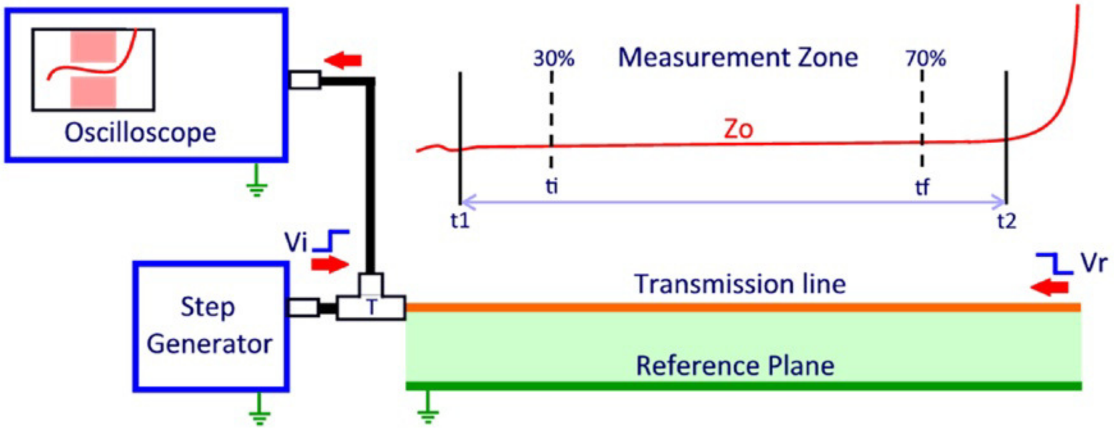


Figure 3: TDR measurement overview.

them in a factory environment yielding repeatable results. Hence, from a cost and practicality perspective, the TDR is the de facto standard impedance measurement instrument in the PCB fabrication industry.

A TDR applies a very fast pulse (< 100 ps) to an impedance test coupon via a controlled impedance cable and matching impedance probe (Figure 3). Whenever there is a change in impedance, part of the signal energy is reflected back to the TDR and is measured by the instrument. The magnitude of the reflected signal is related to the value of the discontinuity. Changes in the cross-sectional area of the trace, distance to the plane(s), and return path or proximity to other pads and traces will also cause a change in the impedance and cause a reflection. From this data, it is possible to graph the impedance and its variation over distance or time.

If a signal propagates from a region with impedance Z1, and enters a region with an impedance Z2, the incident waveform will reflect. The reflection coefficient—defined as the ratio of the reflected to the incident voltage—is related to the two impedances by the reflection coefficient :

$$\rho = \frac{Vreflected}{Vincident} = \frac{Z2 - Z1}{Z2 + Z1} \qquad \text{Equation 1}$$

By measuring the reflected signal and knowing the incident signal and the impedance of the source, the impedance of the transmission line can be extracted. When measured, in the time domain by a TDR, the incident waveform is a fast-rising step edge, and the impedance profile of the trace is measured as:

$$Zo = 50\Omega \frac{1 + \rho}{1 - \rho} \qquad \text{Equation 2}$$

When measured, in the frequency domain by a VNA, the incident waveform is a sine wave, and the reflected amplitude and phase is measured at each frequency value. The reflection coefficient, usually referred to as S-parameter (S_{11}), is related to the total, integrated overall impedance of the transmission line at each frequency by:

$$Zo = 50\Omega \frac{1 + S11}{1 - S11} \qquad \text{Equation 3}$$

The key attribute of a TDR to consider is the pulse rise time, as this determines the measured resolution. The faster the rising edge, the shorter the impedance discontinuity, which can be detected. If you are characterizing a connector or other very short type of interconnect, then a faster rise time will allow you to see anomalies that would be missed with a slower rise time. Most of the energy of the pulse will be in the first harmonic, and it is this frequency that is used to calculate the impedance. Fortunately, impedance does not vary much with frequency although insertion loss does.

Impedance test coupons are generally 150 mm long (see IPC standard IPC-2141A Design Guide for High-Speed Controlled Impedance

Circuit Boards), but by using a very fast rise time of 20 ps (20 GHz), as used in the Zmetrix ST808, traces can be tested down to 20 mm in length, allowing the operator to test actual on-board traces—not just test coupons. This is important as test coupons are normally placed outside the board outline on the panel edge, where the impedance is generally higher than those traces in the center due to an increase in resin and may not accurately represent board trace conditions.

Let's look at a couple of typical examples of impedance prediction and measurement.

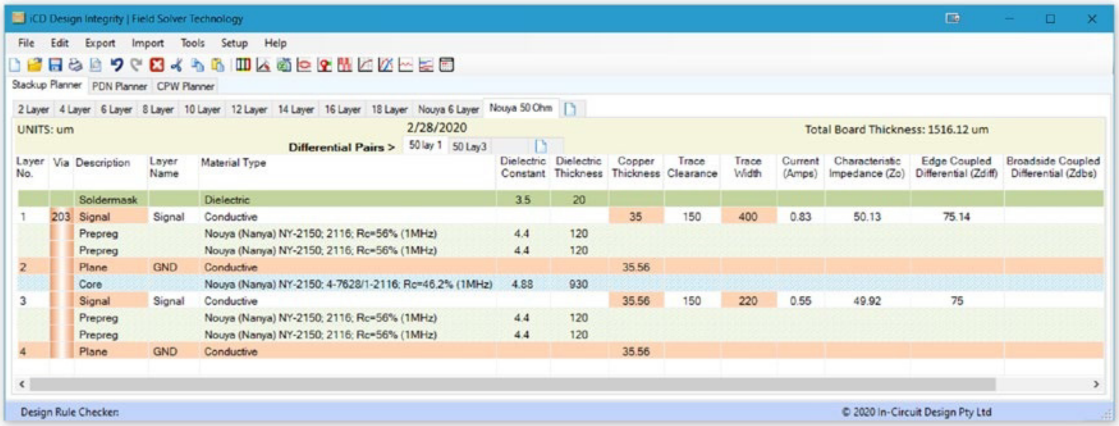
1. 50-ohm Single-ended Impedance

The iCD Stackup Planner was used to model a 50-ohm, single-ended impedance for both microstrip (Layer 1) and stripline (Layer 3) on the part stackup in Figure 4. The substrate used Nouya NY2150 dielectric materials.

The data from the iCD Stackup Planner was exported to the Zmetrix Zscan software (.zmx format). The results of the Zmetrix ST600 TDR (75 ps rise time, 7 GHz bandwidth) were then correlated to the iCD Stackup Planner impedance (Figure 5). The measurements of the 50-ohm impedance test coupons passed for all signal layers.

2. 100-ohm Differential Impedance

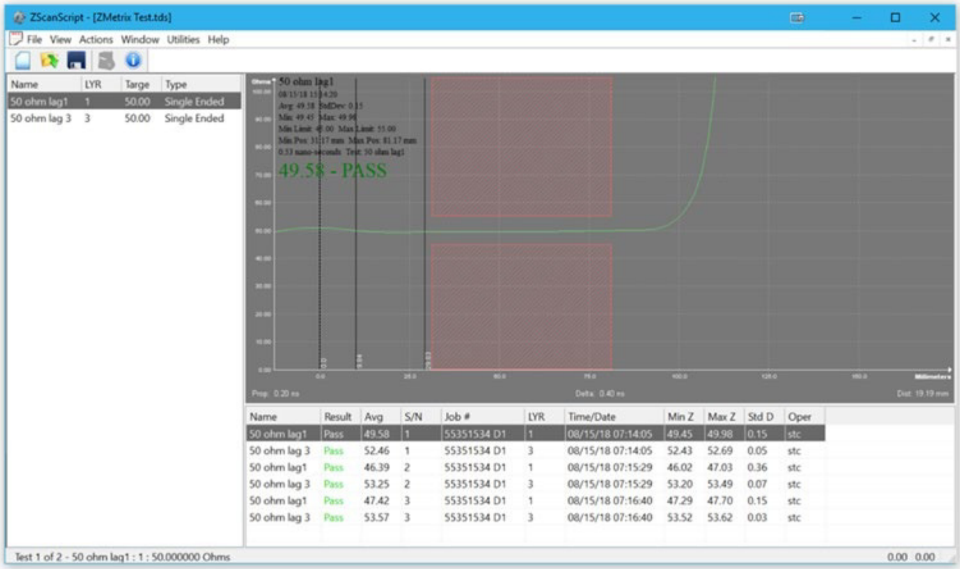
The iCD Stackup Planner was used to model a 100-ohm differential impedance for microstrip Layers 1 and 6 on the stackup in Figure 6.



UNITS: um
2/28/2020
Total Board Thickness: 1516.12 um

Layer No.	Via	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)
		Soldermask		Dielectric	3.5	20							
1	203	Signal	Signal	Conductive			35	150	400	0.83	50.13	75.14	
		Prepreg		Nouya (Nanya) NY-2150; 2116; Rc=56% (1MHz)	4.4	120							
		Prepreg		Nouya (Nanya) NY-2150; 2116; Rc=56% (1MHz)	4.4	120							
2		Plane	GND	Conductive			35.56						
		Core		Nouya (Nanya) NY-2150; 4-7628/1-2116; Rc=46.2% (1MHz)	4.88	930							
3		Signal	Signal	Conductive			35.56	150	220	0.55	49.92	75	
		Prepreg		Nouya (Nanya) NY-2150; 2116; Rc=56% (1MHz)	4.4	120							
		Prepreg		Nouya (Nanya) NY-2150; 2116; Rc=56% (1MHz)	4.4	120							
4		Plane	GND	Conductive			35.56						

Figure 4: 50-ohm microstrip and stripline impedance calculation (iCD Stackup Planner).

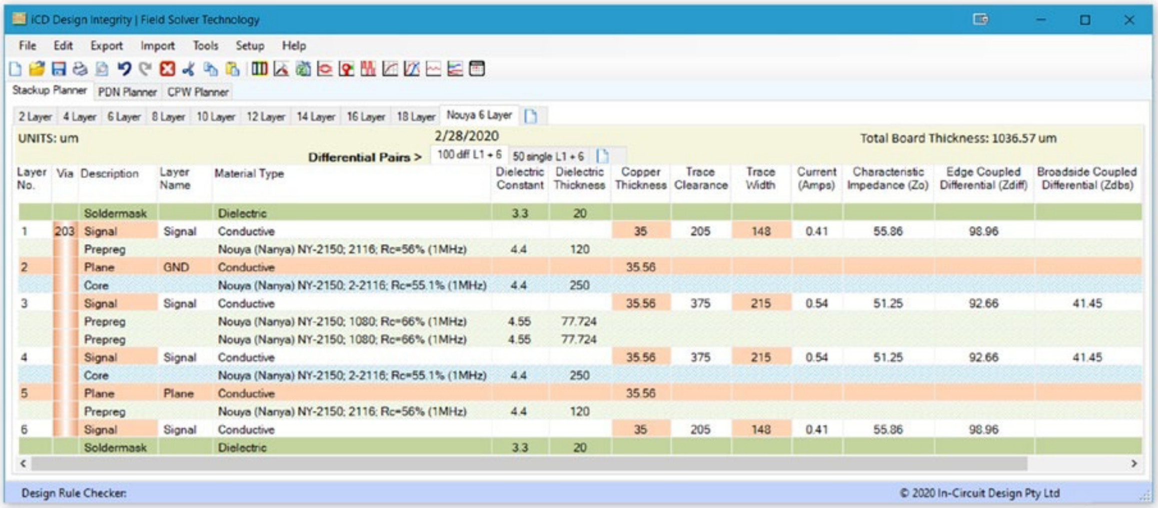


Name	LYR	Targe	Type
50 ohm lag1	1	50.00	Single Ended
50 ohm lag 3	3	50.00	Single Ended

Name	Result	Avg	S/N	Job #	LYR	Time/Date	Min Z	Max Z	Std D	Oper
50 ohm lag1	Pass	49.58	1	55351534 D1	1	08/15/18 07:14:05	49.45	49.98	0.15	stc
50 ohm lag 3	Pass	52.46	1	55351534 D1	3	08/15/18 07:14:05	52.43	52.69	0.05	stc
50 ohm lag1	Pass	46.39	2	55351534 D1	1	08/15/18 07:15:29	46.02	47.03	0.36	stc
50 ohm lag 3	Pass	53.25	2	55351534 D1	3	08/15/18 07:15:29	53.20	53.49	0.07	stc
50 ohm lag1	Pass	47.42	3	55351534 D1	1	08/15/18 07:16:40	47.29	47.70	0.15	stc
50 ohm lag 3	Pass	53.57	3	55351534 D1	3	08/15/18 07:16:40	53.52	53.62	0.03	stc

Test 1 of 2 - 50 ohm lag1 : 1 : 50.000000 Ohms
0.00 0.00

Figure 5: Pass/fail results for the 50-ohm traces (Zmetrix TDR and Zscan software).



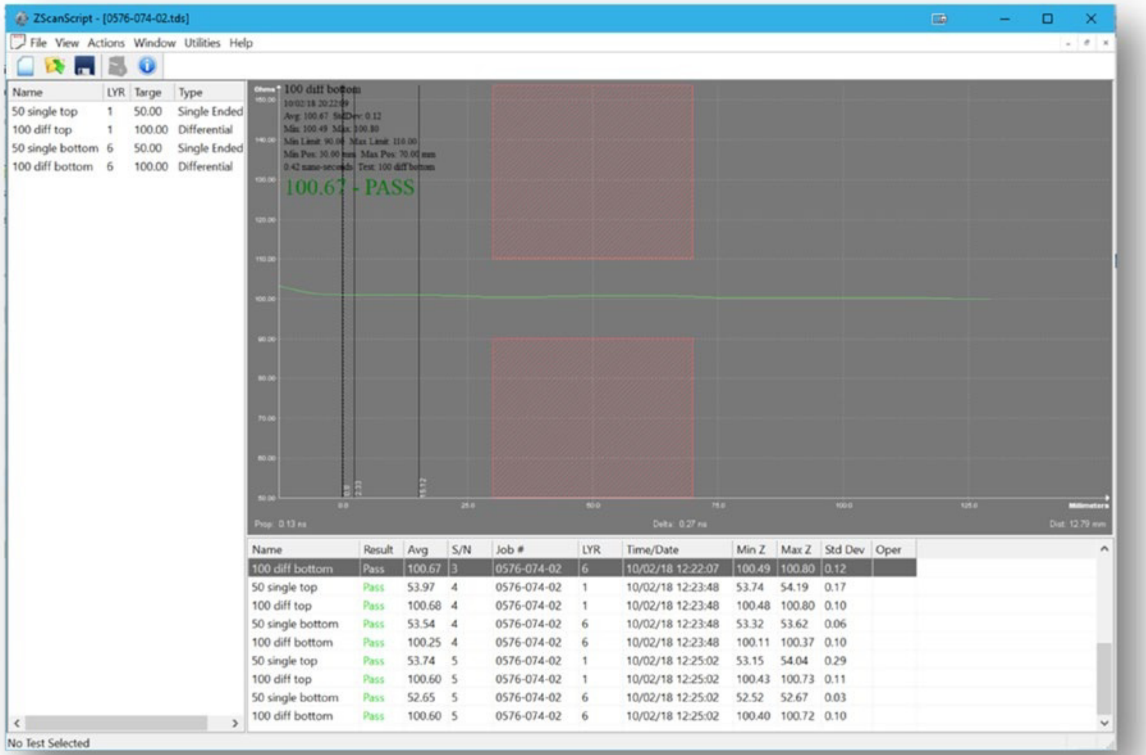
UNITS: um

2/28/2020

Total Board Thickness: 1036.57 um

Layer No.	Via	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)
		Soldermask		Dielectric	3.3	20							
1	203	Signal	Signal	Conductive			35	205	148	0.41	55.86	98.96	
		Prepreg		Nouya (Nanya) NY-2150; 2116; Rc=56% (1MHz)	4.4	120							
2		Plane	GND	Conductive			35.56						
		Core		Nouya (Nanya) NY-2150; 2-2116; Rc=55.1% (1MHz)	4.4	250							
3		Signal	Signal	Conductive			35.56	375	215	0.54	51.25	92.66	41.45
		Prepreg		Nouya (Nanya) NY-2150; 1080; Rc=66% (1MHz)	4.55	77.724							
		Prepreg		Nouya (Nanya) NY-2150; 1080; Rc=66% (1MHz)	4.55	77.724							
4		Signal	Signal	Conductive			35.56	375	215	0.54	51.25	92.66	41.45
		Core		Nouya (Nanya) NY-2150; 2-2116; Rc=55.1% (1MHz)	4.4	250							
5		Plane	Plane	Conductive			35.56						
		Prepreg		Nouya (Nanya) NY-2150; 2116; Rc=56% (1MHz)	4.4	120							
6		Signal	Signal	Conductive			35	205	148	0.41	55.86	98.96	
		Soldermask		Dielectric	3.3	20							

Figure 6: 100-ohm microstrip differential impedance calculation (iCD Stackup Planner).



Name	LYR	Targe	Type
50 single top	1	50.00	Single Ended
100 diff top	1	100.00	Differential
50 single bottom	6	50.00	Single Ended
100 diff bottom	6	100.00	Differential

Name	Result	Avg	S/N	Job #	LYR	Time/Date	Min Z	Max Z	Std Dev	Oper
100 diff bottom	Pass	100.67	3	0576-074-02	6	10/02/18 12:22:07	100.49	100.80	0.12	
50 single top	Pass	53.97	4	0576-074-02	1	10/02/18 12:23:48	53.74	54.19	0.17	
100 diff top	Pass	100.68	4	0576-074-02	1	10/02/18 12:23:48	100.48	100.80	0.10	
50 single bottom	Pass	53.54	4	0576-074-02	6	10/02/18 12:23:48	53.32	53.62	0.06	
100 diff bottom	Pass	100.25	4	0576-074-02	6	10/02/18 12:23:48	100.11	100.37	0.10	
50 single top	Pass	53.74	5	0576-074-02	1	10/02/18 12:25:02	53.15	54.04	0.29	
100 diff top	Pass	100.60	5	0576-074-02	1	10/02/18 12:25:02	100.43	100.73	0.11	
50 single bottom	Pass	52.65	5	0576-074-02	6	10/02/18 12:25:02	52.52	52.67	0.03	
100 diff bottom	Pass	100.60	5	0576-074-02	6	10/02/18 12:25:02	100.40	100.72	0.10	

Figure 7: Pass/fail results for the 100-ohm differential traces (Zmetrix TDR and Zscan software).

The TDR measurements of the 100-ohm differential impedance test coupons passed for both top and bottom microstrip signal layers (Figure 7).

Comparing the modeled impedance to the actual measured impedance, in this case, we get a 1.6-ohm variation for microstrip traces and a 2.5-ohm variation for stripline traces. The Zmetrix TDR's accuracy is within 1%, across the entire impedance range from 10 to 200 ohms. Keep in mind that there is also a multitude of fabrication variables to account for—hence a tolerance of ±10%, which is the IPC standard for controlled impedance measurement. And fabrication variables will be different for every process line. This is where an experienced fabricator can improve yields. Some fabrication shops offer a tolerance of

±5%, but that comes at a premium due to reduced yields.

Also, controlled impedance interconnects are intended to achieve target impedance when the transmission lines are loaded with ICs and powered. These conditions do not prevail on a bare board, so these measurements are likely to read higher than that predicted.

Fortunately, providing the impedance is in the ballpark, the most important factor from a PCB design perspective is the constant value of impedance along the transmission line—no discontinuities or reflections. However, impedance becomes more critical as frequency increases and wavelengths become close to trace lengths.

Key Points

- A TDR measures the impedance in the time domain. However, a far more accurate method is to use a VNA, which operates in the frequency domain.
- TDRs are the de facto standard, as VNAs are expensive, delicate instruments and not as robust.
- A TDR applies a very fast pulse to an impedance test coupon via a controlled impedance cable and matching impedance probe and measures the reflected signal and graphs the impedance.
- The key attribute of a TDR to consider is the pulse rise time, as this determines the measured resolution.
- Impedance test coupons are generally 150 mm long, but with a 20-ps pulse, traces can be tested down to 20 mm in length, allowing the operator to test actual on-board traces—not just test coupons.
- Test coupons are placed outside the board outline, which can make the impedance higher due to increased resin on the panel edge.
- There is also a multitude of fabrication variables to account for—hence a tolerance of ±10%, which is the IPC standard for controlled impedance measurement. **DESIGN007**

Further Reading

- B. Olney, "Beyond Design: Controlled Impedance Design," The PCB Design Magazine, May 2015.
- A. Bahl, "How TDR Impedance Measurements Work," November 28, 2017.
- Tektronix, "TDR Impedance Measurements: A Foundation for Signal Integrity," 2008.
- E. Bogatin, "TDR and VNA Techniques for PCB Characterization," IPC APEX EXPO 2002.

Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded at icd.com.au. To read past columns or contact Olney, click here.