Switchbacks in Tuned Routing

Beyond Design

by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

A switchback is a 180° bend in a road, rail, or path, especially one leading up the side of a mountain. I used to enjoy driving the Great Ocean Road (Figure 1), which is a National Heritage-listed 243-km stretch of windy road along the southeastern coast of Australia. The tight serpentine bends certainly delay your journey but also make it a more enjoyable trip.

Switchback also refers to a long trombone bend in a tuned serpentine trace. But rather than increase the delay of the signal, the switchback actually speeds it up due to the near (NEXT) and far-end (FEXT) crosstalk effects. In this month's column, I will look at why long, parallel switchbacks should be avoided.

Designing a memory interface is all about compared to the related clock or strobe signal in such a way that the data can be captured on both the rising and falling edge of the strobe, hence the term double data rate (DDR). However, the constant increase in data rate has made the timing margin associated with each rising and falling edge much tighter. To match the delay of critical signal timing, adjustments are required to the length of the individual signals within a group. This is accomplished by adding serpentine (accordion) bends in the traces to decrease the velocity of the signal to match the longest delayed signal. However, the opposite occurs—the velocity of the signal is sped up by the serpentine.

When an electromagnetic (EM) wave is a serpentine trace, with coupling between the bends, there is an increase in the speed of the signal. That is, the EM wave negotiates the serpentine section faster than that of a straight trace of the same length. This acceleration is caused by crosstalk coupling (NEXT and FEXT) between the parallel trace segments of the serpentine traces. The amount of acceleration is directly proportional to the coupling strength between the bends and to the rise time of the signal. For long, coupled lengths (those longer than the critical length), signals may become distorted as they pass the serpentine section.

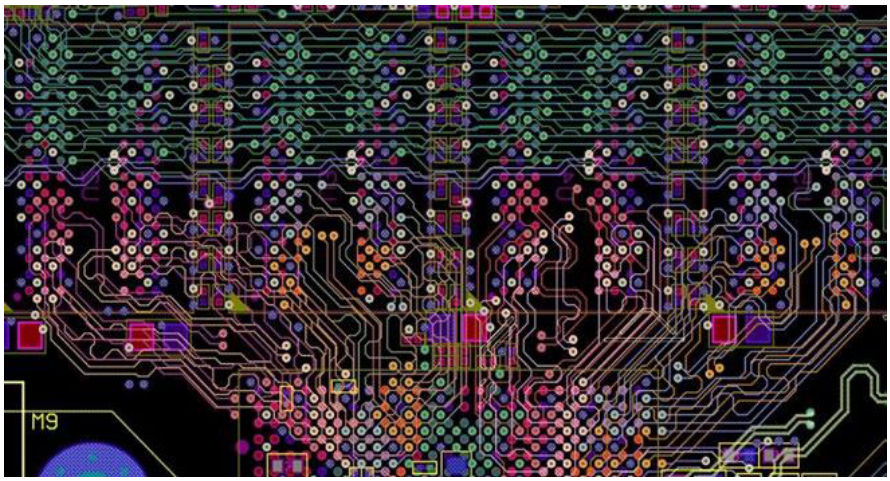

Figure 2: DDR4 fly-by routing.

Signals pass relatively undistorted along short, coupled serpentine sections, but distortion begins to occur when the parallel trombone length approaches one-third the signal wavelength. Figure 2 depicts a properly routed DDR4 fly-by design using short serpentines.

A tight design calls out explicit tolerances on signal timing. The timing requirements for DDR memory are outlined in the JEDEC standards and should be used as a metric for accuracy. The meandering traces must be compacted into an extremely tight space and so one is often tempted to use any method available to complete the design. The boundary between short and long coupled switchbacks is fuzzy. In general, when the round-trip delay of a heavily coupled switchback far exceeds one-third of the rise time, you get seriously distorted signals; when it's much less than one-third, you get advanced timing—and that's what we typically see. A 1 ns rise time used in an FR-4 dielectric limits the maximum useful coupled switchback length to about 1 inch (2 inches, round trip). A 100 ps rise time limits the maximum coupled switchback length to about 100 mil.

In an outer layer microstrip configuration, the mutual capacitive coupling between adjacent traces is generally weaker than the mutually inductive coupling, driving the FEXT coefficient negative. However, forward crosstalk does not exist in the stripline configuration. The fine balance between inductive and capacitive coupled crosstalk produces almost no observable forward crosstalk. Also, the peak amplitude of the crosstalk is considerably reduced. So, all other factors being equal, here is just another good reason why one should always route high-speed signals on the inner layers of a multilayer PCB. Stripline edge-coupled signals can also be placed closer to each other as compared to the microstrip equivalent, which leaves more space for routing and is always welcomed.

When selecting a serpentine routing method, one should avoid long, coupled switchbacks as highlighted in violet in Figure 3. This was taken from a DRR4 reference design that I came across recently. Don't try this at home! The dark blue highlighted serpentine has an ideal configuration.

Figure 4 plots the comparison of a straight trace vs. a serpentine trace routed on the outer microstrip layer. Green is the driver; red is the straight (reference) trace; and blue is the serpentine trace with short, coupled segments. As can clearly be seen, the blue serpentine trace leads the red reference trace by 15 ps despite being the same length. As the trombone parallel sections increase, so does the velocity of the signal. The dip in the blue serpentine trace (around 5 ns) is the forward crosstalk which would not be present on an inner stripline layer.

If the switchback delay is much less than the signal rise time, the NEXT distortion blends into the overall shape of the rising edge. The NEXT distortion for short switchbacks doesn't impact the shape of the rising edge, but it advances the time of arrival. That is, short, coupled switchbacks produce smaller delays than the total trace length would indicate. Long, coupled switchbacks also distort the signals and are not recommended. The key is to route the clock and strobes first as straight as pos-

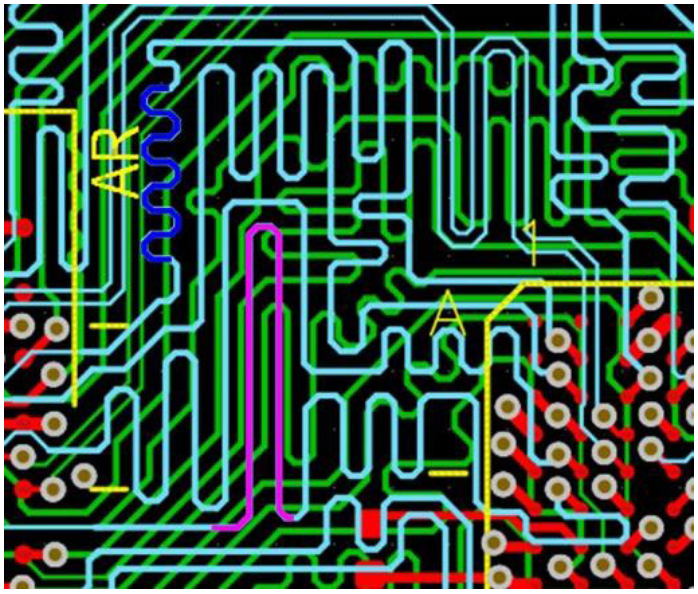

Figure 3: Another poor DDR4 reference design with long switchbacks.

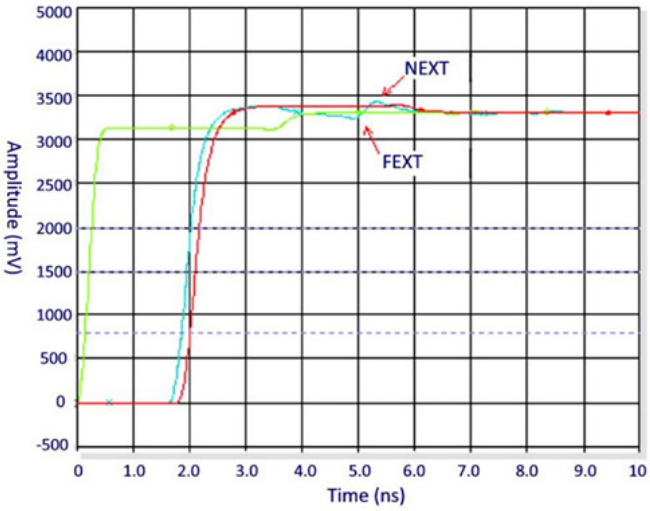

Figure 4: Serpentine trace vs. straight trace (microstrip).

sible, then tune the delay of each signal group to its reference clock. This will ensure that the signals have settled before the data is captured.

Key Points

- Designing a memory interface is all about timing closure
- The velocity of the signal is sped up by the serpentine. The EM wave passes the serpentine section faster than that of a straight trace of the same length
- This acceleration is caused by crosstalk coupling (NEXT and FEXT) between the parallel trace segments of the serpentine traces
- For long coupled lengths, signals may become distorted as they pass the serpentine section
- Signals pass relatively undistorted along short, coupled serpentine sections but distortion begins to occur when the parallel trombone length approaches one-third the signal wavelength
- When the round-trip delay of a heavily coupled switchback far exceeds one-third of the rise time, you get seriously distorted signals; when it's much less than one-third, you get advanced timing
- Forward crosstalk does not exist in the stripline configuration
- Stripline edge coupled signals can also be placed closer to each other compared to the microstrip equivalent
- The NEXT distortion for short switchbacks doesn't impact the shape of the rising edge, but it advances the time of arrival
- Long, coupled switchbacks also distort the signals and are not recommended

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Resources

1. "Beyond Design: Stackup Configurations to Mitigate Crosstalk," Barry Olney, *Design007 Magazine*, February 2021.

"Serpentine Delays," by Howard Johnson, Signal Consulting Inc. Originally published in EDN Magazine, Feb. 5, 2001.

Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded at www.icd.com.au. To read past columns or contact Olney, click here.

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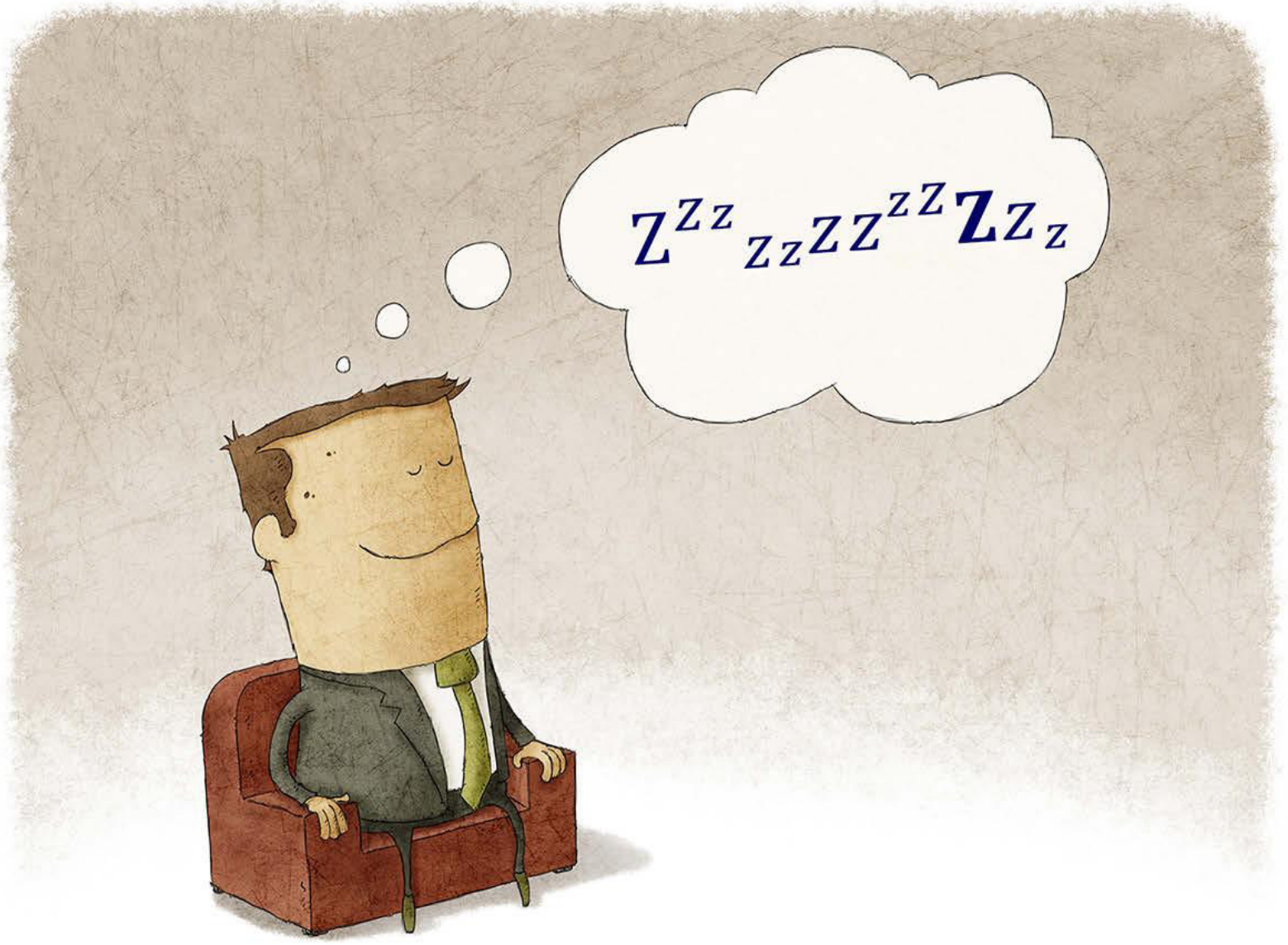

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