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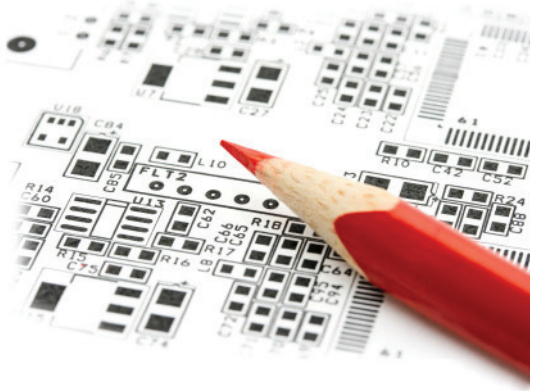


Stackup Planning and the Fabrication Process

by Barry Olney
IN-CIRCUIT DESIGN PTY LTD | AUSTRALIA

SUMMARY: Before starting a PCB design, we need to plan the PCB stackup for optimized performance, ensure that the selected substrate materials are available and clearly document the stackup so that it can be fabricated to engineering specifications.

Back in 1987, when I first started working on high-speed designs, the PCB stackup did not seem that important. If a board would not route, I simply added another couple of signal layers—problem solved. But that was running at a maximum frequency of 166 MHz, which at the time seemed fast.

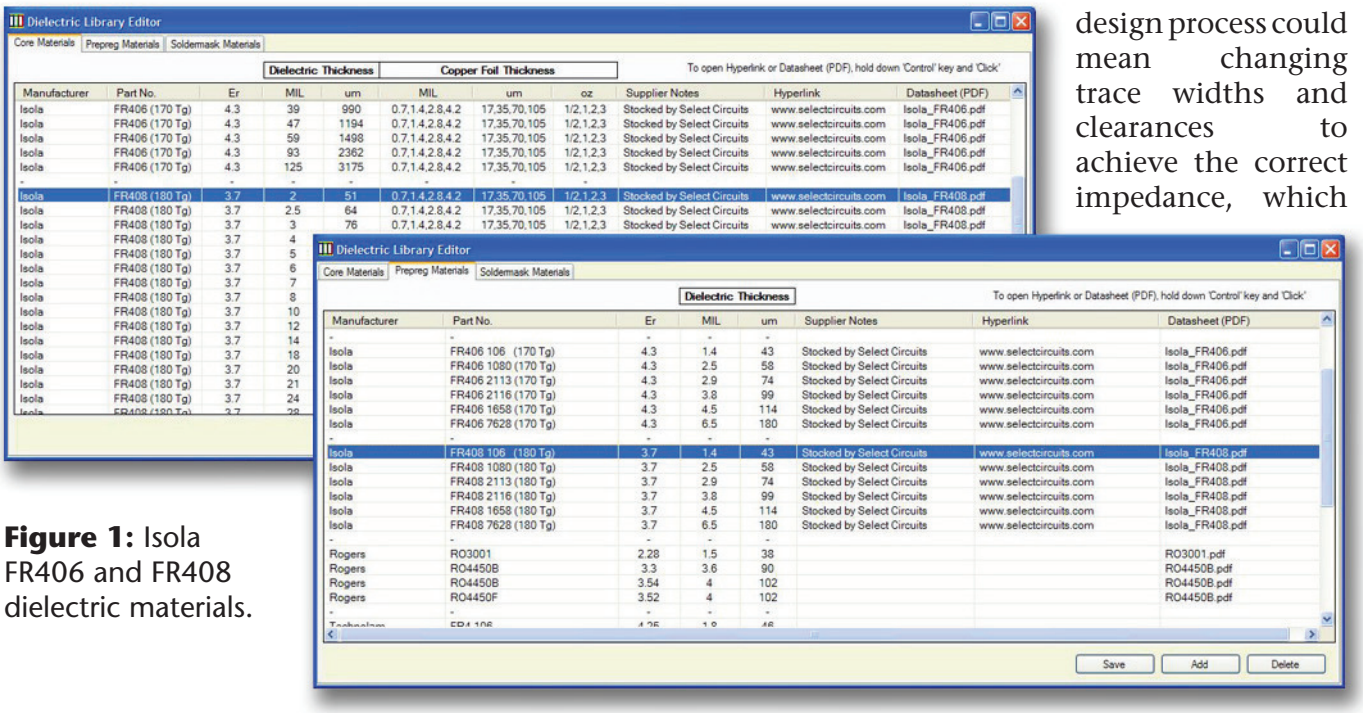
Times have changed. Now, multi GB/s designs are becoming the "norm" and the stackup configuration, characteristic and differential impedance control are crucial to the performance and reliability of the product.

Rick Almeida of Downstream Technologies, Inc. pointed out in his article, "What to Look Forward to in 2012" (*The PCB Magazine,* January 2012) that "The growing importance of stackup design and analysis will be recognized. Today, there is a growing need to plan and design the stackup properly, as well as optimize it for better overall performance and communicate and document stackup information between engineering and fabrication."

I have previously written on the topic as well, but perhaps some designers are not quite at this level, yet. Therefore, let's look at some basic stackup configurations and briefly cover what is required for the fabrication process.

Dielectric Materials

Before starting a PCB design, we need to plan the PCB stackup and ensure that the selected substrate materials are available from our chosen fabrication—a step that is regularly missed. Changing the stackup towards the end of the design process could mean changing trace widths and clearances to achieve the correct impedance, which



Dielectric Library Editor

Core Materials | Prepreg Materials | Soldermask Materials

Dielectric Thickness | Copper Foil Thickness | To open Hyperlink or Datasheet (PDF), hold down 'Control' key and 'Click'

Manufacturer	Part No.	Er	MIL	um	MIL	um	oz	Supplier Notes	Hyperlink	Datasheet (PDF)
Isola	FR406 (170 Tg)	4.3	39	990	0.7,1.4,2.8,4.2	17,35,70,105	1/2,1,2,3	Stocked by Select Circuits	www.selectcircuits.com	Isola_FR406.pdf
Isola	FR406 (170 Tg)	4.3	47	1194	0.7,1.4,2.8,4.2	17,35,70,105	1/2,1,2,3	Stocked by Select Circuits	www.selectcircuits.com	Isola_FR406.pdf
Isola	FR406 (170 Tg)	4.3	59	1498	0.7,1.4,2.8,4.2	17,35,70,105	1/2,1,2,3	Stocked by Select Circuits	www.selectcircuits.com	Isola_FR406.pdf
Isola	FR406 (170 Tg)	4.3	93	2362	0.7,1.4,2.8,4.2	17,35,70,105	1/2,1,2,3	Stocked by Select Circuits	www.selectcircuits.com	Isola_FR406.pdf
Isola	FR406 (170 Tg)	4.3	125	3175	0.7,1.4,2.8,4.2	17,35,70,105	1/2,1,2,3	Stocked by Select Circuits	www.selectcircuits.com	Isola_FR406.pdf
-	-	-	-	-	-	-	-			
Isola	FR408 (180 Tg)	3.7	2	51	0.7,1.4,2.8,4.2	17,35,70,105	1/2,1,2,3	Stocked by Select Circuits	www.selectcircuits.com	Isola_FR408.pdf
Isola	FR408 (180 Tg)	3.7	2.5	64	0.7,1.4,2.8,4.2	17,35,70,105	1/2,1,2,3	Stocked by Select Circuits	www.selectcircuits.com	Isola_FR408.pdf
Isola	FR408 (180 Tg)	3.7	3	76	0.7,1.4,2.8,4.2	17,35,70,105	1/2,1,2,3	Stocked by Select Circuits	www.selectcircuits.com	Isola_FR408.pdf
Isola	FR408 (180 Tg)	3.7	4							
Isola	FR408 (180 Tg)	3.7	5							
Isola	FR408 (180 Tg)	3.7	6							
Isola	FR408 (180 Tg)	3.7	7							
Isola	FR408 (180 Tg)	3.7	8							
Isola	FR408 (180 Tg)	3.7	10							
Isola	FR408 (180 Tg)	3.7	12							
Isola	FR408 (180 Tg)	3.7	14							
Isola	FR408 (180 Tg)	3.7	18							
Isola	FR408 (180 Tg)	3.7	20							
Isola	FR408 (180 Tg)	3.7	21							
Isola	FR408 (180 Tg)	3.7	24							

Dielectric Library Editor

Core Materials | Prepreg Materials | Soldermask Materials

Dielectric Thickness | To open Hyperlink or Datasheet (PDF), hold down 'Control' key and 'Click'

Manufacturer	Part No.	Er	MIL	um	Supplier Notes	Hyperlink	Datasheet (PDF)
-	-	-	-	-			
Isola	FR406 106 (170 Tg)	4.3	1.4	43	Stocked by Select Circuits	www.selectcircuits.com	Isola_FR406.pdf
Isola	FR406 1080 (170 Tg)	4.3	2.5	58	Stocked by Select Circuits	www.selectcircuits.com	Isola_FR406.pdf
Isola	FR406 2113 (170 Tg)	4.3	2.9	74	Stocked by Select Circuits	www.selectcircuits.com	Isola_FR406.pdf
Isola	FR406 2116 (170 Tg)	4.3	3.8	99	Stocked by Select Circuits	www.selectcircuits.com	Isola_FR406.pdf
Isola	FR406 1658 (170 Tg)	4.3	4.5	114	Stocked by Select Circuits	www.selectcircuits.com	Isola_FR406.pdf
Isola	FR406 7628 (170 Tg)	4.3	6.5	180	Stocked by Select Circuits	www.selectcircuits.com	Isola_FR406.pdf
-	-	-	-	-			
Isola	FR408 106 (180 Tg)	3.7	1.4	43	Stocked by Select Circuits	www.selectcircuits.com	Isola_FR408.pdf
Isola	FR408 1080 (180 Tg)	3.7	2.5	58	Stocked by Select Circuits	www.selectcircuits.com	Isola_FR408.pdf
Isola	FR408 2113 (180 Tg)	3.7	2.9	74	Stocked by Select Circuits	www.selectcircuits.com	Isola_FR408.pdf
Isola	FR408 2116 (180 Tg)	3.7	3.8	99	Stocked by Select Circuits	www.selectcircuits.com	Isola_FR408.pdf
Isola	FR408 1658 (180 Tg)	3.7	4.5	114	Stocked by Select Circuits	www.selectcircuits.com	Isola_FR408.pdf
Isola	FR408 7628 (180 Tg)	3.7	6.5	180	Stocked by Select Circuits	www.selectcircuits.com	Isola_FR408.pdf
-	-	-	-	-			
Rogers	RO3001	2.28	1.5	38			RO3001.pdf
Rogers	RO4450B	3.3	3.6	90			RO4450B.pdf
Rogers	RO4450B	3.54	4	102			RO4450B.pdf
Rogers	RO4450F	3.52	4	102			RO4450B.pdf
-	-	-	-	-			

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Figure 1: Isola FR406 and FR408 dielectric materials.

FR406/8 Materials	Final Thickness	Combined Prepreg Materials = Total Thickness
106	1.4	106 + 106 = 2.8 mil
1080	2.5	1080 + 1080 = 5 mil
2113	2.9	2113 + 2116 = 6.7 mil
2116	3.8	2113 + 2116 + 1080 = 9.2 mil
1658	4.5	2 x 2116 + 1658 + 7628 = 18.6 mil etc.
7628	6.5	*There are many combinations to achieve the desired thickness.*

Table 1.

could create a lot of unnecessary work.

If we use the same materials that the fab shop stocks to build our stackup, then the impedance will be more accurate. If we just choose a convenient number, for core thickness, for example, then this may be up to 3% different off from what is available; hence, the impedance will vary by 3%.

The most widely used dielectric material is FR-4 and may be in the form of core or prepreg (pre-impregnated) material. Isola's top selling materials are FR406 and FR408. While FR406 sets the industry standard for basic multilayer PCB fabrication, FR408 is a high-performance FR-4 epoxy dielectric for improved signal performance. Its low dielectric constant and low dissipation factor make it an ideal candidate for broadband circuit designs requiring fast signal speeds or improved signal integrity. Also, the high glass transition temperature makes it compatible with ROHS compliant components and most FR-4 processes. Figure 1 illustrates the available core materials in the default Dielectric Library Editor of the ICD Stackup Planner (download from www.icd.com.au).

The core material is a thin dielectric (cured fibreglass epoxy resin) with copper foil bonded to both sides. For instance: Isola's FR406/8 materials include 2, 2.5, 3, 4, 5, 6, 7, 8, 10, 12, 14, 18, 20, 21, 28, 31, 36, 39, 47, 59, 93 and 125 mil cores. The copper thickness is typically ½ to 2 oz (17 to 70 um). If you look at the datasheets from Isola (or any other manufacturer) these sizes are not very clear, so it is best to contact your fab shop for the details of the materials they stock.

The prepreg material is a thin sheet of fibreglass impregnated with uncured epoxy resin which hardens when heated and pressed during the PCB fabrication process. Isola's FR406/8 materials include 1.4, 2.5, 2.9, 3.8, 4.5, and 6.5 mil prepregs that may be combined to achieve the desired prepreg thickness. These are the final thicknesses after processing (Table 1).

The most common stackup, known as the Foil Method, is to have prepreg with copper foils bonded to the outside on the outermost layers (top and bottom), then core alternating with prepreg throughout the substrate. An alternate stackup is called the Capped Method, which is the opposite of the Foil Method and was used by old-school military contractors, but may still be fabricated today.

The total substrate thickness is generally 62 mils (1.6 mm) but may vary according to the application: 20, 31, 40, 47, 62, 93 and 125 mils are other not-so-typical thicknesses. Obviously, as the layer count increases the total board thickness increases. Twelve layers is the limit for 62 mil substrates.

The configuration of the PCB stackup depends on many factors, but whatever the requirements, one should ensure that the following rules are followed in order to avoid a possible debacle:

- All signal layers should be adjacent to and closely coupled to a reference plane, creating a clear return path and eliminating broadside crosstalk
- There is good interplane capacitance to reduce inductance at high frequencies

UNITS: MIL — ICD STACKUP PLANNER – www.icd.com.au 2/27/2012 — Total Board Thickness: 59.2

Differential Pairs > Diff Pair

Layer Number	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Impedance Characteristic(Zo)	Edge Coupled Differential(Zdiff)	Broadside Coupled Differential(Zdbs)	Description
		Dielectric	3.3	0.5								Soldermask
1	Top	Conductive			0.7	20	12	0.42	54.82	101.71		Signal
		Dielectric	4.3	8								Prepreg
2	GND	Conductive			1.4							Plane
		Dielectric	4.3	39								Core
3	VCC	Conductive			1.4							Plane
		Dielectric	4.3	8								Prepreg
4	Bottom	Conductive			0.7	20	12	0.42	54.82	101.71		Signal
		Dielectric	3.3	0.5								Soldermask

Figure 2: Four-layer board.

UNITS: MIL — ICD STACKUP PLANNER – www.icd.com.au 3/1/2012 — Total Board Thickness: 58.4

Differential Pairs > Diff pair New Pair

Layer Number	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Impedance Characteristic(Zo)	Edge Coupled Differential(Zdiff)	Broadside Coupled Differential(Zdbs)	Description
		Liquid Photo Imageable	3.3	0.5								Soldermask
1	Top	Conductive			0.7	20	12	0.42	55.74	103.99		Signal
		FR408 2116 (180 Tg)	3.7	3.8								Prepreg
		FR408 2116 (180 Tg)	3.7	3.8								Prepreg
2	GND	Conductive			1.4							Plane
		FR408 (180 Tg)	3.7	39								Core
3	VCC	Conductive			1.4							Plane
		FR408 2116 (180 Tg)	3.7	3.8								Prepreg
		FR408 2116 (180 Tg)	3.7	3.8								Prepreg
4	Bottom	Conductive			0.7	20	12	0.42	55.74	103.99		Signal
		Liquid Photo Imageable	3.3	0.5								Soldermask

Figure 3: Four-layer board with dielectric materials.

- High-speed signals should be routed between the planes to reduce radiation
- The substrate should be symmetrical with an even number of layers, which prevents the PCB from warping during manufacture and reflow
- The stackup should accommodate a number of different technologies
- Cost (the boss's most important design parameter) should also be addressed

It is not always possible to configure the stackup to have both tight coupling of the planes and tight coupling of the signal layers to the planes, as this depends on the number of layers and the available materials. Four- and six-layer boards typically have this issue. Fortunately, the lower layer count boards are generally used for designs below 100MHz so the interplane capacitance may not be as important at these frequencies.

In the four-layer board (Figure 2) the signal layers are < 10 mils from the plane, which helps reduce crosstalk, and the single-ended (Z_o) and differential impedances (Zdiff) are 54 and 101, respectively. A good range of impedance (Z_o) is from 50 to 60 ohms. Keep in mind that lower impedance will increase the dI/dt and dramatically increase the current drawn (not good for the PDN); higher impedance will emit more EMI and also make the design more susceptible to outside interference.

In order to communicate our intent to the PCB fab shop, we need to produce documentation detailing the required materials. In Figure 3, the centre core of 39 mils thickness has been replaced by a core from the Dielectric Materials Library which fortunately is also 39 mils thick. Also, in order to get a total of 8 mils thickness of prepreg between layers 1 and 2, as well as between layers 3 and 4, two sheets of FR408 2116 material are used, each totaling 7.6 mils. As mentioned, we cannot always get the exact value and this is where the inaccuracy occurs. The impedance Z_o drops by 1.6 ohms (2.8%) and Zdiff by 2.4 ohms (2.3%). And, the total board thickness reduces.

The six-layer board in Figure 4 again has close coupling between the signal layers and the planes—reducing crosstalk. The bulk of the board thickness is again made up of the centre core material. Broadside coupling between signal layers is reduced by keeping signal layers 3 and 4 far apart, and close to the reference planes. Ideally, these signal layers should be routed diagonally (or at 45 degrees) to each other to minimize the coupling. Routing pairs should be layers 1 and 3 (GND reference) and

UNITS: MIL — ICD STACKUP PLANNER – www.icd.com.au 3/8/2012 — Total Board Thickness: 62

Differential Pairs > Diff Pair

Layer Number	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Impedance Characteristic(Zo)	Edge Coupled Differential(Zdiff)	Broadside Coupled Differential(Zdbs)	Description
		Dielectric	3.3	0.5								Soldermask
1	Top	Conductive			0.7	12	6	0.25	53.52	101.04		Signal
		Dielectric	4.3	4								Core
2	GND	Conductive			1.4							Plane
		Dielectric	4.3	6								Prepreg
3	Inner 3	Conductive			1.4	12	6	0.42	53.33	100.28		Signal
		Dielectric	4.3	35								Core
4	Inner 4	Conductive			1.4	12	6	0.42	53.33	100.28		Signal
		Dielectric	4.3	6								Prepreg
5	VCC	Conductive			1.4							Plane
		Dielectric	4.3	4								Core
6	Bottom	Conductive			0.7	12	6	0.25	53.52	101.04		Signal
		Dielectric	3.3	0.5								Soldermask

Figure 4: Six-layer board.

UNITS: MIL — ICD STACKUP PLANNER – www.icd.com.au 3/8/2012 — Total Board Thickness: 62.6

Differential Pairs > Diff Pair

Layer Number	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Impedance Characteristic(Zo)	Edge Coupled Differential(Zdiff)	Broadside Coupled Differential(Zdbs)	Description
		Liquid Photo Imageable	3.3	0.5								Soldermask
1	Top	Conductive			0.7	12	6	0.25	53.52	101.04		Signal
		FR406 (170 Tg)	4.3	4								Core
2	GND	Conductive			1.4							Plane
		FR406 2113 (170 Tg)	4.3	2.9								Prepreg
		FR406 2113 (170 Tg)	4.3	2.9								Prepreg
3	Inner 3	Conductive			1.4	12	6	0.42	52.95	99.7		Signal
		FR406 (170 Tg)	4.3	36								Core
4	Inner 4	Conductive			1.4	12	6	0.42	52.95	99.7		Signal
		FR406 2113 (170 Tg)	4.3	2.9								Prepreg
		FR406 2113 (170 Tg)	4.3	2.9								Prepreg
5	VCC	Conductive			1.4							Plane
		FR406 (170 Tg)	4.3	4								Core
6	Bottom	Conductive			0.7	12	6	0.25	53.52	101.04		Signal
		Liquid Photo Imageable	3.3	0.5								Soldermask

Figure 5: Six-layer board with dielectric materials.

4 and 6 (VCC reference). High-speed signals should be routed on the stripline layers 3 and 4 to reduce EMI.

Figure 5 illustrates the completed stackup with all the dielectric materials defined, ready for pasting into the PCB specification and sent off with the Gerber and NC Drill data to the fab shop for manufacture.

Please see my previous article "The Perfect Stackup for High-speed Design" for information on additional stackups.

Points to remember:

- Control impedance to ensure performance and reliability of the product
- Keep the signal layers close to the planes to reduce crosstalk
- Avoid broadside coupling by separating the internal signal layers with bulk core material
- Combine prepreg and core materials from the datasheets, in the stackup, in place of the defaults to improve accuracy
- Ensure that the selected substrate materials are available from your chosen fab shop **PCB**

References:

1. "What to Look Forward to in 2012" by Rick Almeida, The PCB Magazine January 2012

2. Electromagnetic Compatibility Engineering—Henry Ott

3. "The Perfect Stackup for High-speed Design", by Barry Olney, The PCB Magazine November 2011

4. The ICD Stackup Planner and ICD PDN Planner can be downloaded from www.icd.com.au

Barry Olney is Managing Director of In-Circuit Design Pty Ltd. (ICD), Australia, a PCB Design Service Bureau and Board Level Simulation Specialist. Among others through the years, ICD was awarded "Top 2005 Asian Distributor Marketing and "Top 2005 Worldwide Distributor Marketing by Mentor Graphics, Board System Division. For more information, contact Barry Olney at +61 4123 14441 or email at b.olney@icd.com.au.