Beyond Design – Stackup Planning Part 5

by Barry Olney | In-Circuit Design Pty Ltd | Australia

Design methodologies change over time, particularly in the ways to simulate electromagnetic fields and return current paths. In my previous series of columns, on stackup planning, I described the traditional stackup structures which use a combination of signal and power/ground planes. But to achieve the next level in stackup design, one needs to not only consider the placement of signal and plane layers, in the stackup, but to visualize the electromagnetic fields that propagate the signals through the substrate.

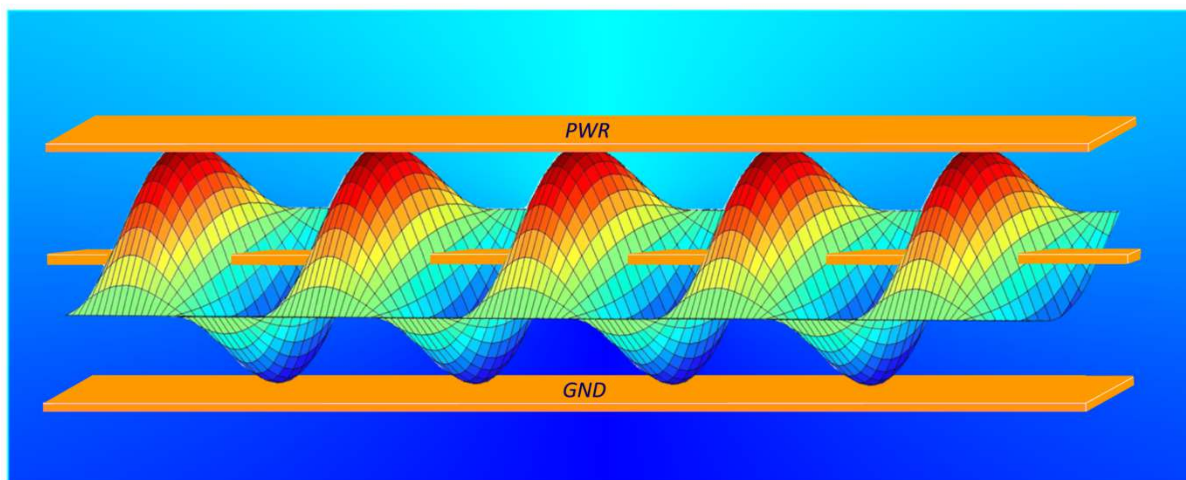

Figure 1–Digital signals travel as a wave of electromagnetic energy in a multilayer PCB

The previous four part Stackup Planning series of columns were published in The PCB Design Magazine in 2015 and included:

In Part 1, I looked at how the stackup is built, the materials used in construction and the lamination process. And, I set out some basic rules to follow for high-speed design. It is important keep return paths, crosstalk and EMI in mind during the design process.

Part 2 follows on from this with definitions of basic stackups starting with four and six layers. Of course, this methodology can be used for higher layer count boards–36, 72 layers and beyond. The virtual materials were replaced with items stocked by the PCB fabricator.

Part 3 looks at higher layer count stackups as the four and six layer configurations are not the best choice for high-speed design. In particular, each signal layer should be adjacent to, and closely coupled to, an uninterrupted reference plane, which creates a clear return path and eliminates broadside crosstalk. As the layer count increases, these rules become easier to implement but decisions regarding return current paths become more challenging. More rules for HSD and EMI were also defined.

In Part 4, I elaborated on 10 plus layer counts. The methodology I set out, in previous columns, can be used to construct higher layer count boards. In general, these boards contain more planes and therefore the issues associated with split power planes can usually be avoided. Also, ten plus layers require very thin dielectrics, in order to reduce the total board thickness. This naturally provides tight coupling between adjacent signal and plane layers reducing crosstalk and electromagnetic emissions. Additional rules for high-speed design were defined. The number one question—determining the required layer count, was also addressed.

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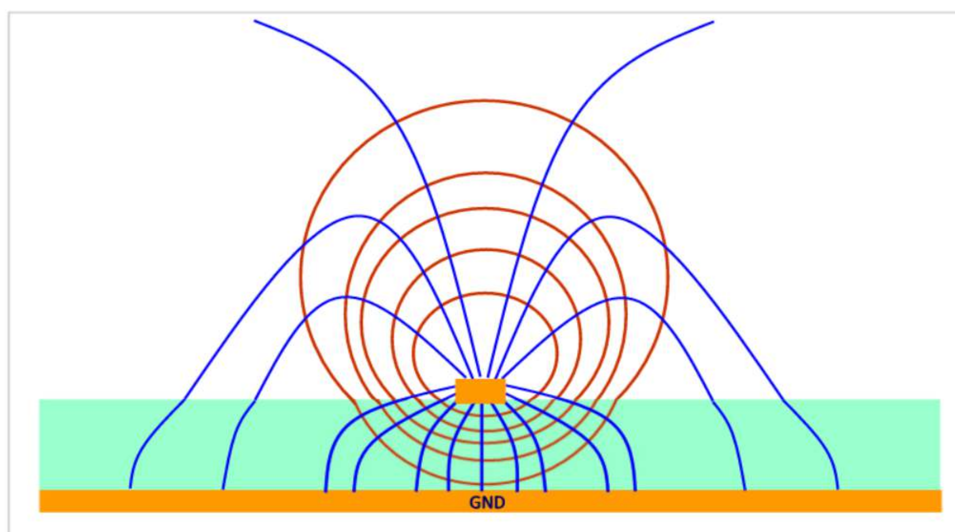

Figure 2–Microstrip Electric (blue) Magnetic (red) Fields

In this month's column, I will add to my previous four part Stackup Planning series, outlined above, with this final chapter (Part 5) covering all the latest concepts in stackup design.

The speed of a digital signal does not depend intrinsically on the speed of electrons, but rather on the speed of energy transfer between electronic components. The actual velocity of electrons through a conductor is very slow (~10mm per second), however the 'knock on' effect is very fast as it follows the electromagnetic field. The energy propagates, between the signal trace and the return path(s), as an electromagnetic wave as in Figure 1. And, the speed of this wave varies depending on the layer, in the multilayer substrate, and the surrounding dielectric materials. For instance, the wave will travel at approximately half the speed of light in a typical FR-4 material with a dielectric constant (Dk) of 4.

The electromagnetic fields of a microstrip (outer) layer are shown in Figure 2. The fields tend to radiate outward, as there is only one solid plane beneath, which blocks the emissions. So it is obvious that, this configuration is not recommended for routing high-speed single ended signals. The electromagnetic fields surrounding the microstrip exist partially within the dielectric material(s) and partially within the surrounding air. Since air has a dielectric constant of one, which is always lower than that of FR-4 (typically 4), mixing a little air into the equation will speed up the signal propagation. You can see this in the kinks in the field lines as they travel into the air region from the dielectric material. Adding a solder mask (Dk=3) will put another kink in the fields.

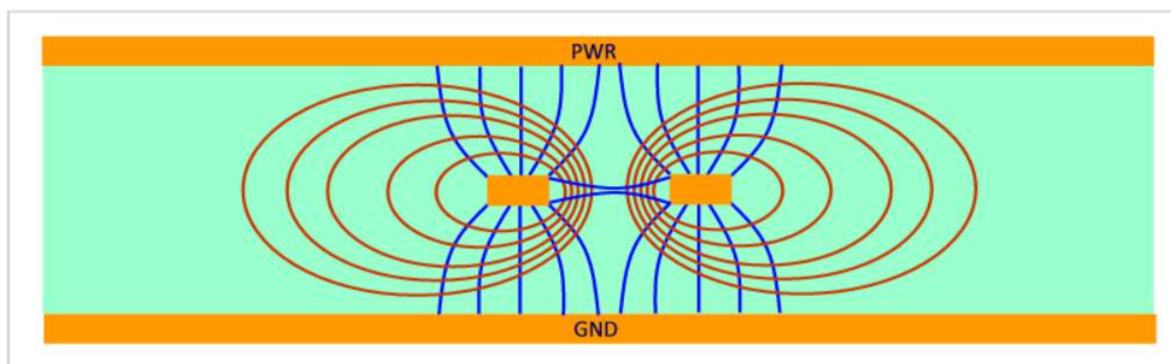

Figure 3–Stripline configuration–differential pair

A stripline is any trace sandwiched between reference planes on both sides as in Figure 3. The electric fields (blue) of a stripline are totally contained between the two solid planes whereas; the magnetic fields (red) are also limited vertically by the planes. Radiation is reduced dramatically and is limited to just the edge fringing fields due to the shielding affects of the planes. Signals that travel in the same dielectric material will couple. This may be good for a differential pair, but is not desirable for non-related signals as part of the aggressor signal will couple to the victim depending on the separation of traces.

Figure 4, illustrates a dual stripline configuration with a combination for edge and broadside coupling. This occurs when two signal layers are stacked between the planes. Again, this may create crosstalk depending on the trace separation. Crosstalk can be reduced by routing the signal traces orthogonally on adjacent layers reducing the couple to just a small area. However, as frequencies and rise times increase this is not a good solution.

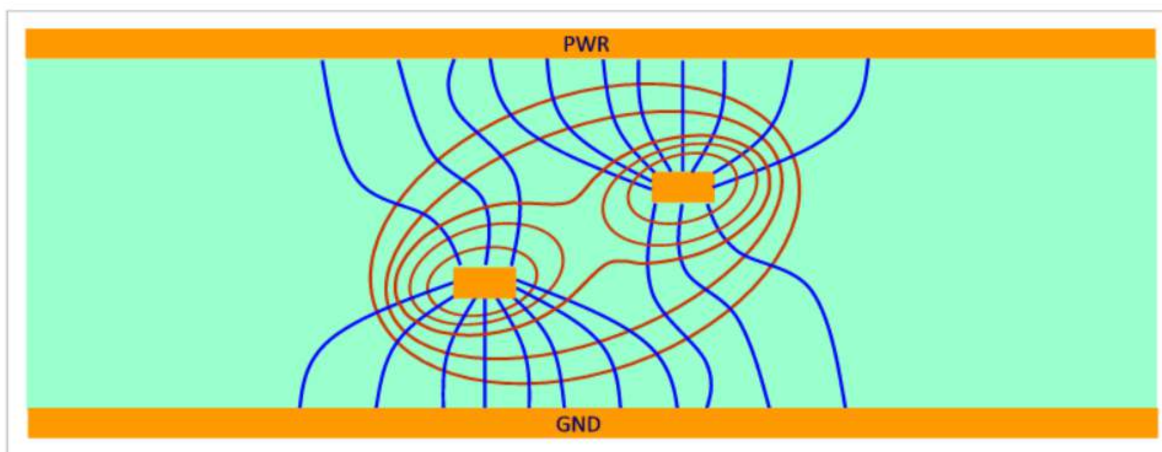

Figure 4–Dual stripline configuration–edge and broadside coupled

Fortunately synchronous buses, as typically used for parallel data signal transfer, benefit from an extraordinary immunity to crosstalk. Crosstalk only occurs when the signals are being switched and this crosstalk only has an impact within a small window around the moment of the clocking. So, providing the receiver waits sufficiently long enough for the crosstalk to settle, before sampling the bus, the crosstalk has no impact on the signal quality at the receiver. I typically use the dual stripline configuration for the DDRx Address, Command and Control signals which are far less critical than the data lanes. But generally, each signal layer should be adjacent to, and closely coupled to, an uninterrupted reference plane, which creates a clear return path and eliminates broadside crosstalk.

iCD Design Integrity | Field Solver Technology

UNITS: mil — 5/31/2019 — Total Board Thickness: 51.6 mil

Differential Pairs > DDR3 40/80 ohms

Layer No.	Via	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)	Notes
		Soldermask		Dielectric	3.3	0.5								
1	8	Signal	Top	Conductive			1.4	20	6.5	0.44	41.36	81.31		Signal/Power
		Prepreg		Dielectric	4.3	3								
2		Plane	GND	Conductive			1.4							GND
		Core		Dielectric	4.3	12								
3		Signal	Inner 3	Conductive			1.4	20	20	1	42.3	78.54	56.01	Signal/Power
		Prepreg		Dielectric	4.3	16								
4		Signal	Inner 4	Conductive			1.4	20	20	1	42.3	78.54	56.01	Signal/Power
		Core		Dielectric	4.3	12								
5		Plane	GND	Conductive			1.4							GND
		Prepreg		Dielectric	4.3	3								
6		Signal	Bottom	Conductive			1.4	15	6.5	0.44	41.36	80.51		Signal/Power
		Soldermask		Dielectric	3.3	0.5								

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Figure 5–A six layer stackup top/bottom microstrip and middle dual stripline (iCD Stackup Planner)

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Figure 5 shows a typical six layer PCB stackup but, here I am using the signal layers for mixed signal/plane pours to eliminate the impact of the electromagnetic fields coupling. These days it is quite common to have ten or more power supplies on a board. So rather than allocating one or two per plane, it is best to use the dual stripline layers to provide mixed signal/power pours. It is a bit hard to visualize this in the spreadsheet format however Figure 6 illustrates the point clearly. Layers 3 and 4 can be used for critical signals but are separated by a power pour on either side. From left to right: Differential pair, broadside-coupled pair, coupling between unrelated signals. This gives the PCB designer flexibility, adds planar capacitance and provides plenty of room for multiple supplies.

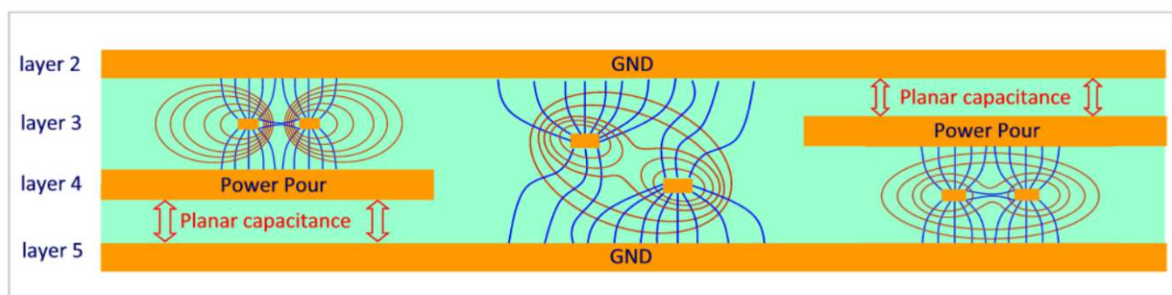

Figure 6–Mixed signal/power pours on the inner stripline layers

An advantage, of using high layer count boards, is that power and grounds planes can be placed closely together (2-5 mils) so as to provide high-frequency planar capacitance. Above 100MHz, planar capacitance replaces individual decoupling capacitors. These plane pairs are best positioned directly under a BGA near the (top or bottom) surface, rather than in the center of the symmetric stack to reduce via inductance.

A via that provides the connection between signal traces, referenced to planes of different DC potential, creates return path discontinuities. In other words, the return current has to jump between the planes to close the current loop, which in turn increases the inductance, affecting the signal quality. This return current can also excite the parallel plate resonance mode, causing significant electromagnetic radiation from the fringing fields.

When return current flows through the impedance of a cavity, between two planes, it generates voltage. Although quite small (typically in the order of 5mV) the accumulated noise from simultaneous switching devices can become significant. This voltage, emanating from the vicinity of the signal via, injects a propagating wave into the cavity which can excite the cavity resonances or any other parallel structure (for instance, between copper pours over planes). Other signal vias, also passing through this cavity, can pick-up this transient voltage as crosstalk. Plane pairs should be coupled closely together to dampen this cavity resonance and to provide high planar capacitance.

In order to design the perfect stackup, one needs to understand how and where the electromagnetic fields propagate and where the current return paths flow through the substrate. Placing power supplies as copper pours allows the designer to make full use of the planar capacitance and to isolate critical signals within the substrate.

Key Points:

- The speed of a digital signal does not depend intrinsically on the speed of electrons, but rather on the speed of energy transfer between electronic components.
- The energy propagates, between the signal trace and the return path(s), as an electromagnetic wave.
- Microstrip (outer) layer EM fields tend to radiate outward as there is only one solid plane beneath which blocks the emissions.

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- The electric fields of a stripline are totally contained between the two solid planes whereas the magnetic fields are also limited vertically by the planes. Radiation is reduced dramatically and is limited to just the edge fringing fields due to the shielding affects of the planes.
- Stripline crosstalk can be reduced by routing the signal traces orthogonally on adjacent layers reducing the couple to just a small area.
- For synchronous buses, crosstalk only occurs when the signals are being switched and this crosstalk only has an impact within a small window around the moment of the clocking.
- Each signal layer should be adjacent to, and closely coupled to, an uninterrupted reference plane, which creates a clear return path and eliminates broadside crosstalk.
- Rather than allocating one or two supplies per plane, it is best to use the dual stripline layers to provide mixed signal/power pours.
- Power and ground planes can be placed closely together so as to provide high-frequency planar capacitance in high layer count boards.
- Return current can also excite the parallel plate resonance mode, causing significant electromagnetic radiation from the fringing fields.
- Plane pairs should be coupled closely together to dampen the cavity resonance and to provide high planar capacitance.

References:

Beyond Design: Stackup Planning Parts 1-4, Plane Cavity Resonance, Faster than a Speeding Bullet, Signal Flight Time Variances in Multilayer PCBs, Crosstalk Margins, The Proximity Effect–Barry Olney
Electromagnetic Compatibility Engineering–Henry Ott
High Speed Digital Design–Howard Johnston
All graphics–Barry Olney

Bio:

Barry Olney is Managing Director of In-Circuit Design Pty Ltd (iCD), Australia. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN and CPW Planner, is a PCB Design Service Bureau and specializes in board level simulation. The software can be downloaded from www.icd.com.au

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Calculates Series Terminator of the Distributed System Including Loads
PDN EMI Plot with EMC limits (FCC, CISPR) to 100GHz