

Split Planes: Reprise

Beyond Design

by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

A high-speed digital signal crossing a split in the reference plane impacts at least three aspects of design integrity: signal quality, crosstalk, and EMI. The problem is the impedance discontinuity in the return signal path crossing the split. Any discontinuity in impedance reflects energy back toward the source, particularly the higher-frequency components of the signal. At high frequencies, the return current follows the path of least inductance, which is directly above and/or below the signal trace, but that path is broken by the split. In this case, the return current has to find an alternative path back to the source, creating a larger loop area. In this month's column, I will review the two common solutions to this issue, plus introduce a third optimal solution for high-speed design.

1. The Pass-Through Gap

Low-frequency circuits in the audio range can often benefit from splitting the ground planes, whereas digital circuits cannot be effectively isolated from analog circuits using this method. Many years ago, wiring the ground connections to one common point was a great way to eliminate noise in a guitar amplifier, particularly value-based amplifiers. But as frequency increases, the parasitic capacitive and inductive components dominate, and distance or electromagnetic shielding is the only solution.

The key to a successful mixed analog/digital design is functional partitioning, understanding the current return path, and routing

control and management—not carving up the ground planes. Analog and digital grounds should be connected together through a low impedance path. It is always better to have just one single reference (ground) plane for a system.

When both analog and digital devices are used on the same PCB, it is usually necessary to partition (not split) the ground plane. The components should be grouped by functionality and positioned such that no digital signals will cross over the analog ground, and no analog signals will cross over the digital ground. Precise partitioning will minimize the trace lengths, improve signal quality, minimize the coupling, and reduce radiated emissions and susceptibility. This is traditionally done by using keep-out zones, whereby no trace can cross through the keep-out area. But this also creates issues in that data and control signals need to go into and out of these sensitive areas.

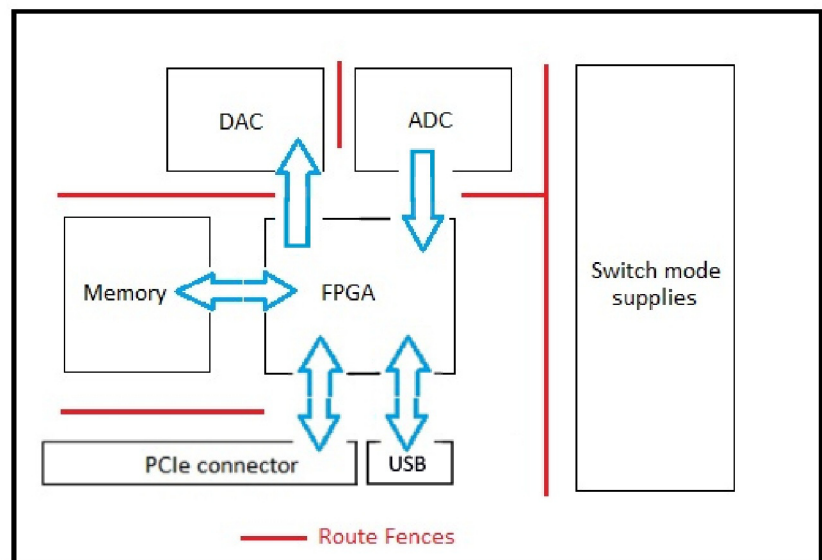


Figure 1: Route fences used to control routing and isolation.

Particular care needs to be taken with oscillators and switch-mode power supplies that may generate high-frequency electromagnetic fields. If space permits, keep these circuits at least 250 mils from any critical signals to avoid parasitic coupling.

Route fences (a thin elongated keep-out), rather than regional keep-out areas, are a useful tool to control the routing. The ground plane should not be split; rather, a pass-through gap is left in the fences so that data and control signals can enter and leave that area, as seen in Figure 1. At high frequencies, return current follows directly under the signal trace on the reference plane, and as such, will follow the trace through the pass-through gap.

2. Bridging Planes of Different Potential

These days, it is quite common to have multiple power supplies on a board. Instead of allocating one or two power supplies per plane, it is best to use the dual-stripline layers to provide mixed-signal/power pours and reduce the layer count. This also prevents the overlapping of electromagnetic fields, which creates crosstalk.

This is particularly critical with dual asymmetric stripline configurations where one or two signal layers are sandwiched non-uniformly between two planes, as in Figure 2. It is important to have a clearly defined return current path and to know exactly where the return current will flow. The question is not, “Which plane does the return current flow on?” but, “How is the current distributed on each plane?” Also, if a return path discontinuity exists, then the current tends to divert increasing the loop area, inductance, and delay.

A via that provides the connection between signal layers, referenced to planes of different DC potential, creates return path discontinuities. In other words, the return current has to pass between the planes to close the current loop, which increases the inductance, affecting the signal quality. This return current can also excite the parallel plate resonance mode, causing significant electromagnetic radiation from the fringing fields.

If the reference planes are at the same DC potential, then they can be directly connected by stitching vias near the signal via transition to provide shorter paths for the return current.

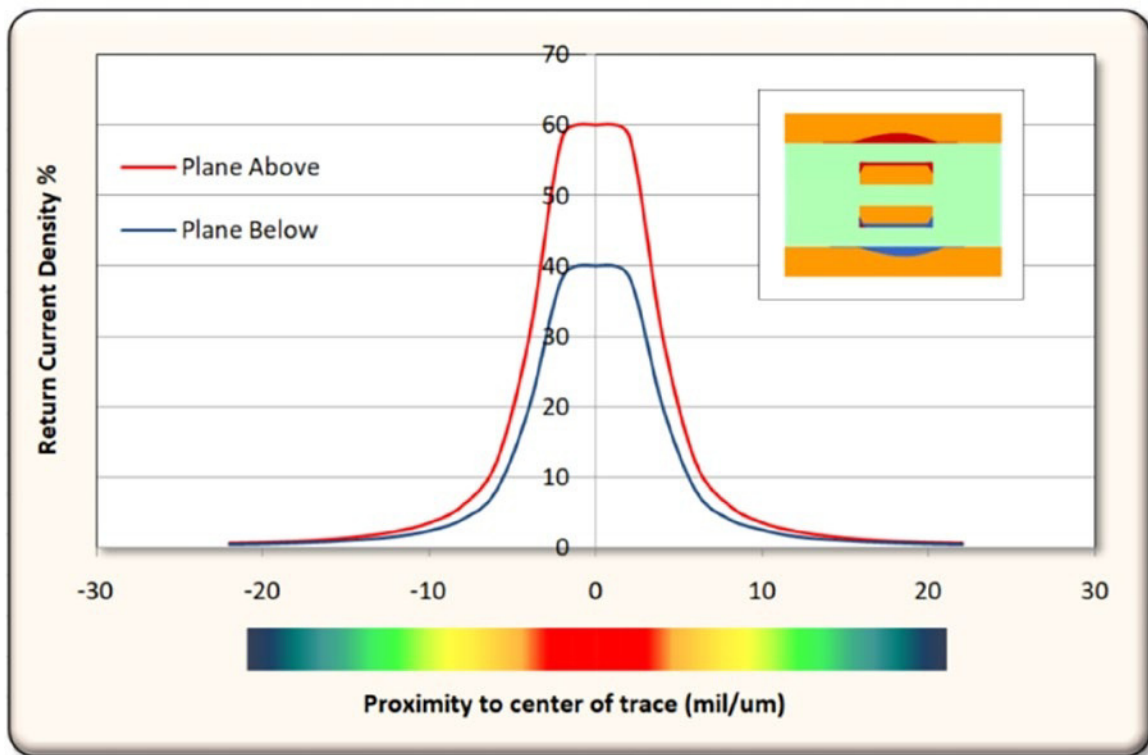


Figure 2: Return-path current density for a dual asymmetric stripline.

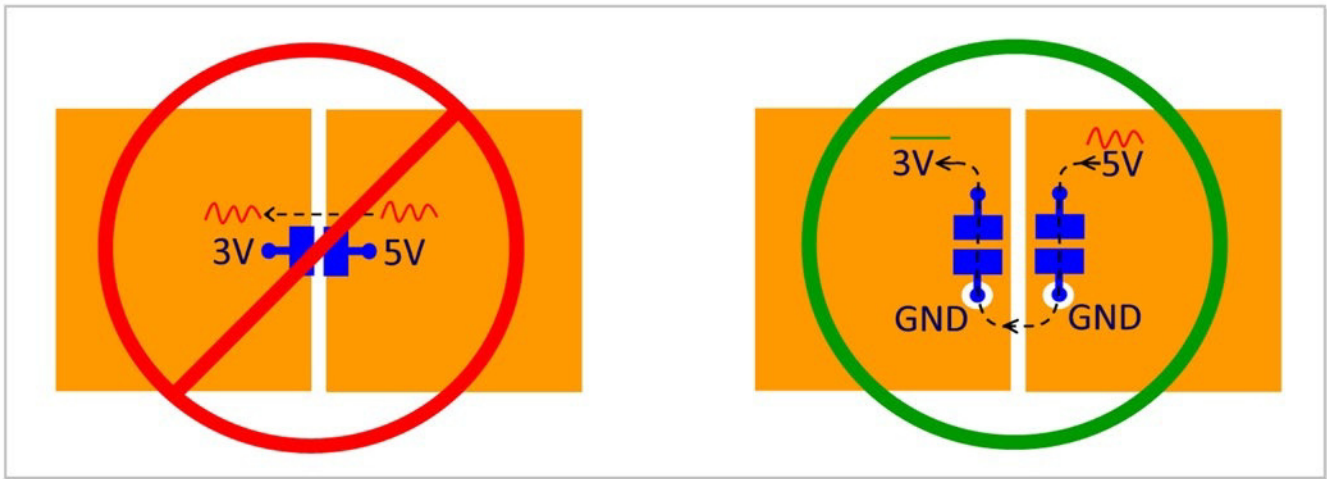


Figure 3: Eliminating the transfer of noise in the return path of split power planes (right).

However, if the planes are at different DC potential, then a bypass capacitor can be connected across the planes at these points, as in Figure 3 (left). Unfortunately, this can pass AC noise between the power supplies. Two bypass capacitors, configured as in Figure 3 (right), is a much better solution, as this eliminates the transfer of power supply noise from one supply to another. Although this does add an additional loop area, it also provides additional decoupling to the planes, reducing power distribution network impedance.

3. Planar Capacitance

The aforementioned solutions work for most designs, but are they the optimal solution for a high-speed signal to cross a split plane? A slot in the plane under two or more nearby signal traces will usually cause return currents to overlap (shared return path), resulting in some degree of crosstalk. And since dense designs can have 20 or more power regions, spanning

just five or so plane pairs, then most complex designs can't possibly be routed without crossing a split. This issue arises in nearly every intricate design. Adding 100 nF ceramic capacitors to span the split consumes real estate and creates a larger loop area, which, in turn, creates emissions to some extent.

The secret here is to design the stackup in such a way as to make use of planar capacitance, instead of bypass capacitors, by making sure each VDD/VCC region is closely coupled to a continuous ground plane. A plane pair is basically a large capacitor that becomes more efficient as the dielectric becomes thinner. Signal layers must also have an adjacent solid ground return plane to properly steer the electromagnetic wave. By using a combination of three plane layers as in Figure 4, the planar capacitance will provide an alternative return path to transverse the gap. This does not increase the plane count because the next signal layer in the stackup can also use the additional ground plane. Since the

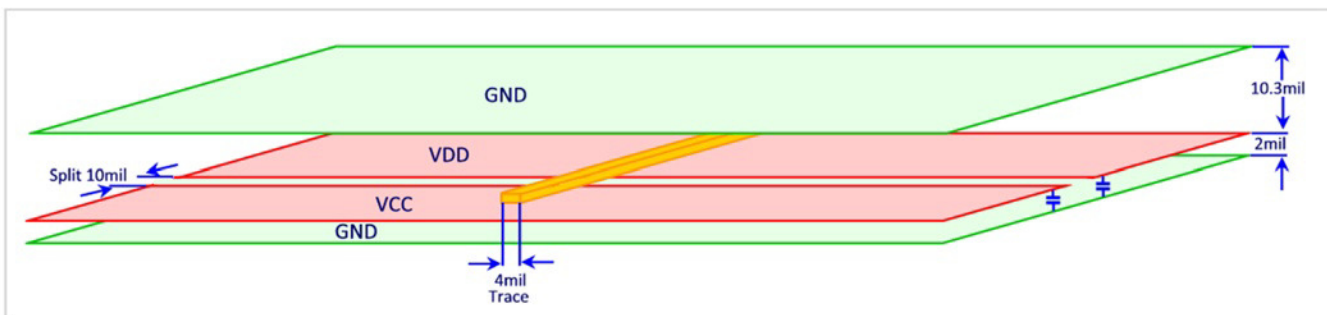


Figure 4: 3D view of the split plane stripline configuration.

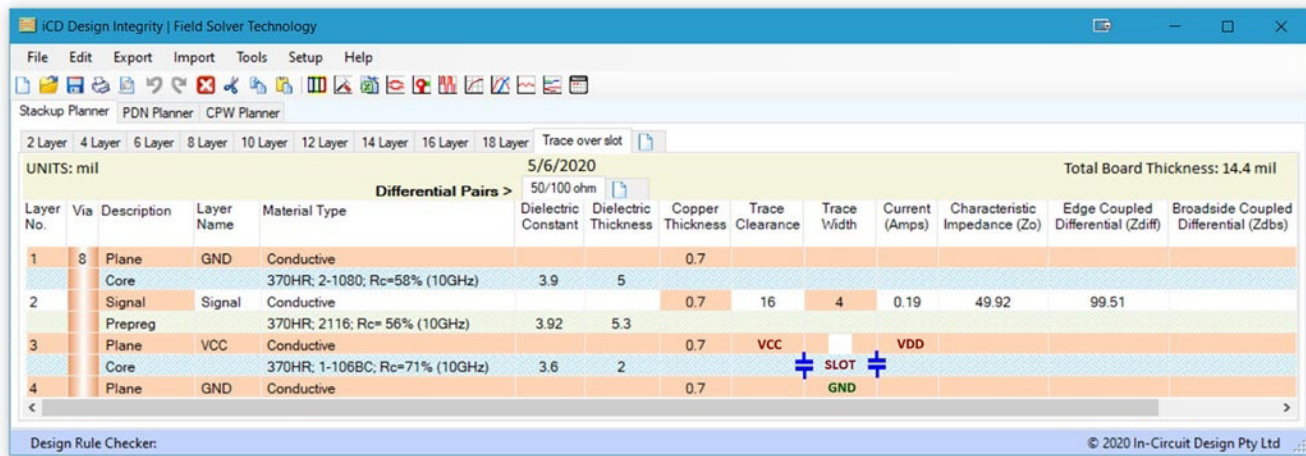


Figure 5: Thin dielectric creates more planar capacitance (iCD Stackup Planner).

skin effect forces current to flow in the outer periphery of the plane at high frequencies, it virtually creates two independent ground planes on the top and bottom surfaces with no return path crosstalk, although it is actually one physical sheet of copper.

However, this methodology is also frequency dependant and determined by geometry. As the frequency increases, more power is injected into the plane cavity propagating along the slot. Above 10 GHz, the slot mode radiation begins to couple excessive electromagnetic energy into the adjacent traces.

Properly designed power distribution networks have the power planes tightly coupled to their respective ground planes, as in Figure 5, to provide planar capacitance. Of course, none of this is valid if the two planes are far apart. Stackup data can be transferred to the iCD PDN Planner to demonstrate the impact of planar capacitance on plane resonance for different configurations.

If very thin dielectrics (2–3 mils) are used between the power and ground planes, split planes can have minimal impact on the quality of signal transmission if designed correctly. If the split plane is covered with solid ground planes both above and below in a stripline configuration, radiation will not be an issue. And keep in mind that this also applies to differential pairs traversing a split plane. The return current flows in the reference planes(s)—not the opposite signal trace, particularly if the pair is not very tightly coupled.

One would typically use a minimum gap of 20 mils to isolate planes of dissimilar potential. However, with today's modern fabrication etching techniques, a 10-mil gap is quite acceptable for low voltage applications (but please check with your fab shop first).

Ground planes should never be split with the exception of audio frequency circuits, special RF/microwave applications, and for high-voltage isolation. Functional partitioning and controlled routing is the key to a successful mixed-signal design, while utilizing planar capacitance is an excellent solution for high-speed digital designs up to 10 GHz.

Key Points

- A split in a ground plane creates an impedance discontinuity in the return signal path.
- Low-frequency circuits in the audio range can often benefit from splitting the ground planes.
- The key to a successful mixed analog/digital design is functional partitioning, understanding the current return path, and routing control and management.
- Route fences are a useful tool to control the routing.
- The ground plane should not be split; rather, a pass-through gap is left in the fences so that data and control signals can enter and leave that area.
- Dual-stripline layers can provide mixed-signal/power pours and reduce the layer count.

- If a return path discontinuity exists, then the current tends to divert increasing the loop area, inductance, and delay.
- A via that provides the connection between signal layers, referenced to planes of different DC potential, creates return path discontinuities.
- If the reference planes are at the same DC potential, then they can be directly connected by stitching vias near the signal via transition.
- If the planes are at different DC potential, then a bypass capacitor can be connected across the planes.
- Two bypass capacitors are a much better solution, as this eliminates the transfer of power supply noise from one supply to another.
- A slot in the plane under two or more nearby signal traces will cause return currents to overlap, resulting in some degree of crosstalk.
- The secret for high-speed design is to construct the stackup in such a way as to make use of planar capacitance by making sure each VDD/VCC region is closely coupled to a continuous ground plane.

- If thin dielectrics are used between the power and ground planes, split planes can have minimal impact on the quality of signal transmission. **DESIGN007**

Further Reading

- B. Olney, "Beyond Design: Stackup Planning, Part 5," *Design007 Magazine*, July 2019.
- B. Olney, "Beyond Design: The Proximity Effect," *Design007 Magazine*, March 2019.
- B. Olney, "Beyond Design: Split Planes in Multilayer PCBs," *The PCB Design Magazine*, March 2015.
- B. Olney, "Beyond Design: The Plain Truth About Plane Jumpers," *The PCB Design Magazine*, November 2012.
- H. W. Johnson & M. Graham, *High-Speed Digital Design: A Handbook of Black Magic*, Prentice Hall, 1993.
- Yuriy Shlepnev, et al. "Stripline With One Solid and One Split Reference Plane: SI List."



Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded at icd.com.au. To read past columns or contact Olney, [click here](#).

National Instruments to Acquire OptimalPlus

National Instruments Corporation, the provider of a software-defined platform that accelerates the development and performance of automated test and automated measurement systems, announced it has entered into a definitive agreement to acquire OptimalPlus Ltd., a global leader in data analytics software for the semiconductor, automotive and electronics industries.

The acquisition will expand NI's enterprise software capabilities to provide customers with business-critical insights through advanced product analytics across their product development flow and supply chain.

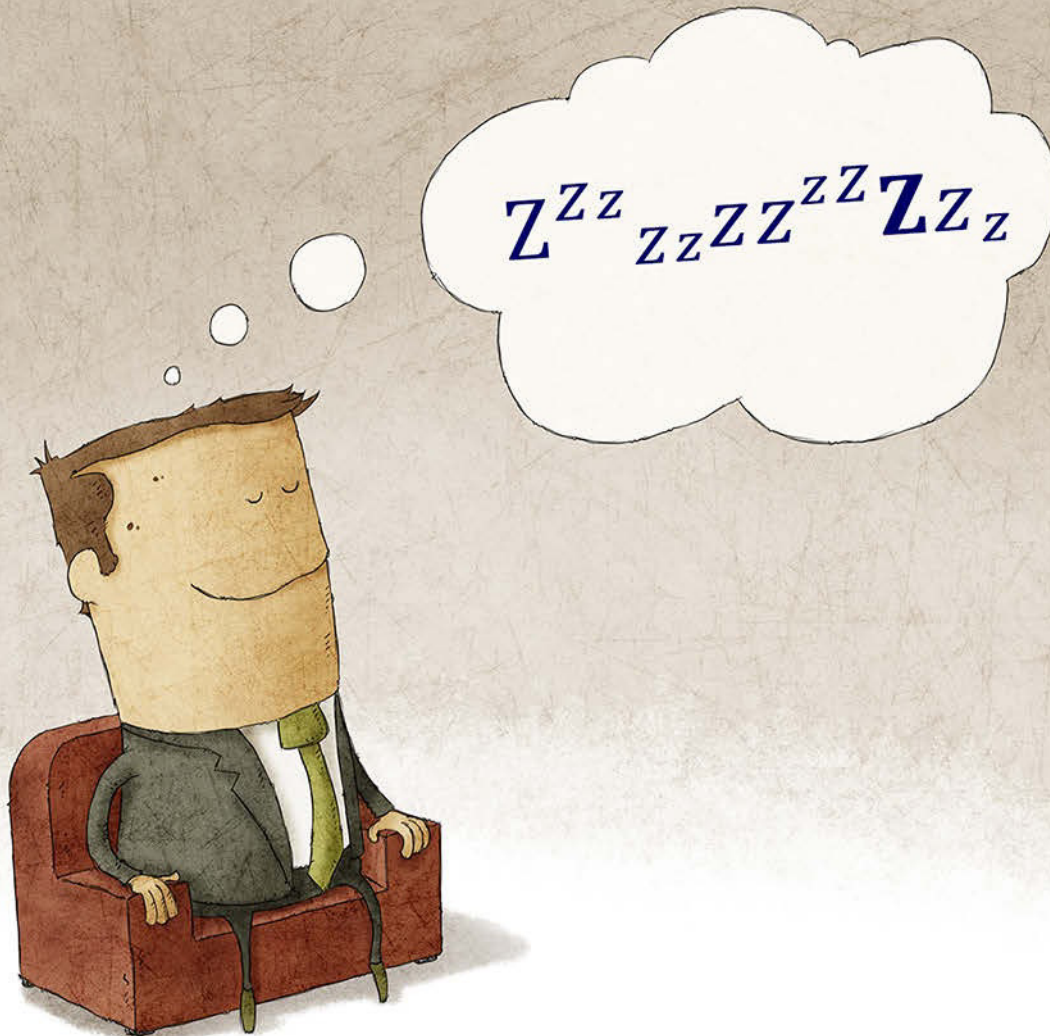
NI and OptimalPlus serve highly complementary positions in the semiconductor, automotive and electronics industries. NI test systems are used in semiconductor manufacturing with OptimalPlus serving as a leading supplier of semiconductor manufacturing data analytics.

Similarly, the NI automotive and electronics production test offerings are complementary to OptimalPlus' growing automotive and electronics analytics business. Combining the strength of NI's software-centric approach with OptimalPlus' enterprise-level analytics software is expected to dramatically increase the value of test and manufacturing data, enabling product insights that will improve quality, efficiency and time to market for both NI and OptimalPlus customers.

"The addition of OptimalPlus' data analytics capabilities will enable us to accelerate our growth strategy by increasing enterprise-level value for shared customers in the semiconductor and automotive industries," said Eric Starkloff, NI President and CEO.

(Source: Business Wire)

We **DREAM** Impedance!



Did you know that two seemingly unrelated concepts are the foundation of a product's performance and reliability?

- Transmission line impedance and
- Power Distribution Network impedance

DISCOVER MORE

iCD software quickly and accurately analyzes impedance so you can sleep at night.

iCD Design Integrity: Intuitive software for high-speed PCB design.

iCD
In-Circuit Design Pty Ltd

"iCD Design Integrity software features a myriad of functionality specifically developed for PCB designers."

– Barry Olney



www.icd.com.au