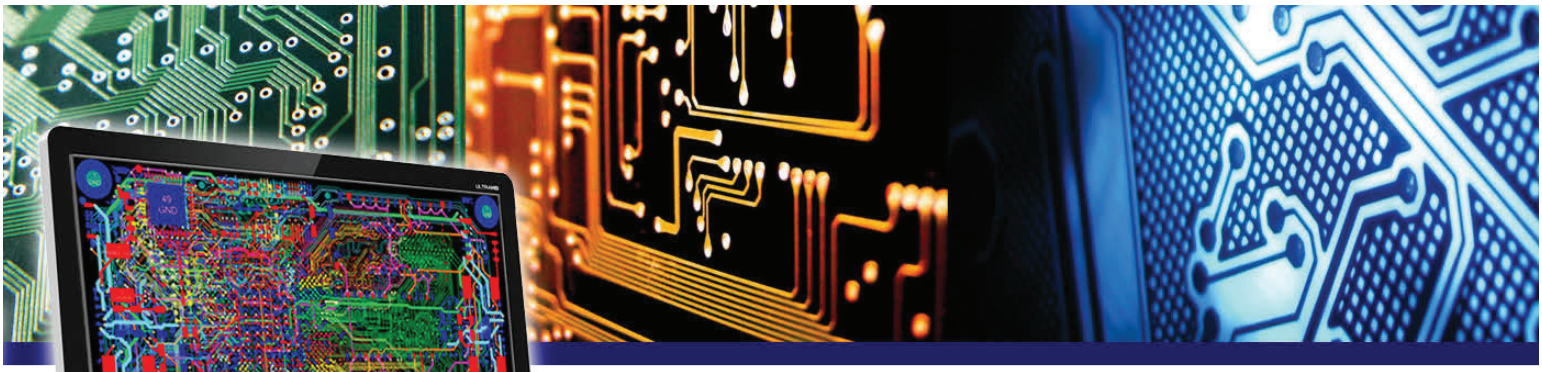

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Split Planes in Multilayer PCBs

by Barry Olney
IN-CIRCUIT DESIGN PTY LTD

Creating split planes or isolated islands in the copper planes of multilayer PCBs at first seems like a good idea. Today's high-speed processors and FPGAs require more than six or seven different high-current power sources. And keeping sensitive analog circuitry isolated from those nasty, fast, digital switching signals seems like a priority in designing a noise-free environment for your product. Or is it?

Many analog-to-digital converter (ADC) manufacturers recommend the use of split ground planes. "The analog ground (AGND) and digital ground (DGND) pins must be connected together externally to the same low impedance ground plane with minimum lead length." This has been the age-old method for audio design. However, this approach has the potential of creating a number of additional problems in high-speed digital circuits. A much better way to connect AGND and DGND together, through a low impedance path, is to use only one ground plane to begin with.

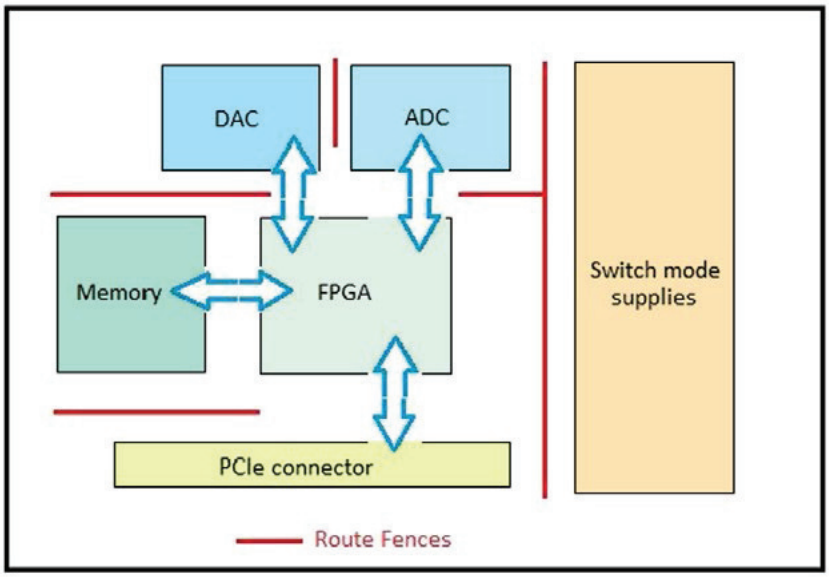


Figure 1: Route fences used to control routing and isolation.

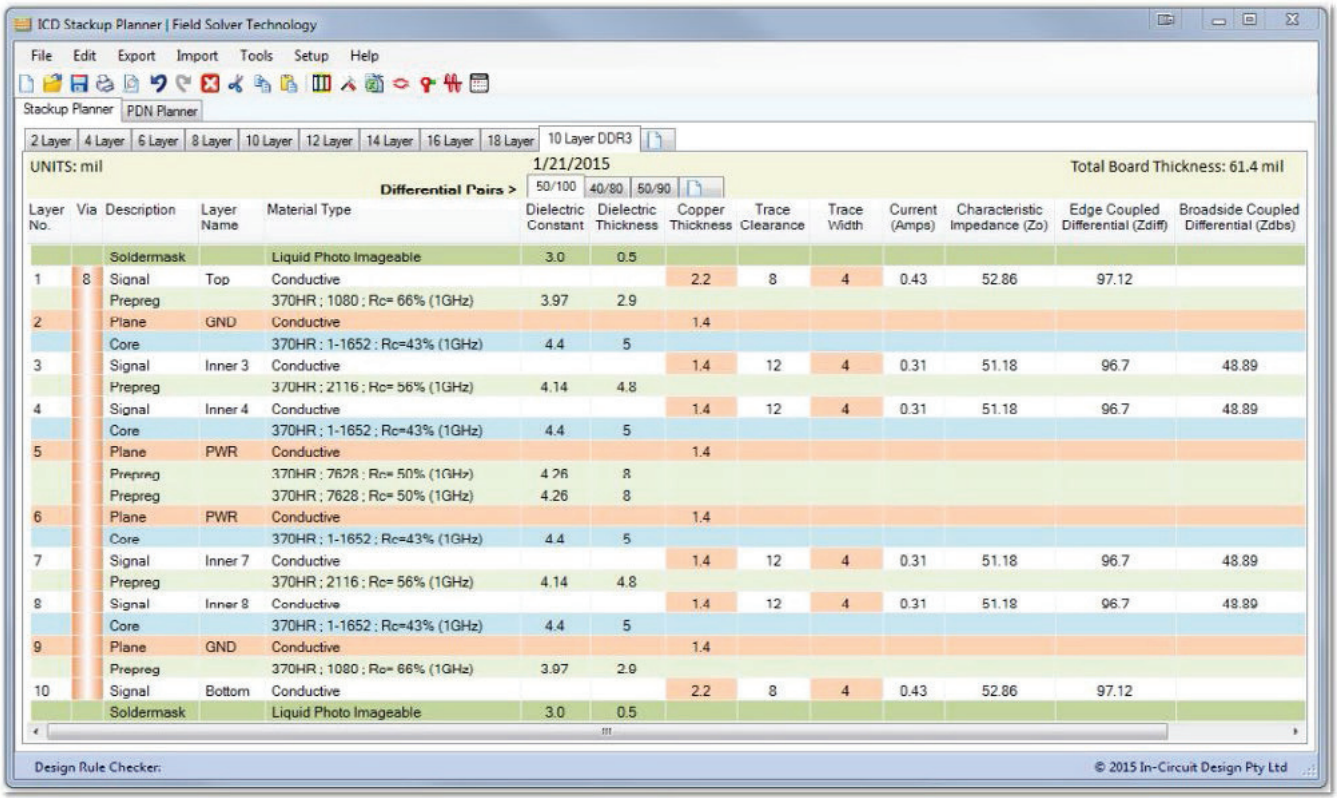
When both analog and digital devices are used on the same PCB, it is usually necessary to partition (not split) the ground plane. The components should be grouped by functionality and positioned so that no digital signals will cross over the analog ground, and no analog signals will cross over the digital ground. Precise partitioning will minimize the trace lengths, improve signal quality, minimize the coupling and reduce radiated emissions and susceptibility. This is traditionally done by using keep-out zones whereby no trace can cross through the keep-out area. But this also creates issues in that control signals need to go into and out of these sensitive areas.

Particular care needs to be taken with oscillators and switch mode power supplies that may generate high frequency electromagnetic fields. If space permits, keep these circuits 10mm from any critical signals to avoid parasitic coupling.

Route fences, rather than route keep-outs, are useful to control the routing. Controlled routing is the key to a successful mixed signal design. The planes should not be split, but rather a pass-through gap is left in the plane so that control signals can enter and leave that area as seen in Figure 1. Route fences are also very effective is controlling an autorouter. They can be set up for each router pass and then moved to a different location. This is best done with interactive cross-probing from schematic to PCB, controlling functional sections of the design one-by-one, building up the route to completion.

At low frequencies, current follows the path of least resistance. But at high frequencies, return current follows the path of least inductance—which happens to be directly under the signal trace on a plane (power or ground) that is closest to

SPLIT PLANES IN MULTILAYER PCBS *continues*



Layer No.	Via	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)
		Soldermask		Liquid Photo Imageable	3.0	0.5							
1	8	Signal	Top	Conductive			2.2	8	4	0.43	52.86	97.12	
		Prepreg		370HR ; 1080 ; Rc= 66% (1GHz)	3.97	2.9							
2		Plane	GND	Conductive			1.4						
		Core		370HR ; 1-1652 ; Rc=43% (1GHz)	4.4	5							
3		Signal	Inner 3	Conductive			1.4	12	4	0.31	51.18	96.7	48.89
		Prepreg		370HR ; 2116 ; Rc= 56% (1GHz)	4.14	4.8							
4		Signal	Inner 4	Conductive			1.4	12	4	0.31	51.18	96.7	48.89
		Core		370HR ; 1-1652 ; Rc=43% (1GHz)	4.4	5							
5		Plane	PWR	Conductive			1.4						
		Prepreg		370HR ; 7628 ; Rc= 50% (1GHz)	4.26	8							
		Prepreg		370HR ; 7628 ; Rc= 50% (1GHz)	4.26	8							
6		Plane	PWR	Conductive			1.4						
		Core		370HR ; 1-1652 ; Rc=43% (1GHz)	4.4	5							
7		Signal	Inner 7	Conductive			1.4	12	4	0.31	51.18	96.7	48.89
		Prepreg		370HR ; 2116 ; Rc= 56% (1GHz)	4.14	4.8							
8		Signal	Inner 8	Conductive			1.4	12	4	0.31	51.18	96.7	48.89
		Core		370HR ; 1-1652 ; Rc=43% (1GHz)	4.4	5							
9		Plane	GND	Conductive			1.4						
		Prepreg		370HR ; 1080 ; Rc= 66% (1GHz)	3.97	2.9							
10		Signal	Bottom	Conductive			2.2	8	4	0.43	52.86	97.12	
		Soldermask		Liquid Photo Imageable	3.0	0.5							

Figure 2: A 10-layer DDR3 stackup.

the trace. This also provides the smallest loop area.

When a trace crosses a gap in the adjacent plane, the return current is diverted from underneath the trace in order to go around the gap. This causes the current to flow through a much larger loop area which changes the characteristic impedance of the trace, increases the crosstalk between adjacent traces, and thus increases the radiation from the board. In some instances, the return current may have to go all the way back to the power supply. A major EMC problem occurs when there are discontinuities in the current return path. Routing traces via the pass-through gap alleviates these problems and still allows vital signals to enter and leave the sensitive area. The return current will always follow the signal traces and will not go through other areas.

Also, there is the issue of what to do with all the different power supplies for the major chips without splitting the planes. These days, it is typical to have six or more different supplies. In fact, a DDR3 motherboard that I just completed had a count of 30 different supplies plus an analog and a digital ground. On a complex multilayer board, it is typical to use eight or more layers, four of these being planes.

Figure 2 shows how the ICD Stackup Planner was used to calculate the impedance of the traces and to plan the stackup of the PCB substrate using multiple supplies. This may at first look unusual for DDR3 design, but the addition of copper pours on the dual stripline layers changes everything. Power planes are on layers 5 and 6 and are also placed as pours under the chips on the top and bottom layers. However, pouring copper over the entire outer layers is not recommended. With this particular design, ground pours were added to layers 4 and 7 under the DDR3 devices, to drop the impedance in these areas to 40/80 ohm single-ended/differential. Figure 3 shows layer 4 as GND and the impedance has been altered to 40/80 ohms with the addition of this plane under the DDR3 devices. This also provides good planar capacitance and stability for the 1.5V power distribution network (PDN).

UNITS: mil | 1/21/2015 | Differential Pairs > 50/100 40/80 50/90 | Total Board Thickness: 62.8 mil

Layer No.	Via	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)
		Soldermask		Liquid Photo Imageable	3.0	0.5							
1	8	Signal	Top	Conductive			2.2	8	4	0.43	52.86	97.12	
		Prepreg		370HR ; 1080 ; Rc= 66% (1GHz)	3.97	2.9							
2		Plane	GND	Conductive			1.4						
		Core		370HR ; 1-1652 ; Rc=43% (1GHz)	4.4	5							
3		Signal	Inner 3	Conductive			1.4	12	4	0.31	40.76	80.75	
		Prepreg		370HR ; 2116 ; Rc= 56% (1GHz)	4.14	4.8							
4		Plane	GND	Conductive			1.4						
		Core		370HR ; 1-1652 ; Rc=43% (1GHz)	4.4	5							
5		Plane	PWR	Conductive			1.4						

Figure 3: Impedance altered to 40/80 ohms by pours under the DDR3 devices.

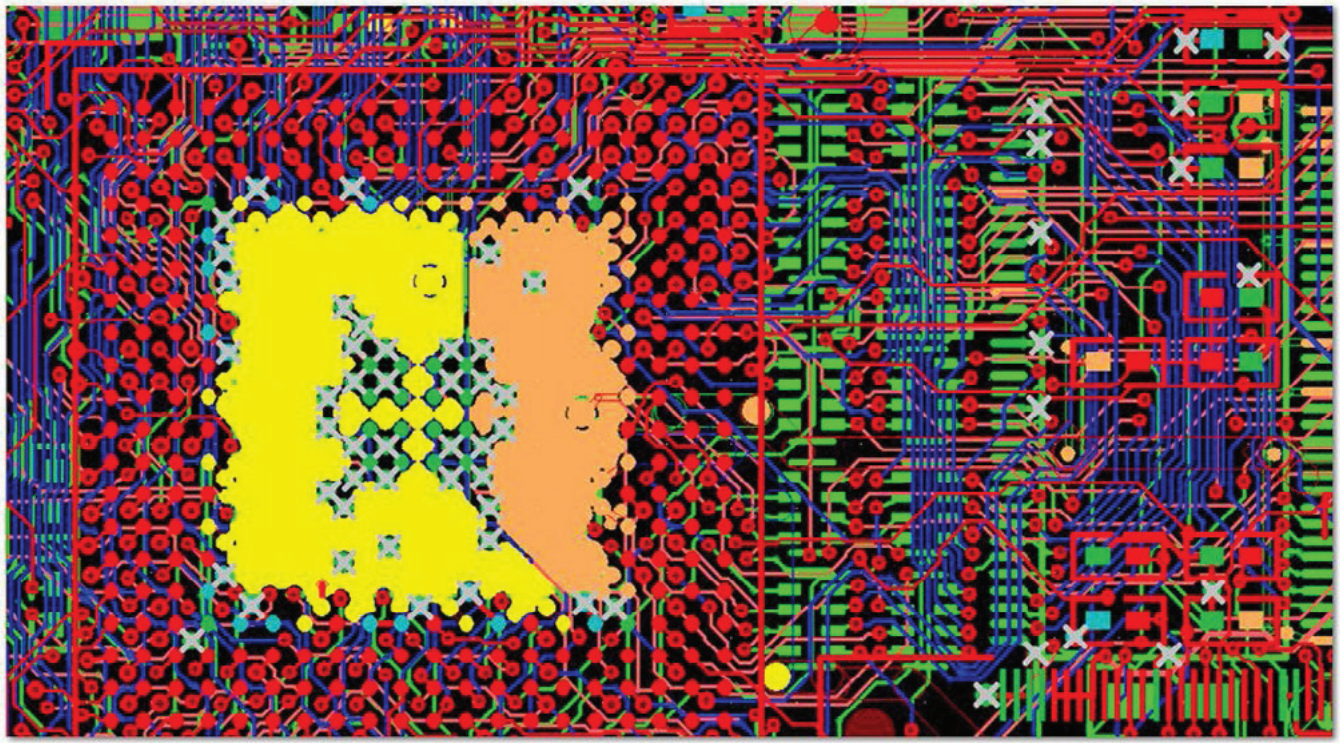


Figure 4: Supplies routed directly under the IC on the top layer.

One of the keys to determining the optimal PCB stackup is to understand how and where the return signals actually flow. The schematic only shows the signal path whereas the return path is implicit. The ICD Stackup Planner allows the designer to determine any number of single-ended and differential impedance technologies on the same substrate. In Figure 3, I have simulated 50/100 (digital), 40/80 (DDR3) and 50/90 ohm (USB) on the same substrate.

It is recommended to use as many GND planes as possible in the stackup. The decoupling capacitor and IC GNDs naturally provide stitching vias to connect the GND planes in most cases. However, any plane, not just ground, can act as the return path of a signal. Care must be taken to ensure there is a provision for enough decoupling between the power and ground planes, in this case. But still, even after putting as many supplies as possible on the power planes, without doubling up, we soon run out of planes. So what do we do with the other supplies?

In the above screenshot of Figure 3, 1V8

(yellow) and 2V5 (orange), supplies are routed on the top layer and the core fills (copper pours) are placed directly under the processor chip. Since there is little room for routing on the top (or bottom) layer anyway, this does not affect the routability of the design but rather has the added advantage of a low inductance power supply close to the chip.

In conclusion, split ground planes are a great way to create discontinuities of impedance, crosstalk and EMI—so, don't use them! Controlled routing is the key to a successful mixed signal design. The ground planes should not be split, but rather partitioned and a pass-through gap left in the plane so that vital signals can enter and leave the sensitive area.

Points to Remember

- The best way, to connect AGND and DGND together through a low impedance path, is to use only one ground plane to begin with.
- When both analog and digital devices are used on the same PCB, it is usually necessary to partition (not split) the ground plane.
- Keep-outs create issues in that control signals need to go into and out of these sensitive areas.
- If space permits, keep these circuits 10 mm from any critical signals to avoid parasitic coupling.
- Route fences, rather than route keep-outs, are useful to control the routing.
- The planes are not split but rather a pass-through gap is left in the plane so that control signals can enter and leave that area. Route fences are also very effective is controlling an autorouter.
- At low frequencies, current follows the path of least resistance. But at high frequencies, return current flows the path of least inductance—which happens to be directly under the signal trace on a plane (power or ground) that is closest to the trace.
- When a trace crosses a gap in the adjacent plane, the return current is diverted from underneath the trace in order to go around the gap. This causes the current to flow through a much larger loop area.
- A major EMC problem occurs when there are discontinuities in the current return path. Routing traces via the pass-through gap alleviates these problems and still allows vital signals to enter and leave the sensitive area.
- Pouring copper over the entire outer layers is not recommended.
- One of the keys to determining the optimal PCB stackup is to understand how and where the return signals actually flow. The schematic only shows the signal path, whereas the return path is implicit.
- The ICD Stackup Planner allows the designer to determine any number of single-ended and differential impedance technologies on the same substrate.
- Use as many GND planes as possible in the stackup. The decoupling capacitor and IC GNDs naturally provide stitching vias to connect the GND planes in most cases.
- Supplies may be routed on the top layer and the core fills (copper pours) are placed directly under the processor chip.
- Split ground planes are a great way to create discontinuities of impedance, crosstalk and EMI—so, don't use them! **PCBDESIGN**

References

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2. Howard Johnson: High-Speed Digital Design—A Handbook of Black Magic.

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4. The ICD Stackup and PDN Planner: www.icd.com.au.

Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. This PCB design service bureau specializes in board-level simulation, and has developed the ICD Stackup Planner and ICD PDN Planner software. To read past columns, or to contact Olney, click here.