

# Simulation Slashes Iterations

## Beyond Design

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The majority of high-speed digital designs take at least two iterations to develop into a working product. However, these days, the product life cycle is very short; therefore, time to market is of the essence. An aggressive timeline can mean that a re-spin is not possible. Plus, it will cost more than just engineering time; one must also consider the cost of delaying the product's market launch. This missed opportunity could cost hundreds of thousands of dollars.

However, multilayer boards can be designed to work right the first time with little additional effort, providing you follow a tried and proven process that results in a reliable, manufacturable design that performs to specifications and is produced on time and to budget. One of the most frustrating aspects of PCB design is when you have to redo work that has already been completed. Yet design re-spins will continue

to happen until designers make regular use of simulation software.

Complex multilayer boards should be designed using a proven design methodology, incorporating pre-layout simulation before placing a single chip on the board. Simulation tools can be used to analyze various signal integrity (SI) issues like reflections (due to impedance mismatches), crosstalk, signal attenuation, stackup and power distribution network (PDN) impedance, and noise—all of which can impact interconnect performance.

Unfortunately, simulation is often engaged toward the end of the design cycle, which is too late. Ideally, the simulation should be done during the design process as part of standard practice. The post-layout simulation should be the final PCB design process, not the first. If changes are made late in the design

process, then it takes more time, people, material, and money.

This is where board-level simulation cuts re-spins: A pre-layout simulation identifies issues in the conceptual stage so that they can easily be avoided, and the post-layout simulation catches the issues during the design process eliminating the potentially disastrous final stage changes. Of course, you also need to keep your eye on the ball during the entire design process, catching any small issue before it becomes a major problem. This is the most cost-effective way to design a board with fewer iterations rather than starting with the “find-and-fix” post-layout simulation approach.

There are multiple facets to board-level analysis, including:

- Stackup planning for controlled impedance, SI, crosstalk, and cost control
- Dielectric material selection for manufacturing yield and high-frequency operation
- Transmission line termination strategy
- Floor-planning for critical components
- Deriving layout routing constraints, including trace width, spacing, and delay matching

- PDN optimization
- I/O buffer and drive strength selection
- Topology optimization
- SI analysis to meet the design specifications, with respect to noise margins, timing, skew, crosstalk, and signal distortion
- Estimated electromagnetic radiation

The board stackup configuration is the most often overlooked issue in the early design stages. The majority of designers leave the stackup planning to deal with at design completion, along with fabrication deliverables. Before starting a PCB design, you need to plan the PCB stackup and impedance to ensure that the selected substrate materials are available from your chosen fabricator—a step that is regularly missed. Changing the stackup toward the end of the design process could mean changing trace widths and clearances to achieve the correct impedance, which could create a lot of unnecessary work.

If you use the same materials that the fab shop stocks to build your stackup, then the impedance will be more accurate (Figure 1). If we just choose a convenient (virtual) number for core thickness, for example, then this may

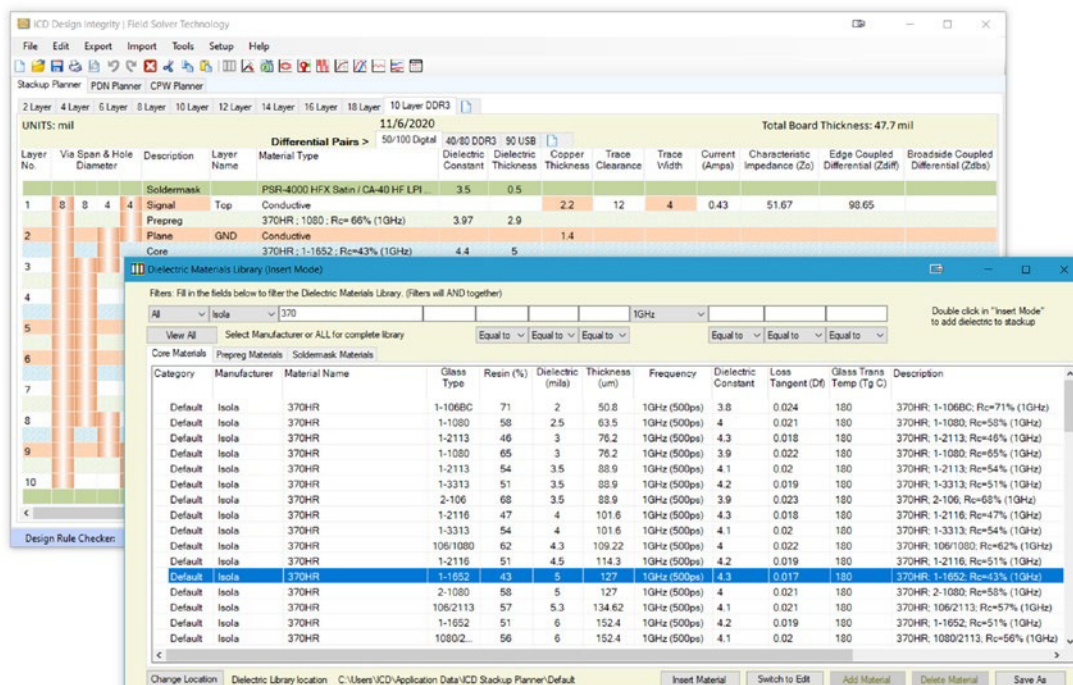


Figure 1: The dielectric materials library lists the fabricator’s stocked materials (iCD Stackup Planner).

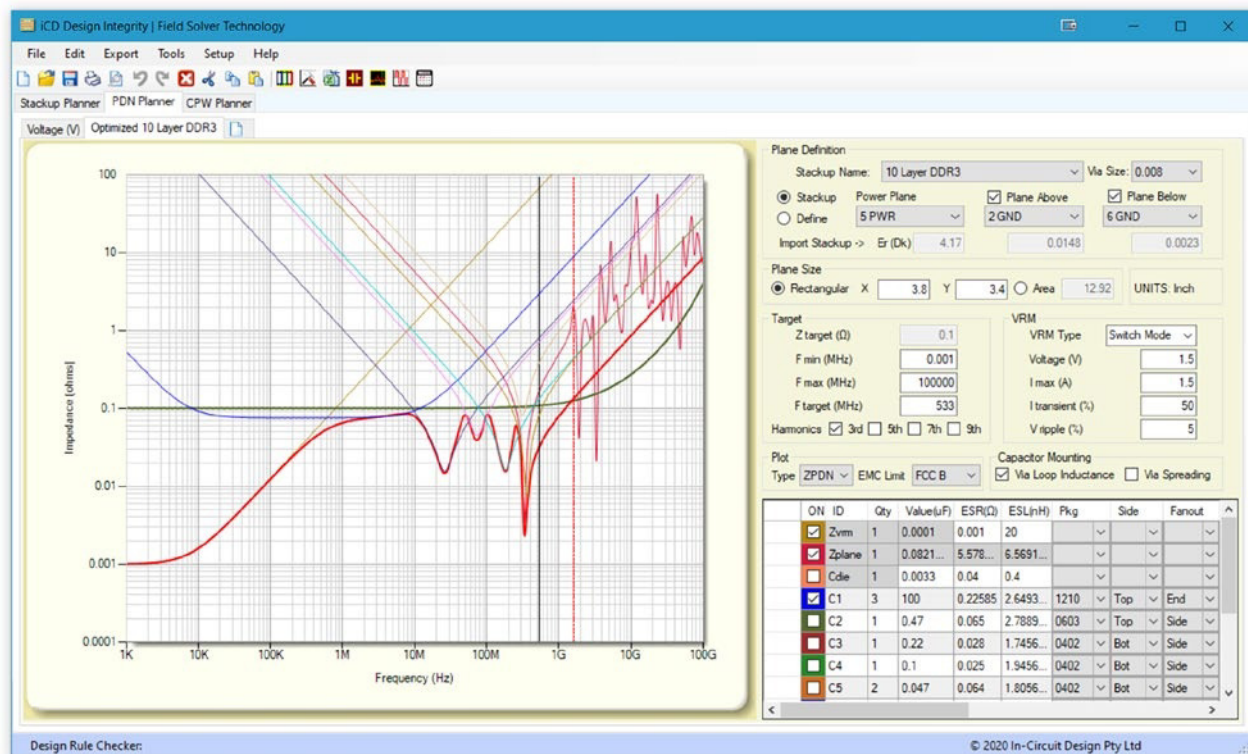


Figure 2: Optimized DDR3 PDN (iCD PDN Planner).

be up to 3% different from what is available; hence, the impedance will vary by 3%. Incorrect impedance creates reflections that lead to downstream SI, crosstalk, and radiation issues.

The design of the PDN is also a very important part of the conceptual design process, ensuring that you have a stable power delivery system before you even start placing a chip on the board.

Decoupling and bypass capacitors supply instantaneous current at different frequencies to the drivers until the power supply can respond. In other words, it takes a finite time for the current to flow from the power supply circuit (whether on-board or remote) due to the inductance of the trace and/or leads to the drivers. Decoupling capacitors also lower the impedance at different frequencies to help meet the AC impedance target.

Every decoupling capacitor has an equivalent series inductance (ESL) and mounting inductance that causes its impedance to increase at high frequencies. To reduce this inductance as much as possible, several small value decaps should be spread throughout the PDN. These decaps interact to create anti-resonance peaks

but should work together to lower the AC impedance. This is a trial-and-error process and needs to be done with the assistance of a PDN analysis tool (Figure 2).

A post-layout simulation requires the translation of the design files so that they can be read into the simulator. The simulation software should interface to all major EDA PCB design packages. However, if you have a simulation tool that is built into the PCB design software, then critical signals can be readily simulated by extracting the topology into the simulation environment. This creates a free-form schematic of the transmission lines, including drivers, microstrip and stripline modules, vias, and loads.

A batch mode simulation identifies possible SI, crosstalk, and EMC violations. Interactive simulation is then used to further analyze these potential issues. Crosstalk is typically picked up on long parallel trace segments. These can be on the same layer, as in Figure 3, but may also be broadside coupled from the adjacent signal layer. It is for this reason that orthogonal routing is recommended on adjacent signal layers (between planes) to minimize the coupling area.

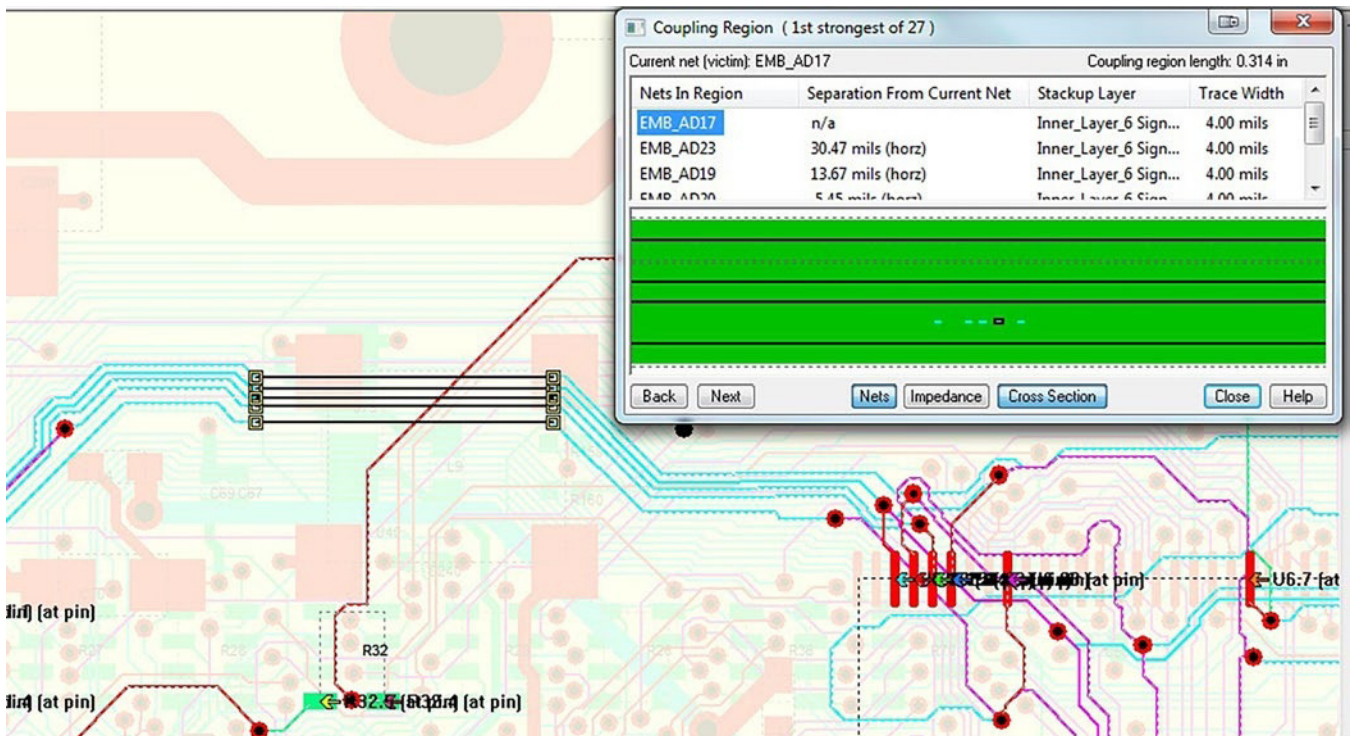


Figure 3: Crosstalk on long, parallel trace segments.

Flight times of the critical signals should be examined. One could compare the matched lengths of each signal, but the delay will vary depending on the meander pattern and stackup layer. Thus, it is important to match delays, not lengths (Figure 4).

Since all products must comply with strict electromagnetic compliance (EMC) regulations, all critical signals should be simulated to determine the amount of expected radiation. Don't let your project call for Plan B, which is basically disaster recovery.

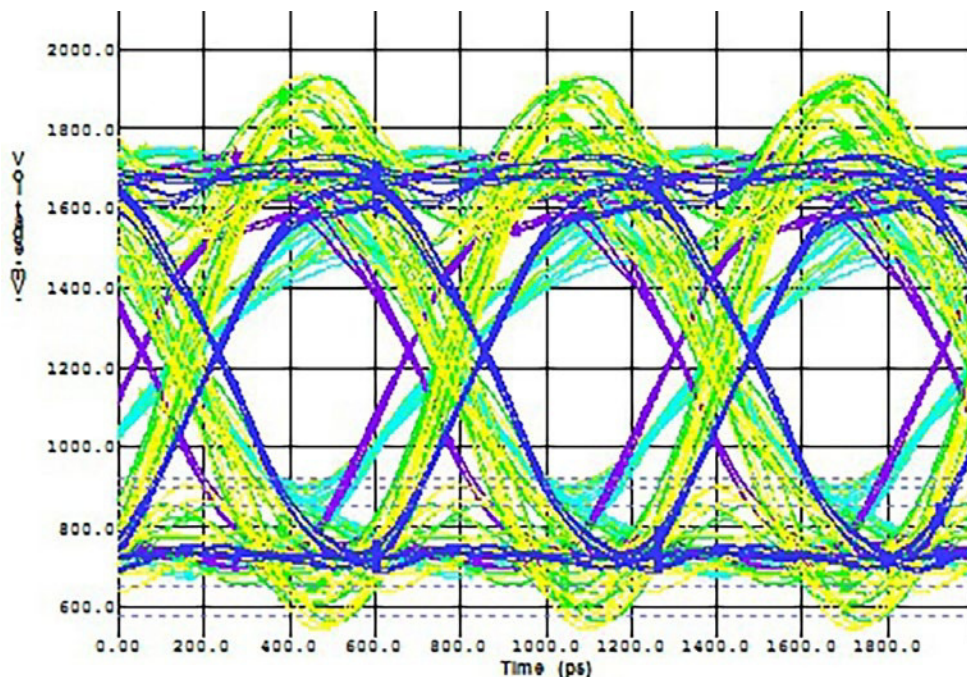


Figure 4: Skew of the clock to address, control, and command signals.

If, for instance, on the third iteration, your product still does not meet specifications, and management is pushing to have the project completed, then you may need to look for new employment opportunities. However, if simulation is done during the design process, then these re-spins can be avoided, keeping your project on budget and on schedule.

## Key Points

- The product life cycle is very short; therefore, time to market is of the essence
- Multilayer boards can be designed to work right the first time with little additional effort, providing you follow a tried and proven process
- Re-spins will continue to happen until designers make regular use of circuit simulation software
- Simulation is often engaged toward the end of the design cycle, which is too late
- Ideally, the simulation should be done during the design process as part of standard practice
- A pre-layout simulation identifies issues in the conceptual stage
- The post-layout simulation catches the issues during the design process, eliminating the potentially disastrous final stage changes
- Keep your eye on the ball during the entire design process, catching any small issue before it becomes a major problem
- Before starting a PCB design, you need to plan the PCB stackup and ensure that the selected substrate materials are available from your chosen fabricator
- If you use the same materials that the fab shop stocks to build your stackup, then the impedance will be more accurate
- The design of the PDN is also a very important part of the conceptual design process, ensuring that you have a stable power delivery system

- Decoupling and bypass capacitors supply instantaneous current at different frequencies to the drivers until the power supply can respond
- Decoupling capacitors also lower the impedance at different frequencies to help meet the AC impedance target
- PDN design is a trial-and-error process and needs to be done with the assistance of a PDN analysis tool
- If you have a simulation tool that is built into the PCB design software, then critical signals can be readily simulated by extracting the topology into the simulation environment
- Crosstalk is typically picked up on long parallel trace segments on the same layer but may also be broadside coupled from the adjacent layer
- One could compare the matched lengths of each signal, but the delay will vary depending on the meander pattern and stackup layer. Thus, it is important to match delays, not lengths **DESIGN007**

## Further Reading

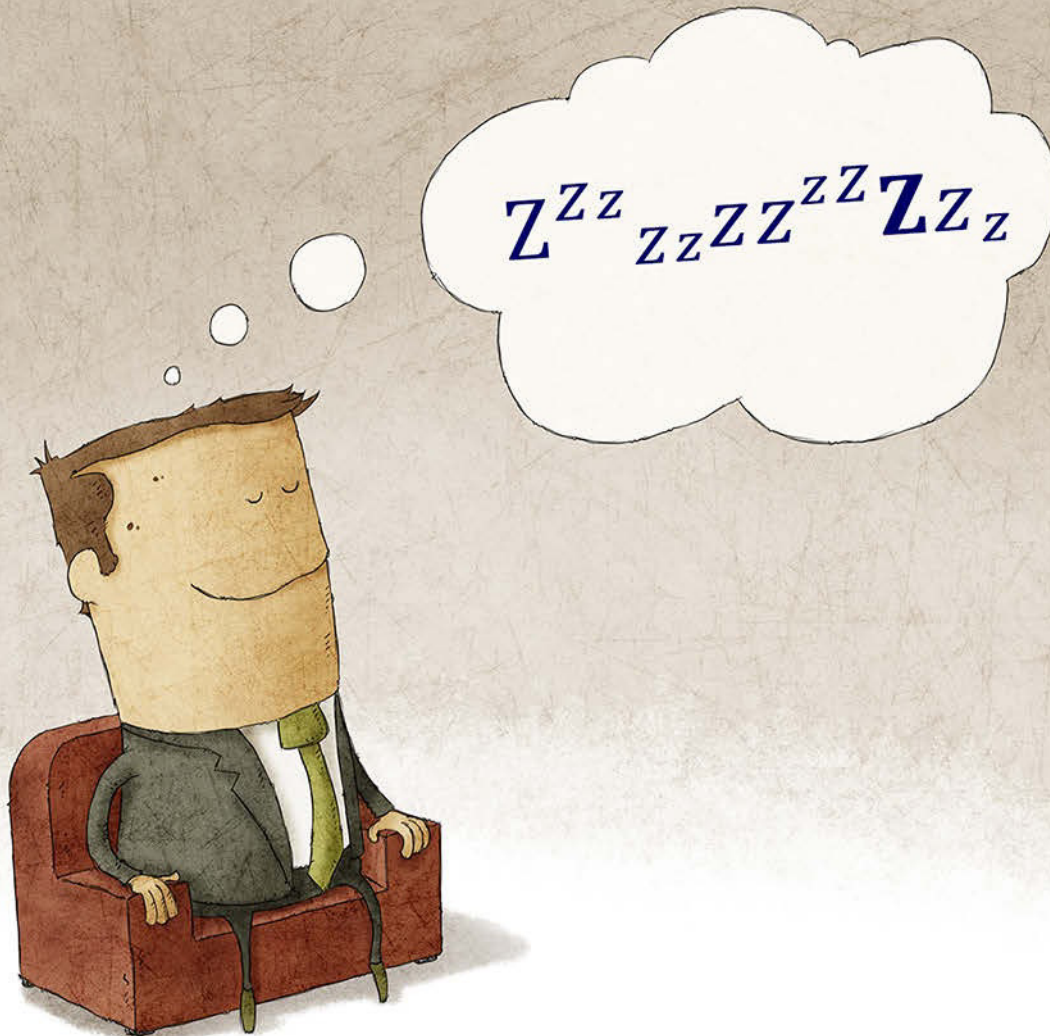
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- B. Olney, "Beyond Design: Board-Level Simulation and the Design Process: Plan B—Post-Layout Simulation," *The PCB Magazine*, February 2012.
- B. Olney, "Board-Level Simulation," *Electronics News*, Australia, February 2013.



**Barry Olney** is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD

Stackup, PDN, and CPW Planner. The software can be downloaded at [icd.com.au](http://icd.com.au). To read past columns or contact Olney, [click here](#).

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- Power Distribution Network impedance

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– Barry Olney

