Key SI Considerations for High-speed PCB Design

Beyond Design

by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

Over the past two decades, I've simulated numerous complex, high-speed designs for customers creating computer-based products. In addition, I've conducted signal integrity software training courses and led classes on high-speed design. In this month's column, I will reflect on the key considerations for achieving a successful high-speed PCB design that performs reliably, and I'll highlight some of the common signal integrity issues that I frequently encounter.

Arguably, the most critical factor in high-speed PCB design is the impedance of the interconnect. We know that transmission line drivers must be matched to the impedance of the line for the perfect transfer of energy. Energy is never lost but rather transforms into other forms of energy. Specifically, for an unmatched transmission line, energy can be transferred into heat, coupled into adjacent elements, reflected, or radiated—all of which should be avoided.

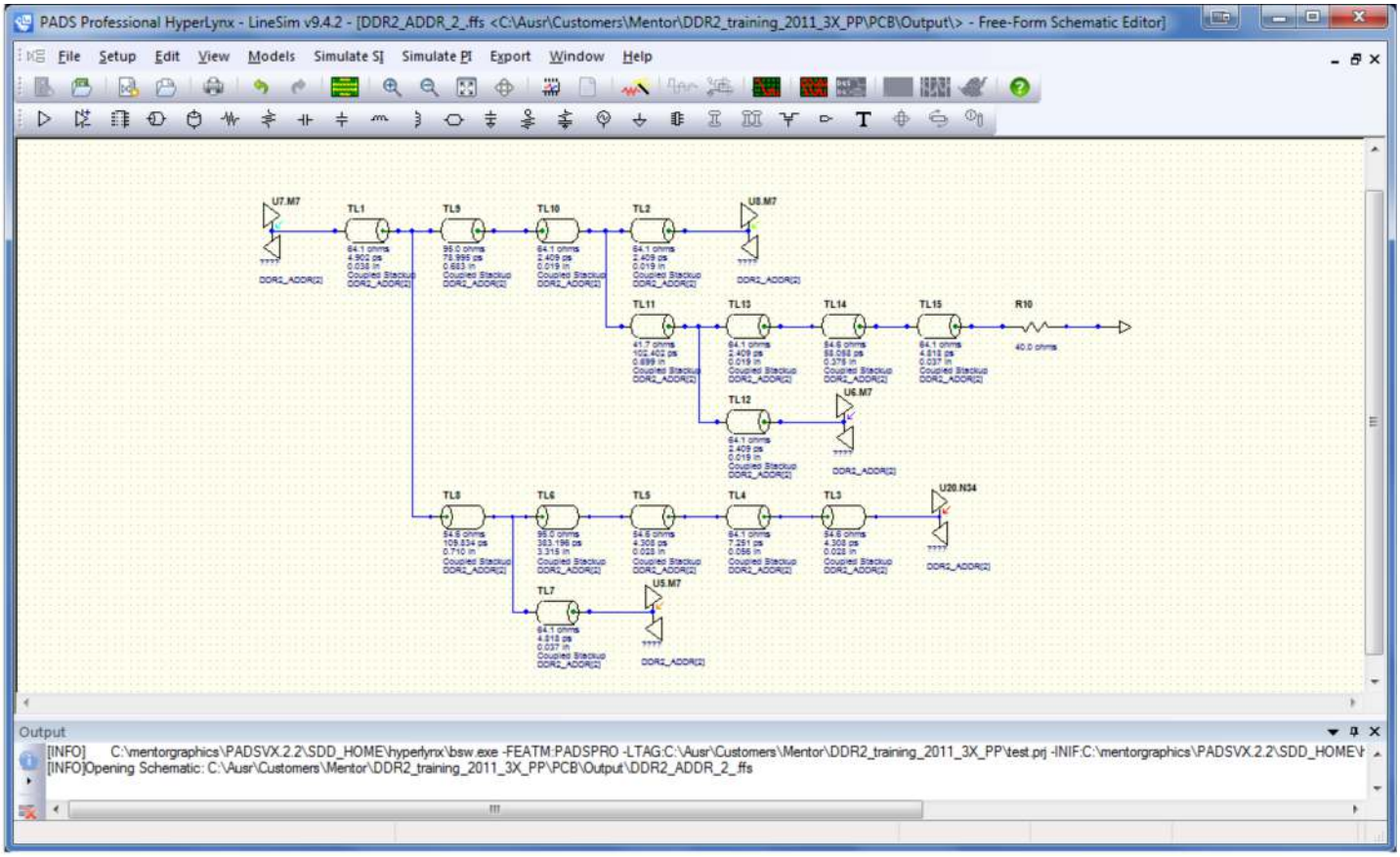


Figure 1: Free-form schematic model of a DDR address signal (simulated in HyperLynx).

Impedance is at the core of the methodology that is used to solve signal integrity issues. If you extract the interconnect topology (Figure 1) from a PCB layout to a free-form schematic model, the result can be terrifying—not quite that simple DDR address trace that was routed. In this case, any of the 15 individual transmission lines that form just one DDR signal interconnect can create issues if incorrectly routed.

In source-synchronous interfaces like DDR memory, it's crucial for data signals to reach the load simultaneously with the data strobe. This synchronization is achieved by matching the delays of all signals between data lanes and strobes within a certain tolerance. While address and command signals are also matched to the clock, they have a less stringent tolerance. However, matching the lengths doesn't ensure uniform propagation delay for each signal. Traces routed to equal lengths on different layers exhibit different delays, especially when comparing microstrip (outer layers) to stripline (inner layers), due to the differing dielectric materials (including air) surrounding the traces. Hence, buses and associated control signals should all be routed on the same layer or a symmetric layer of the stackup. However, if they are routed on different layers then they must be routed to matched delay.

Typically, serpentine traces (or meander lines) are used to match the length of these critical signals, assuming that the extra length of the serpentine pattern will be electrically the same as a straight trace and no parasitics are introduced. But as technology advances and demands for smaller traces with less clearance and faster rise times become more the norm, this assumption may no longer be valid. Contrary to what you may believe, the propagation delay of a serpentine trace is less than the delay through an equivalent-length straight trace. The meandering signal is sped up because a portion of the signal will propagate perpendicular to the serpentine. This also varies with the type of serpentine pattern used. For instance, the "switch-back" serpentine pattern may

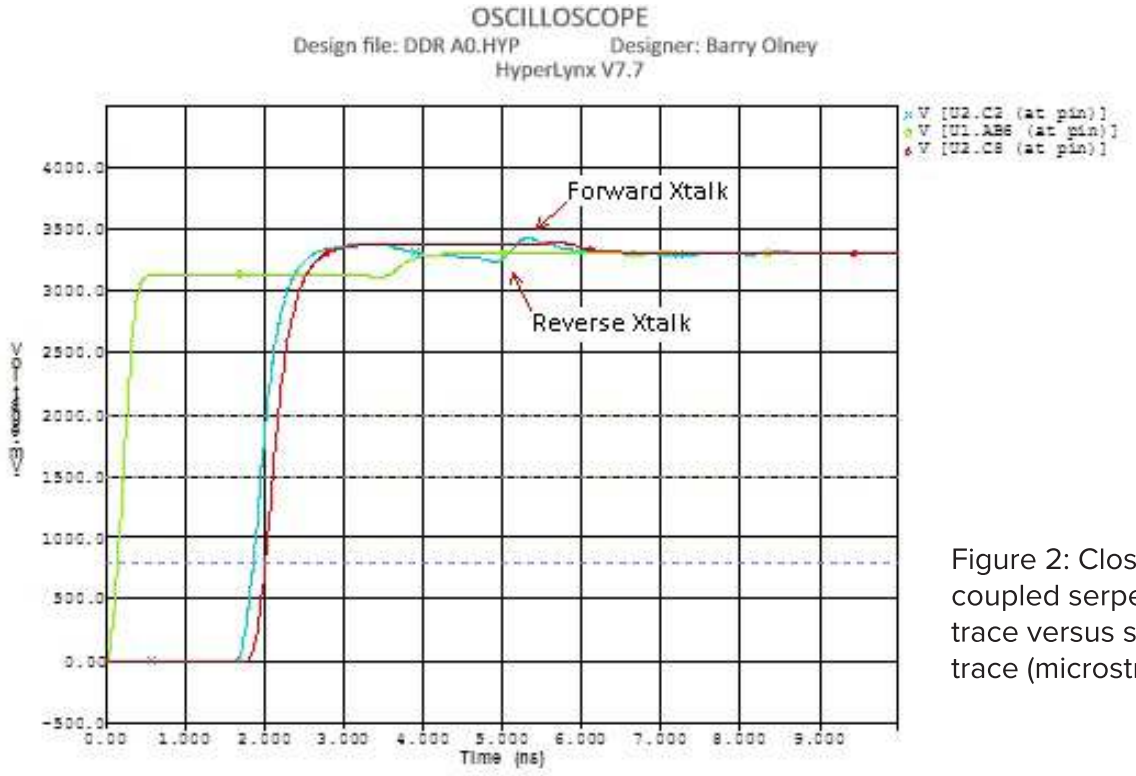


Figure 2: Closely coupled serpentine trace versus straight trace (microstrip).

feature long parallel segments spaced closely together causing multiple instances of signal coupling throughout the serpentine pattern. This self-coupling, involving both forward and reverse crosstalk, effectively shortens the electrical path.

In Figure 2, the green waveform is the driver. Red is the straight (reference) trace. Blue is the serpentine trace which leads the reference trace by 150 ps despite being the same length. The peak and trough in the blue serpentine trace (between 4 to 6 ns) are the reverse and forward crosstalk, respectively, from the close segment coupling. In this case, matching the delay of the traces may not be sufficient and the resultant overall delay of 150 ps may not be within margins.

Clock delay is another common issue I encounter regularly. The clock (or strobe) signal in source-synchronous interfaces should have the longest delay within the bus group. Synchronous interfaces are uniquely immune to crosstalk, provided the data signals are clocked after they have settled—during the hold time. However, if the clock delay is shorter than the data signal delay, it may sync during the setup time and crosstalk may arise. Route the clock/strobe last to ensure it is the longest trace.

Ground pours can also affect the impedance of a critical trace. Some PCB designers do this habitually, claiming various reasons for its use. Additionally, many reference designs provided by chip manufacturers employ this ground pour technique. However, placing a copper

Figure 3: Symmetric coplanar waveguide with ground plane (simulated in iCD CPW Planner).

pour on one or both sides of a trace effectively creates a coplanar waveguide, which can reduce the impedance at the coupling point on the trace.

If a standalone trace is routed to 60 Ω, the difference in impedance for the scenario of creating a coplanar waveguide represents a maximum variation of 9.2% in Zo (Figure 3):

Standalone trace: Zo = 60 Ω
Ground pour on both sides: Zo = 55.26 Ω

Ground pours may be effective on high-impedance, analog two-layer boards but do not significantly reduce crosstalk on low-impedance digital multilayer boards since the traces are closely coupled to the plane. Also, ground pours have the disadvantage of altering the impedance of traces that run adjacent to a ground pour area, causing reflections, and are therefore not recommended for use in the digital domain. 500 µm (20 mil) spacing should be used to avoid this issue.

High-speed PCB design is not as simple as sending a signal from the driver to the receiver over a transmission line. One should also consider the presence and interaction of the power distribution network (PDN) and how and where the return displacement current flows. A logic schematic diagram masks details crucial to the operation of unintentional signal pathways vital to the understanding of signal performance, crosstalk, and electromagnetic emissions. The PCB designer needs to be able to visualize the connectivity of the return current flow in order to avoid large loop areas that increase series inductance, degrade signal integrity, and elevate crosstalk and electromagnetic radiation.

Ground impedance is the root cause of nearly all signal and power integrity issues; maintaining low ground impedance is essential for both. While a continuous ground reference plane effectively achieves this, it becomes more challenging with the addition of plane layers in a multilayer PCB. A ground plane serves as a reliable signal return, provided it remains continuous under the signal path.

One must also understand the importance of referencing and how to control the return displacement current flow of a signal. Each signal layer should be adjacent to, and closely coupled to, a reference plane, which creates a clear, uninterrupted return path. As the layer count increases, this concept becomes easier to implement but decisions regarding return current paths become more challenging.

The return current of a high-speed, fast-rise time digital signal will always follow the path of least inductance which is directly beneath the signal path. However, discontinuities tend to divert the return current, increasing the loop area, inductance, and delay, which is not desirable. The best way to identify the discontinui-

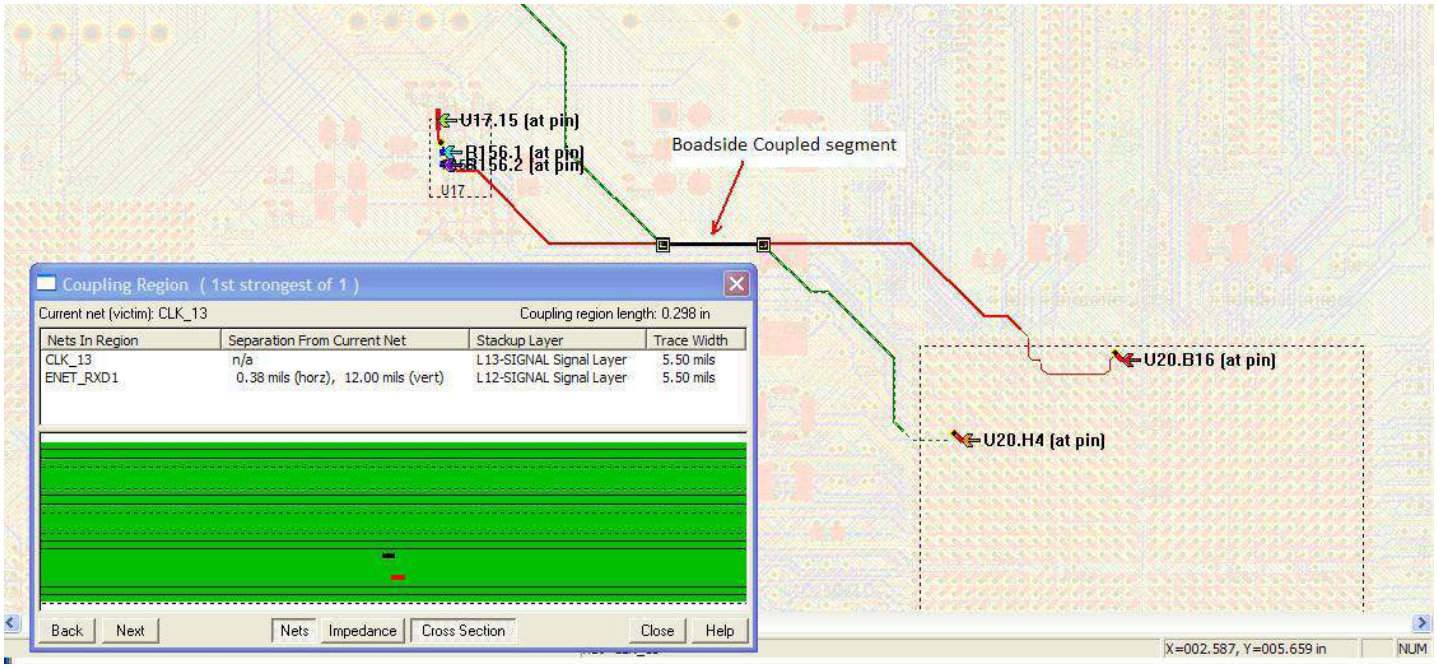


Figure 4: Broadside coupled crosstalk (simulated in HyperLynx).

ties is to follow the signal path and imagine the return path closely coupled on the nearest plane. If there are multiple planes present in the layer stack, then the displacement current will still take the path of least inductance and follow closely coupled to the signal trace. If a discontinuity interrupts this return flow, then the return current will be forced into a distant plane where it has a clear run creating increased inductance.

Crosstalk can occur either between traces on the same layer or through broadside coupling between traces on adjacent layers (Figure 4). This coupling is three-dimensional. Broadside coupling is harder to detect (particularly on built-up outer layers) because we typically focus on trace clearances when assessing crosstalk, but a simulator can identify this issue. Traces routed in parallel and broadside experience more crosstalk than those routed side-by-side due to the larger coupling area and tighter spacing. Hence, it's good practice to route adjacent signal layers orthogonally to each other in the stackup to minimize the coupling region.

When performing interactive routing, PCB designers often group signals for aesthetic reasons, showcasing their artistic side. However, while this might look tidy and organized, it might not yield the best performance. Beyond the previously discussed synchronous buses, it is advisable to space unrelated critical trace segments by three times the trace width, if possible. Alternatively, if real estate is limited, the trace-to-plane height in the stackup can be reduced to increase coupling.

High-speed PCB design involves many considerations to ensure reliable performance and signal integrity. Impedance matching remains the core of solving signal integrity issues. By focusing on these critical considerations, PCB designers can create successful high-speed designs that meet the demands of modern technology and perform reliably.

"High-speed PCB design involves many considerations to ensure reliable performance and signal integrity."

Key Points

- The most critical factor in high-speed PCB design is the impedance of the interconnect.
- Impedance is at the core of the methodology that is used to solve signal integrity issues.
- Traces routed to equal lengths on different layers exhibit different delays.

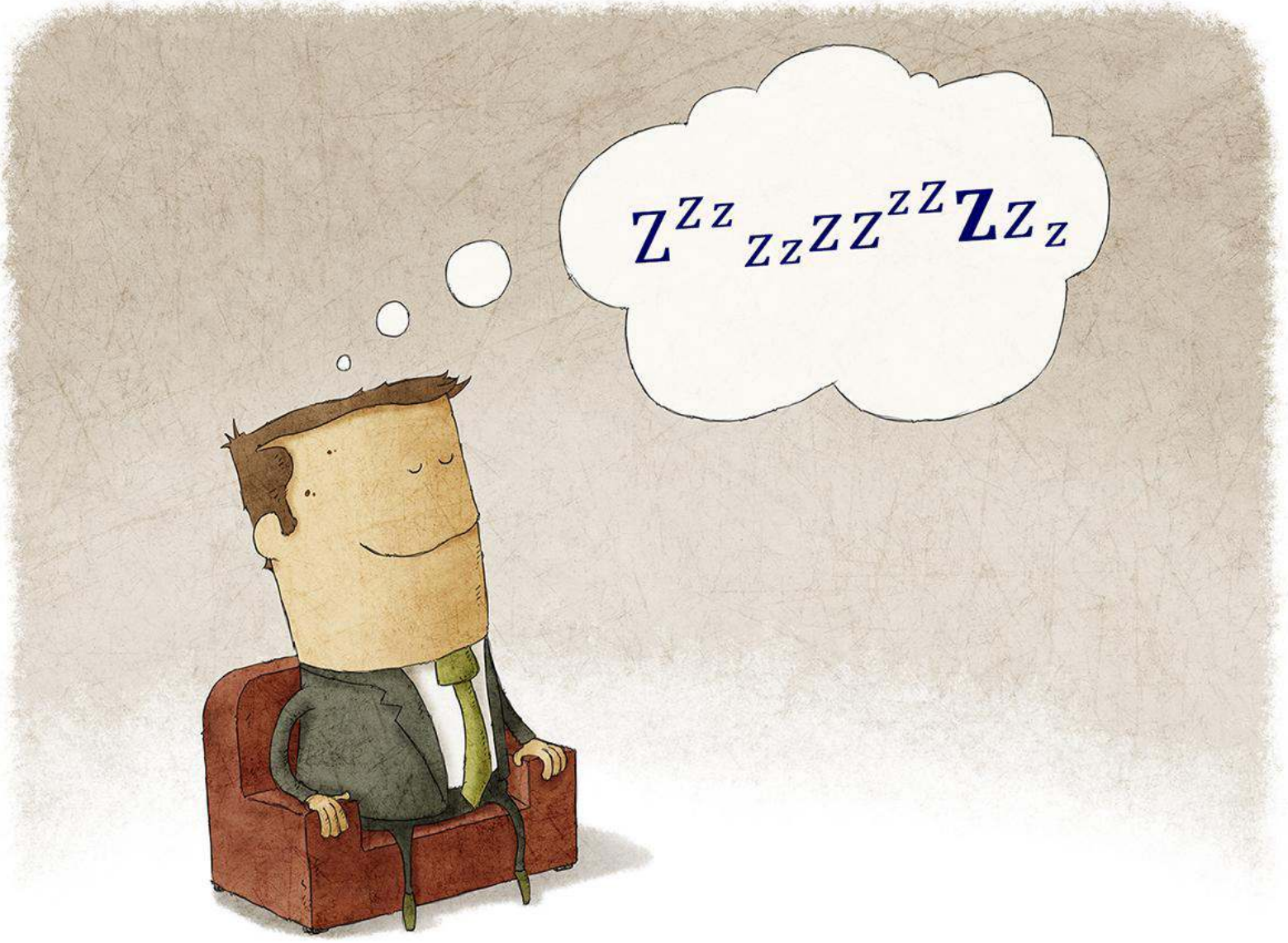
- Buses and associated control signals should all be routed on the same layer or a symmetric layer of the stackup. However, if they are routed on different layers then they must be routed to matched delay.
- The propagation delay of a serpentine trace is less than the delay through an equivalent-length straight trace.
- The clock (or strobe) signal in source synchronous interfaces should have the longest delay within the bus group.
- Placing a copper pour on one or both sides of a trace effectively creates a coplanar waveguide, which can reduce the impedance at the coupling point on the trace.
- Ground pours may be effective on high-impedance analog two-layer boards but do not significantly reduce crosstalk on low-impedance digital multilayer boards since the traces are closely coupled to the plane.
- The PCB designer needs to be able to visualize the connectivity of the return current flow to avoid large loop areas that increase series inductance.
- Each signal layer should be adjacent to, and closely coupled to, a reference plane, which creates a clear, uninterrupted return path.
- Discontinuities tend to divert the return current increasing the loop area, inductance and delay.
- Crosstalk can occur either between traces on the same layer or through broadside coupling between traces on adjacent layers.
- Broadside coupling is harder to detect because we typically focus on trace clearances.
- Traces routed in parallel and broadside experience more crosstalk than those routed side-by-side due to the larger coupling area and tighter spacing.
- Route adjacent signal layers orthogonally to each other in the stackup to minimize the coupling region.
- Space unrelated critical trace segments by three times the trace width. **DESIGN007**

Resources

Beyond Design columns by Barry Olney: "Interconnect Impedance," "To Pour or Not to Pour," "Return Path Optimization"

Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded at www. icd.com.au. To read past columns, click here.

We DREAM Impedance!



Did you know that two seemingly unrelated concepts are the foundation of a product's performance and reliability?

- Transmission line impedance and
- Power Distribution Network impedance

DISCOVER MORE

iCD software quickly and accurately analyzes impedance so you can sleep at night.

iCD Design Integrity: Intuitive software for high-speed PCB design.

"iCD Design Integrity software features a myriad of functionality specifically developed for PCB designers."
– Barry Olney

iCD
In-Circuit Design Pty Ltd

www.icd.com.au