# Slaying Signal Integrity Villains

**by Barry Olney,** In-Circuit Design PTY LTD / Australia

**High-speed PCB design** is a balancing act, where subtle oversights can develop into major signal integrity nightmares. Some culprits lie dormant during early validation, only to reveal themselves later through workflow disruptions and elusive performance bottlenecks. Take crosstalk, for example. What begins as a stray signal coupling between traces can ripple through the design, ultimately destabilizing the power distribution network. Each of these troublemakers operates with signature tactics, but they also have well-known vulnerabilities. While it's often possible to track down the source after the fact, a proactive approach offers the greatest defense. In this month's column, I'll profile a lineup of common signal integrity offenders and explore proven techniques to eliminate

## The Terminator

He lurks in the shadows between layers or hides beneath the solder mask, disguised as a compliant transmission line. To the untrained eye, he appears well-behaved—clean geometry, acceptable tolerances—but underneath the surface, he's changing character from one edge to the next. This guy uses dielectric inconsistency, trace width and spacing variation, and via transitions to deviate impedance unpredictably. His signature tactic is reflection. He tosses mismatches back up the line, destabilizing receivers.

However, the Terminator isn't invincible. With vigilant stackup planning, disciplined fabrication, precise impedance modeling by field solvers, and well-placed terminations, he's cornered before he can strike. Because in high-speed design, certainty is a

The blueprint for strategic stackup planning:

1. Define performance requirements. Outline the single-ended and the differential pair requirements based on the technology used.
2. Choose dielectric materials wisely. Use materials with consistent Dk over the bandwidth. Choose a low-Dk and low-Df material for low loss between signal layers. Conversely, use a high-Dk and low-Df material between the closely coupled power planes to increase inter-plane capacitance.
3. Build the layer order intentionally. Top/bottom for components and routing fanout. Use coplanar waveguides on the outer layers for RF and SERDES design. Make adjacent layers reference planes (for clean return paths) and have internal signal layers nested between closely coupled planes to gain stripline advantages.
4. Determine series and/or parallel terminations to match the impedance and dampen reflections.

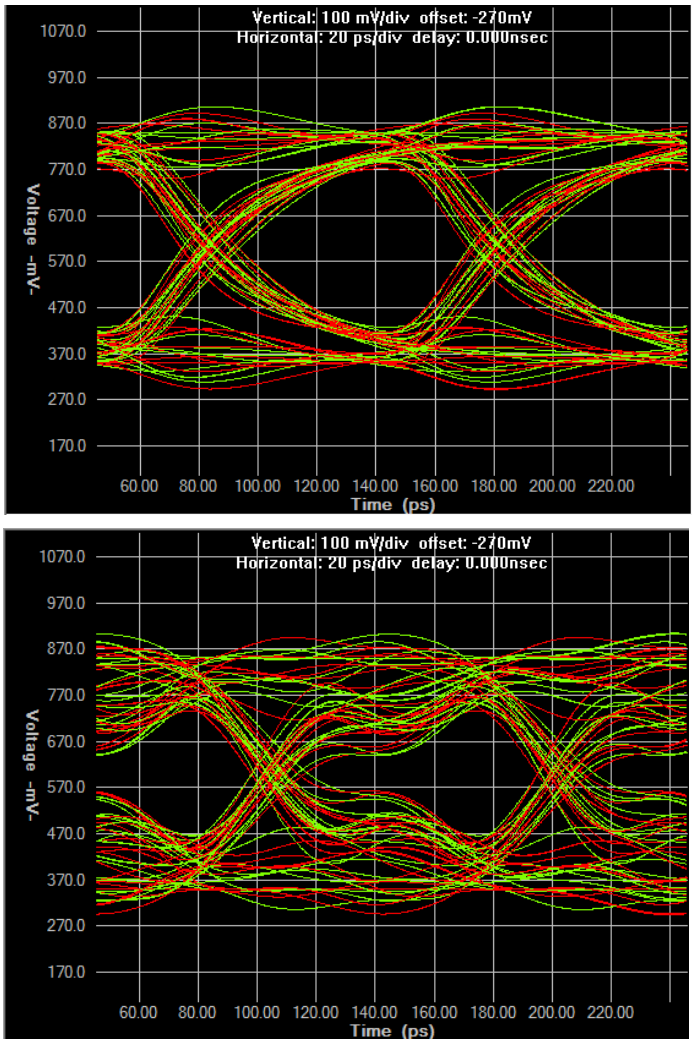
## The Via Vandal

He's the chaotic saboteur who punches holes through return paths and loves messing with impedance. He creates stubs, disrupts signal flow, and throws your reference planes into disarray. He injects a propagating wave into the cavity, which can excite the cavity resonances. Other signal vias, also passing through this cavity, can pick up this transient voltage as crosstalk, and when the wave meets the PCB edge, the two reference planes form a slot antenna that will radiate noise with the potential to generate electromagnetic interference (EMI) to nearby equipment. The more switching signals that pass through the cavity, the more noise is induced into other signals. He affects vias all over the cavity. Treating the plane pair as a radial transmission line and terminating it in its characteristic impedance can suppress reflections and standing waves.

A region under a large BGA densely populated with vias also appears as a discontinuity because of the large array of antipads eating a hole in the plane. A discontinuity reflects propagating energy because it represents a mismatch with the characteristic impedance of the transmission line. To open up planes under BGAs, use via-in-pad, shrink the antipad diameter, and use teardrops to offset antipads.

Dangling via stubs can distort signals passing through an interconnect and also decrease the usable bandwidth of the signal. Vias can add jitter and reduce eye openings (Figure 1), which can cause data to be misinterpreted by the receiver. Length is the primary factor that influences the inductance of the via, which depends on the design complexity, the number of layers, and hence the overall PCB thickness.

To neutralize the Via Vandal, you have two tactical options: back-drill the plating (Figure 2) to remove the residual stub, or—far more effective—route the signal through the full length of the via barrel, leaving no stub or minimal stub to exploit. By eliminating unused segments, you shut down his favorite hiding spot and keep reflections at bay.




▲ **Figure 1: Through via signal (top) and stub on via (bottom).**

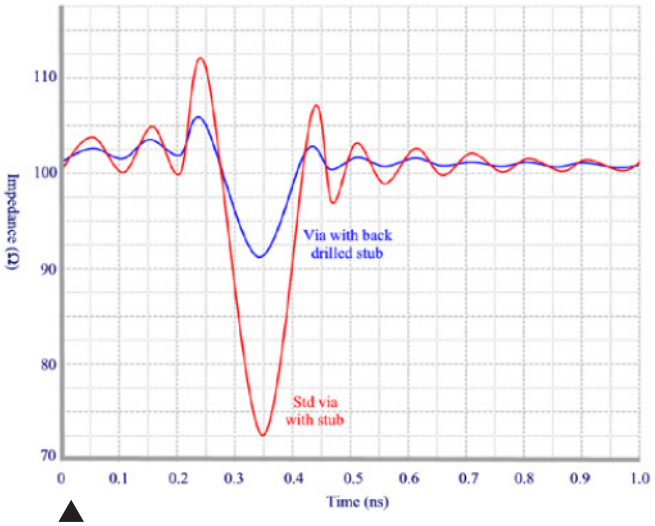



Figure 2: Differential 100Ω via with stub (red) versus via with back-drilled stub (blue).

## The Crosstalk Bug

This guy is a parasite and unpredictable. He thrives in overcrowded routing lanes and feeds off concealed coupling zones. He induces unwanted electromagnetic interaction between adjacent trace segments, resulting in noise, false triggering, degraded timing margins, and jitter. He leverages fast rise times to magnify interference. He loves a fast signal, and he tampers with balance by skewing one leg of the differential pair, undermining common-mode cancellation. He gets in through tight trace spacing on long parallel runs with poor reference plane structure and inadequate shielding or stitching vias, and exploits oversights in the termination strategy.

The Crosstalk Bug may be elusive, but he's far from invincible:

1. **Spacing is the defense:** Increase separation between critical traces, especially single-ended nets. Alternatively, tightly couple the signal to the reference plane.

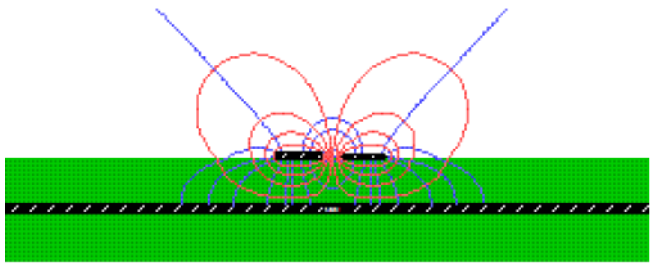


Figure 3: Crosstalk on the outer (microstrip) layer.

2. **Stackup strategy:** Use stripline routing where possible to shield signals with reference planes above and below.
3. **Stagger routing layers:** Avoid running parallel nets across adjacent layers. Rotate orientation (e.g., vertical on Layer 3, horizontal on Layer 4).
4. **Guard traces:** Place grounded traces between aggressors and victims. Stitch them with GND vias for continuity.
5. **Controlled edge rates:** Skew rate control minimizes high-frequency content.
6. **Simulation and modeling:** Use signal integrity tools to identify high-risk areas before layout lockdown.

## The Parasitic Phantom

Meet the unsung menace of the high-speed design domain—a spectral saboteur that clings to circuits and drains performance one subtle swerve at a time. He doesn't shout; he whispers through stray fields and forgotten pads. He hijacks energy by exploiting unintended capacitance and inductance in the layout, lurking in via stubs, oversized pads, split planes, and isolated copper.

Residual via stubs act as open-ended antennas, storing and releasing energy that wreaks havoc on signal integrity. Copper pours disconnected from return paths become floating traps for electric fields. Misplaced or excessive capacitors create unpredictable resonance, turning power distribution into a disarray of impedance spikes. He dwells near trace edges where fringe fields are strongest, feeding off loosely controlled geometry. He hides under BGA fan-outs with unterminated stubs, in unused layers with leftover copper, beneath mismatched pad stacks and antipads, and around split plane edges where return currents skirmish.

Defenses and banishment tactics against the Phantom:

1. **Stub removal:** Back-drill the via stub or eliminate dangling stubs.
2. **Plane continuity:** Maintain consistent reference planes beneath critical signals. Avoid splits or gaps.
3. **Copper sanitation:** Tie unused zones to ground or eliminate entirely.

4. **Stackup harmonization:** Align power and ground layers to suppress resonance and maximize interplane capacitance.
5. **Simulate the Phantoms:** Use 3D field solvers to visualize and quantify his lurking influence. No Phantom survives scrutiny.

## The Return Path Renegade

He's daring, reckless, and electromagnetic by nature. He thrives in fractured reference planes, where continuity is broken and chaos reigns. When high-speed electromagnetic signals traverse these voids or splits, he severs the clean path of return currents, forcing them to detour through unintended loops, increasing inductance, radiating noise, and stirring up EMI. He leaves a wake of interference that can couple into nearby circuitry or radiate outward through enclosures, and he especially loves tampering with clean reference paths under high-speed clock signals, leading to jitter and instability.

His favorite hideouts are large BGAs with broken plane continuity, layer transitions where ground/power is not mirrored, power islands with isolated copper and signal routing over plane voids, or anti-pads without thought to the return current path.

You don't just fence him in; you give the return currents a highway back home:

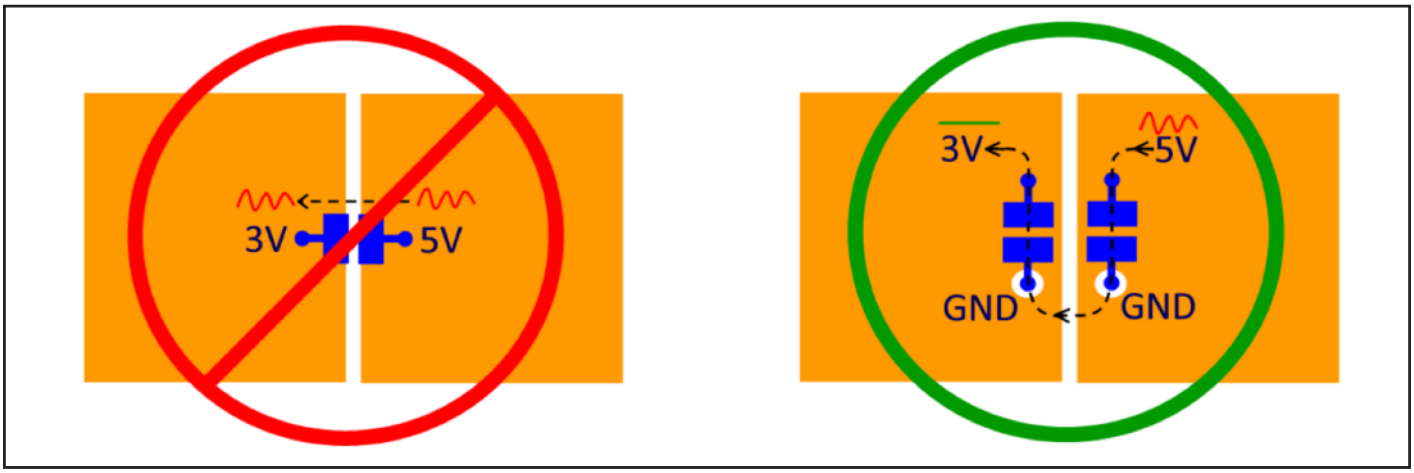
- **Planes that span:** Use continuous ground/power planes beneath critical signals, especially clocks and data lines.
- **Stitching vias:** Add ground vias near every plane transition or add decaps to each power plane near the transition (Figure 4). Create a clear path for return currents to flow smoothly.
- **Signal-plane alignment:** Route differential pairs and high-speed signals over solid reference plane pairs. No splits, no gaps.
- **Plane pair matching:** Layer stackups with matched plane pairs reduce impedance variation, increase bypass capacitance, and minimize detours.
- **Simulation sweep:** Visualize return current density with EM solvers to expose hidden risks.

## The Lord of Latency

He corrupts a signal traveling at nearly half the speed of light, stretching signal paths with invisible tendrils of dielectric sludge, causing skew between data lines and violating setup/hold times with malicious precision. He lurks in the depths of multilayer stackups, sowing chaos by delaying critical data and disrupting synchronous harmony. He feeds on high-Dk materials like FR-4, slowing signal velocity. The greater the dielectric constant, the stronger his grip. Only low-Dk laminates can weaken his influence. He coils signal paths into serpentine traces, stretching them across the board. In DDR buses, he thrives on mismatched delays, sowing chaos through skew and timing violations. Dielectric and conductor losses amplify his power, dragging signals into the abyss of latency.

Every component becomes a pawn in his delay game. He stacks intrinsic delays like dominoes, toppling timing margins with ease. He fractures parallel signals, mis-aligning their arrival and breaking synchronous harmony, and he distorts waveforms, combining delay with reflections and attenuation to wreak havoc.

▼ **Figure 4: Decaps provide a clear return path for power plane transitions.**



Mitigation tactics against latency:

- **Material mastery:** Deploy low-Dk laminates to accelerate signal velocity and weaken his dielectric grip.
- **Trace discipline:** Match trace delays with ruthless accuracy, especially in differential pairs and timing-critical buses, to sever his serpentine influence.
- **Geometry control:** Select transmission line formats (stripline, CPW) with strategic intent, balancing shielding and delay to neutralize his geometric traps.
- **Route symmetry:** Deploy critical synchronous buses (like DDR) across perfectly mirrored layers. This symmetrical routing forms an impenetrable barrier, ensuring impedance uniformity and denying him the imbalance he feeds on.
- **Predictive modeling:** Use field solvers and simulation tools to expose hidden delay paths and preempt his interference before layout lockdown.

## Key Points

- It's often possible to track down the source after the fact; however, a proactive approach offers the greatest defense.
- With vigilant stackup planning, disciplined fabrication, precise impedance modeling by field solvers, and well-placed terminations, you can corner the Terminator before he can strike.
- Switching signals that pass through the cavity induce noise into other signals. Treating the plane pair as a radial transmission line and terminating it in its characteristic impedance can suppress reflections and standing waves.
- A region under a large BGA densely populated with vias also appears as a discontinuity because of the large array of anti-pads eating a hole in the plane. To open up planes under BGAs, use via-in-pad, shrink the antipad diameter, and use teardrops to offset antipads.
- Dangling via stubs can distort signals passing through an interconnect and also decrease the usable bandwidth of the signal. Back-drill the plating to remove the residual stub, or route the signal through the full length of the via barrel.

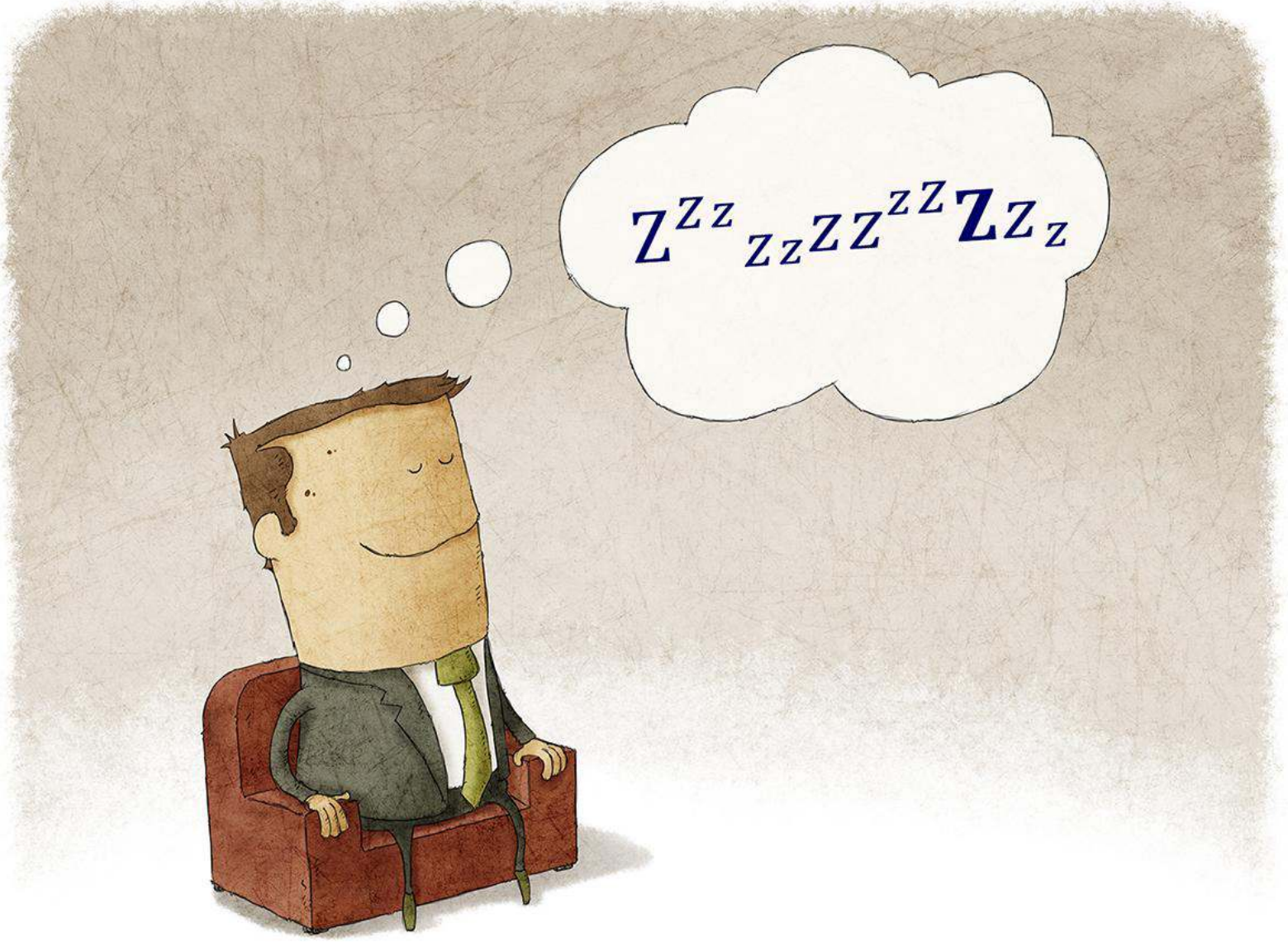

- Spacing is the best defense against crosstalk. Increase the separation between critical traces. Alternatively, tightly couple the signal to the reference plane.
- Maintain consistent reference planes beneath critical signals; avoid splits or gaps. Tie unused zones to ground or eliminate them.
- Add ground vias near every plane transition or add decaps to each power plane near the transition. Create a clear path for return currents to flow smoothly.
- Match trace delays with ruthless accuracy, especially in differential pairs and timing-critical buses.
- Deploy critical synchronous buses (like DDR) across perfectly mirrored layers. **DESIGN007**

***Resources***

1. "Beyond Design: Standing Waves in Multilayer PCB Plane Cavities", by Barry Olney.
2. "Beyond Design: How to Handle the Dreaded Danglers Part 1", by Barry Olney.
3. "Beyond Design: How to Handle the Dreaded Danglers Part 2", by Barry Olney.
4. "Beyond Design: Dampening Plane Resonance with Termination", by Barry Olney.

**Barry Olney** is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software, incorporating the iCD Stackup, PDN, and CPW Planner. You can download the software at www.icd.com.au. To read past columns, click here.

# We DREAM Impedance!




Did you know that two seemingly unrelated concepts are the foundation of a product's performance and reliability?

- Transmission line impedance and
- Power Distribution Network impedance

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