# Beyond Design - Signal Integrity Part 2 of 3

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In last month's column, I looked at how advanced IC fabrication techniques have created havoc with signal quality and radiated emissions. Part 2, of Signal Integrity, will cover the effects of crosstalk, timing and skew on signal quality.

**Crosstalk**

Crosstalk is the unintentional electromagnetic coupling between traces on a PCB. But crosstalk can also be induced in the return path–which often gets overlooked. Figure 1 shows the crosstalk associated with two parallel trace segments on the outer (microstrip) layer of a PCB.

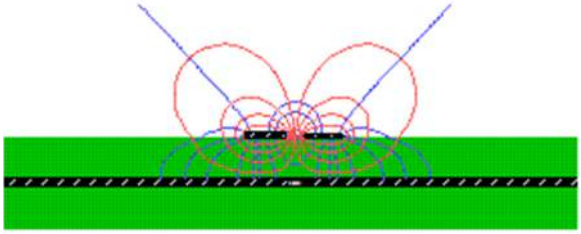

Figure 1 – Crosstalk on the outer (microstrip) layer

The red lines represent the magnetic field that couples voltage inductively to the nearby trace and also radiates electromagnetic emissions. The blue lines are electric fields that capacitively couple current into the nearby trace and are somewhat absorbed by the plane but still tend to radiate noise outward.

Crosstalk can be coupled trace-to-trace, on the same layer, or can be broadside coupled by traces on adjacent layers. The coupling is three dimensional. Broadside coupling is difficult to spot as generally we look for trace clearances, on the same layer, when evaluating crosstalk but a simulator will pick this up. Traces routed in parallel and broadside cause greater amounts of crosstalk than those routed side by side. This is due to the width of the trace being much larger that the thickness – so more coupling occurs in the broadside configuration. It is therefore good practice to route adjacent signal layers, in the stackup, orthogonally to each other to minimize the coupling region. A better solution is to only have one signal layer between two planes to totally avoid broadside coupling altogether.

Also, these days many stackups use a buildup microstrip layer top and bottom of the board. This can be very dangerous as one needs to take particular care of traces routed on the adjacent layers.

UNITS: mil | 8/21/2014 | Total Board Thickness: 69.4 mil

Differential Pairs > 50/100 ohm

| Layer No. | Via Span & Hole Diameter | Description | Layer Name | Material Type | Dielectric Constant | Dielectric Thickness | Copper Thickness | Trace Clearance | Trace Width | Current (Amps) | Characteristic Impedance (Zo) | Edge Coupled Differential (Zdiff) | Broadside Coupled Differential (Zdbs) | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Soldermask | | Dielectric | 3.3 | 0.7 | | | | | | | | |
| 1 | 8 4 8 | Signal | Top | Conductive | | | 2.2 | 10 | 5.5 | 0.55 | 70.13 | 121.81 | | Surface Traces & Pads |
| | | Prepreg | | Dielectric | 3.7 | 3.4 | | | | | | | | |
| 2 | | Signal | Inner 2 | Conductive | | | 0.6 | 10 | 4.5 | 0.18 | 53.5 | 99.23 | | Buried Microstrip |
| | | Core | | Dielectric | 3.6 | 3 | | | | | | | | |
| 3 | | Plane | GND | Conductive | | | 0.6 | | | | | | | |

Figure 2 – layers 1 and 2 have only 3.4mil separation and are prone to coupling

Since crosstalk is induced by one or more aggressors onto a victim trace, it is obvious that the higher the aggressor voltage the more crosstalk will be induced. It is therefore best to segregate groups of nets according to their signal amplitude. This strategy prevents larger voltage nets (3.3V) from affecting smaller voltage nets (1.5V).

 

Crosstalk is defined by:

$$Xtalk = \frac{1}{1 + (\frac{D}{H})^2}$$

The above equation clearly shows that in order to reduce crosstalk, we need to minimize H (height above the plane) and maximize D (distance between traces). The easiest way to reduce crosstalk, from a nearby aggressor signal, is of course by increasing the spacing between the signals in question. Crosstalk falls off very rapidly with distance. Crosstalk plummets roughly quadratically with increased separation. Doubling the spacing cuts the crosstalk to roughly a quarter of its original level.

**Rule of Thumb:** Gap = 3 x trace width.

However in today's complex, dense designs, it is not always possible to use up valuable real estate to satisfy the above. An alternative is to set up parallel segment rules to prevent traces running in parallel for more than 500mils. Also, the effect of dielectric height above a reference plane on trace-to-trace coupling plays an important role in reducing the crosstalk. A 3mil thickness dielectric material reduces the crosstalk by approximately a quarter, compared to the 6mil, given the same trace spacing.

**Rule of Thumb:** Couple the signal traces closely to the plane.

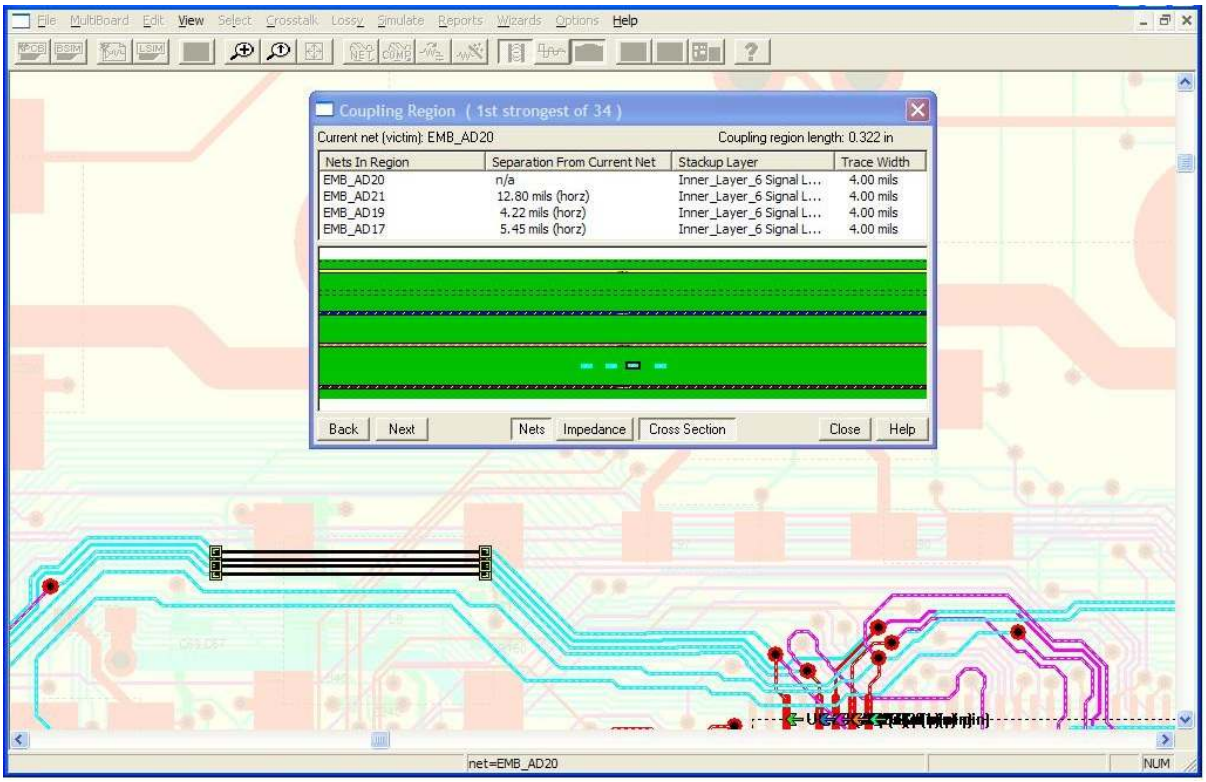


Figure 3 – Crosstalk on long parallel trace segments

Crosstalk is typically picked up on long parallel trace segments. These can be on the same layer as in Figure 3, but may also be broadside coupled from the adjacent layer. It is for this reason that orthogonal routing is recommended on adjacent layers (between planes) to minimize the coupling area. This will not occur with the stackup illustrated in Figure 3 of Part 1, because there is only one signal layer between the planes – so this is very safe as far as broadside crosstalk is concerned.

 

**Timing and Skew**

Flight time delay and skew are key pillars in high-speed PCB design signal integrity. One of the driving factors for flight time and skew performance is the placement of components. Maximum placement refers to the placement in which the distances between the devices are the maximum distance permitted. Controlling the maximum placement of devices, combined with the assumption that good general design practices are adhered to, limits maximum trace delay to roughly the longest Manhattan distance of the signals contained in a specific clock domain.

Why the longest Manhattan distance? This is due to skew matching requirements: all of the shorter nets in a clock domain must be lengthened to skew match to the longest run length. Therefore, flight time and skew—for an entire clock domain—are governed by the maximum placement, along with the routing rules that constrain the matching of the trace lengths.

In the classic high-speed design flow, timing specifications simulation results are compared to determine placement and routing constraints. Given a length constraint, a designer can control signal integrity by controlling the PCB trace topology of the various parts of an interface. Included in this topology are any terminations.

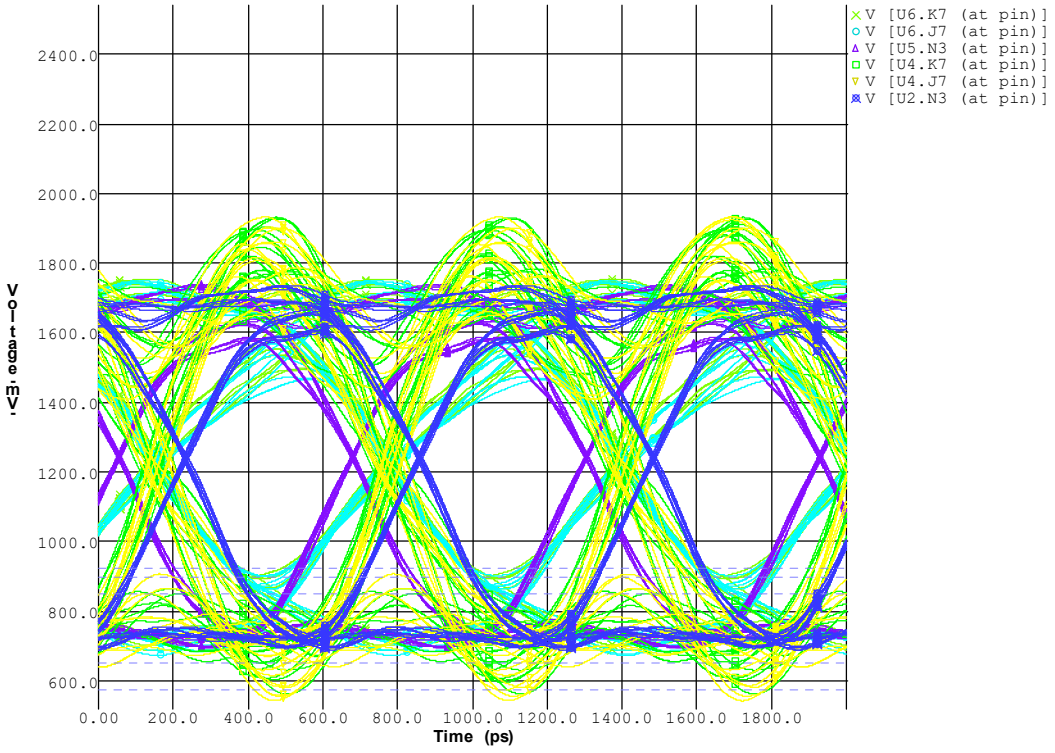


Figure 4 – Skew of clock to address, control and command signals of DDR3 memory

Figure 4 illustrates the timing of the clock compared to the address, control and command signals of a DRR3 memory design. Also, the skew between data lanes and data strobes should be kept to a minimum and the eyes should be wide open. DDR3 is much easier to route, in fact, than DDR2 as leveling can be used to synchronize the delay of data lanes.

There are many other factors that can influence signal integrity, but basically the stackup planning and the PDN analysis, of a PCB, are the two main factors that control the stability of a design. Getting these two factors right, helps ensure the long term reliability and performance of any high-speed digital design.

 

We all know that simulation tools aren't cheap and then there is a learning curve associated with complex software not to mention that the Engineer needs to have years of experience analyzing high speed designs. By utilizing a PCB Board Level Simulation Service, you can be assured that your PCB will be reliable, manufactureable, conforms to specifications and passes the relevant compliancy tests saving you time, money and frustration for a fraction of the cost of board iterations and multiple compliancy testing. Plus, the simulation can be done before the design is finalized (before Gerber output or even earlier in the design process) to further reduce production time and costs.

Next month's column will continue to discuss signal integrity, in particular where most designers go wrong with signal integrity and how to avoid the common pit-falls.

**Points to Remember:**

- Crosstalk is the unintentional electromagnetic coupling between traces on a PCB. But crosstalk can also be induced in the return path–which often gets overlooked.
- Crosstalk can be coupled trace-to-trace, on the same layer, or can be broadside coupled by traces on adjacent layers. The coupling is three dimensional.
- The higher the aggressor voltage, the more crosstalk will be induced. It is therefore best to segregate groups of nets according to their signal amplitude.
- The easiest way to reduce crosstalk, from a nearby aggressor signal, is by increasing the spacing between the signals.
- Reducing the dielectric height, will also dramatically reduce crosstalk without impacting on real estate.
- Flight time delay and skew are key pillars in high speed PCB design signal integrity. One of the driving factors for flight time and skew performance is the placement of components.
- Flight time and skew—for an entire clock domain—are governed by the maximum placement, along with the routing rules that constrain the matching of the trace lengths.
- Given a length constraint, a designer can control signal integrity by controlling the PCB trace topology of the various parts of an interface. Included in this topology are any terminations.
- Stackup planning and the PDN analysis, of a PCB, are the two main factors that control the stability of a design.

**References:**

Beyond Design: Practical Signal Integrity – Barry Olney
Beyond Design: Pre-Layout Simulation – Barry Olney
Intro to Board-Level Simulation and the PCB Design Process – Barry Olney
Beyond Design: Impedance Matching: Terminations – Barry Olney
High-speed Signal Propagation – Howard Johnson
Electromagnetic Compatibility Engineering – Henry Ott
The ICD Stackup and PDN Planner is distributed globally by www.altium.com

**Bio:**

Barry Olney is Managing Director of In-Circuit Design Pty Ltd (ICD), Australia. The company developed the ICD Stackup Planner and ICD PDN Planner software, is a PCB Design Service Bureau and specializes in board level simulation.

 