# Beyond Design – Signal Integrity Part 1 of 3

by Barry Olney | In-Circuit Design Pty Ltd | Australia

As system performance increases, the PCB Designer's challenges become more complex. The impact of lower core voltages, high frequencies and faster edge rates has forced us into the high-speed digital domain. But in reality, these issues can be overcome by experience and good design techniques. If you don't currently have the experience – then listen-up. This three part series on signal integrity will cover the following topics:

1. How advanced IC fabrication techniques have created havoc with signal quality and radiated emissions.
2. The effects of crosstalk, timing and skew on signal integrity.
3. Where most designers go wrong with signal integrity and how to avoid the common pit-falls.

Technology is moving fast and much has changed over the past 25 years since I have been involved in high-speed multilayer PCB design. Particularly, advances in lithography enable IC manufacturers to ship smaller and smaller dies on chips. In 1987 we thought that 0.5 micron technology was the ultimate but today 22 nm technology is common.

Also, power consumption in FPGA's has become a primary factor for FPGA selection. Whether the concern is absolute power consumption, usable performance, battery life, thermal challenges, or reliability, power consumption is at the center of it all. In order to reduce power consumption, IC manufacturers have moved to lower core voltages and higher operating frequencies, which of course mean faster edge rates. However, faster edge rates mean reflections and signal quality problems. So even when the package has not changed and your clock speed has not changed, a problem may exist for legacy designs. The enhancements in driver edge rates have a significant impact on signal quality, timing, crosstalk, and EMC.

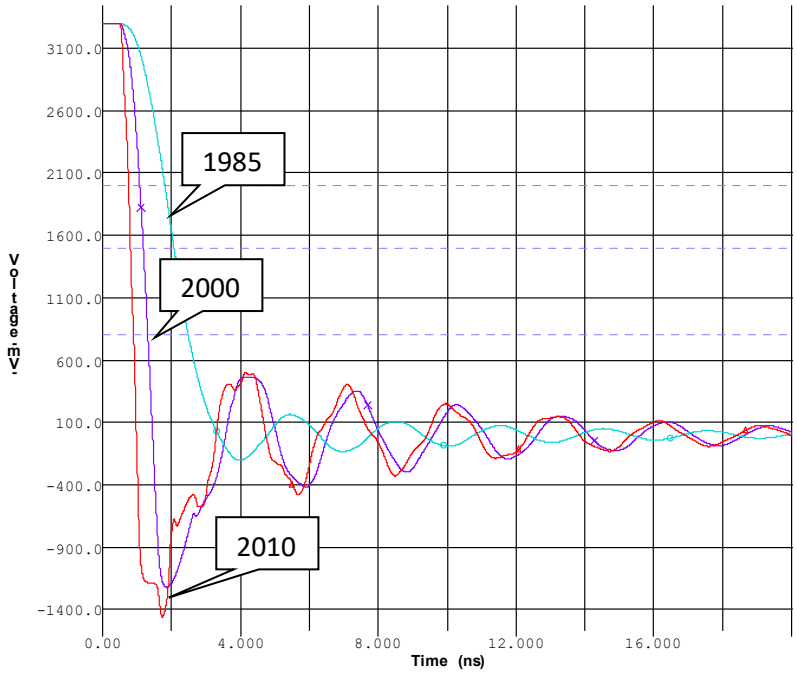


Figure 1 – Edge rate changes over the past 25 years

 

Figure 1. illustrates the change in edge rates over the years – from 10ns back in 1985 to less than 1ns in 2010. The faster edge rate for the same frequency and same length trace creates ringing in the un-terminated transmission line. This also has a direct impact on radiated emissions. Figure 2 shows the massive increase in emissions from the slowest to fastest rise time. When dealing with 1ns rise times, the emissions can easily exceed the FCC/CISPR Class B limits for an un-terminated transmission line.

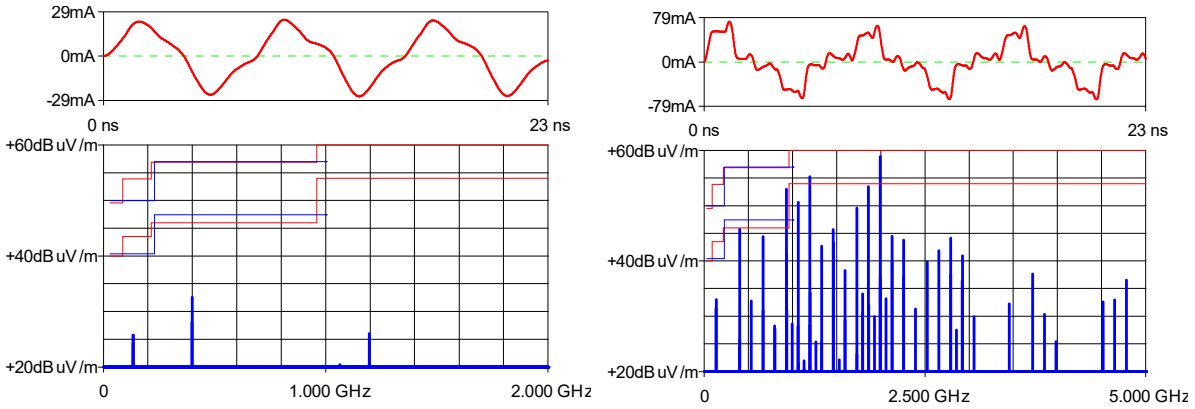


Figure 2 – Radiated emissions from the 10ns edge rate (left) and 1ns (right)

At high frequencies, traces on a PCB act as a mono-pole or loop antennas. Unfortunately, the high frequency components of the fundamental radiate more readily because their shorter wavelengths are comparable to trace lengths (particularly stubs), which act as antennas. Consequently, although the amplitude of the harmonic frequency components decrease as the frequency increase, the radiated frequency varies depending on the antennas/traces characteristics.

Computer based products tend to radiate on the odd harmonics. High emissions are generally detected at the 3$^{rd}$, 5$^{th}$ and sometimes the 7$^{th}$ harmonic of the fundamental clock frequency. If this also occurs where the AC impedance of the power distribution network is high, then the radiation is even higher. So at what speed should there be concern about wave propagation rather than just current in conductors?

**Rule of thumb:** Transmission line effects become an important design consideration when the trace length approaches 1/6 of the wave-length of the signal being transported. If the system clock frequency is 300 MHz, then the wavelength in FR4 is about 0.5m.

Impedance is the key factor that controls the stability of a design – it is the core issue of the signal integrity methodology. At low frequencies, a PCB trace is almost an ideal circuit with little resistance, and without capacitance or inductance. Current follows the path of least resistance. But at high frequencies, alternating current circuit characteristics dominate causing impedance, inductance and capacitance to become prevalent. Current then follows the path of least inductance. The impedance of an ideal lossless transmission line is related to the capacitance and inductance:

$$Zo = \sqrt{L/C}$$

But this is very simplistic and the impedance should be simulated by a field solver (as in Figure 3.) to obtain accurate values of impedance for each signal layer of the substrate. The impedance of the trace is extremely important, as any mismatch along the transmission path will result in a reduction in quality of the signal and possible radiation of noise. For perfect transfer of energy, the impedance at the source must equal the impedance at the load. However, this is not naturally the case and terminations are generally required at fast edge rates to limit ringing.

 

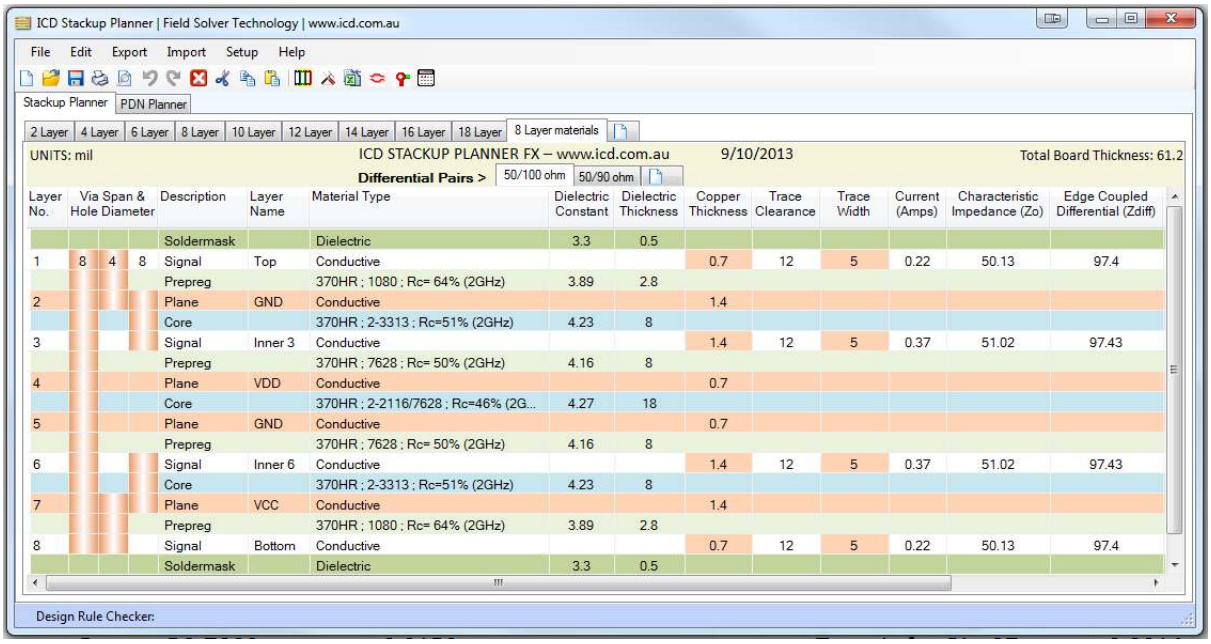


Figure 3 – Illustrates impedance simulated by a 2D BEM field solver in the ICD Stackup Planner

The configuration of the PCB Stackup depends on many factors. But whatever the requirements, one should ensure that the following rules are followed in order to avoid a possible debacle:

- All signal layers should be adjacent to and closely coupled to a uninterrupted reference plane, creating a clear return path and eliminating broadside crosstalk.
- There is good planar capacitance to reduce AC impedance at high frequencies.
- High speed signals should be routed between the planes to reduce radiation.
- The substrate should be symmetrical with an even number of layers. This prevents the PCB from warping during fabrication and reflow.
- The stackup should accommodate a number of different technologies.
- Cost (the most important design parameter) should also be addressed.

As signal rise times increase, consideration should be given to the propagation time and reflections of a routed trace. If the propagation time and reflection from source to load are longer than the edge transition time, an *electrically long trace* will exist. If the transmission line is short, reflections still occur but will be overwhelmed by the rising or falling edge and may not pose a problem. But even if the trace is short, termination may still be required if the load is capacitive or highly inductive to prevent ringing. Note that series terminators are the most effective for high-speed design.

For a driver signal with a 1ns rise time, since the speed of a signal in FR-4 is approximately 6in/ns (150mm/ns), then an un-terminated trace can only be 6 x 1/6 = 1.0 inches (25mm) before reflections occur and termination is required.

**Rule of Thumb:** All drivers, whose trace length (in inches) is equal to or greater than the rise time (in ns), must have provision for termination.

In order to terminate a transmission line, one first needs to know the impedance of the driver and the transmission line. So how do we find this information? First of all an accurate field solver, such as the ICD Stackup Planner is required to determine the impedance of the PCB traces. Then, the source impedance must be extracted from the IBIS model. Subtracting the source impedance from the trace

 

characteristic impedance gives the required series terminator value. Further details on how to find the source impedance in the IBIS model can be found in a previous column Beyond Design: Impedance Matching: Terminations.

Differential pairs are frequently used in high-speed design to provide noise immunity on serial interconnects. A differential pair is two complementary transmission lines that transfer equal and opposite signals down their length. These lengths should be kept equal and they should be coupled evenly along the signals length where possible. Symmetry is the key to successfully deploying differential signals in high-speed designs. Maintaining the equal and opposite amplitude and timing relationship is the principle concept.

Many people believe that since the two halves of the pair carry equal and opposite signals, that good ground connection is not required as the return current flows in the opposite signal. However, the return current actually flows in the reference plane below each trace. Figure 4, illustrates the return current of a microstrip pair flowing directly below each trace – just as is the case for a single ended transmission line. The only reason the pair of traces need to be coupled, is to reject common external noise.

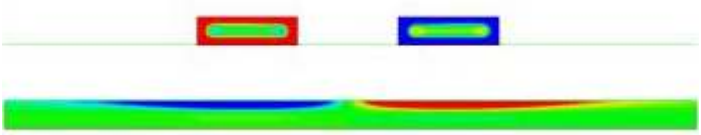

Figure 4 – Return current of a microstrip differential pair – courtesy Ansoft

If a differential pair can be routed closely coupled along the entire length, then consider using tight coupling. Otherwise, if the pair need to separate around an obstacle (a via for instance) then coupling the pair by twice the trace width is more effective. The reason being that a tightly coupled pair will increase impedance by 25% if separated while a more loosely couple pair will only vary by about 4% impedance. This provides more stable impedance along the trace length.

**The rule of thumb:** Gap = 2 x trace width.

Next month's column will continue to discuss signal integrity, in particular the effects of crosstalk, timing and skew on signal integrity so stay tuned….

**Points to Remember:**

- Advances in lithography enables IC manufacturers to ship smaller and smaller dies on chips.
- In order to reduce power consumption, IC manufacturers have moved to lower core voltages and higher operating frequencies which of course mean faster edge rates.
- Faster edge rates mean reflections and signal quality problems.
- The faster edge rate, for the same frequency and same length trace, creates ringing in the un-terminated transmission line. This also has a direct impact on radiated emissions.
- Transmission line effects become an important design consideration when the trace length approaches 1/6 of the wave-length of the signal being transported.
- Impedance is the key factor that controls the stability of a design – it is the core issue of the signal integrity methodology.
- Any mismatch in impedance along the transmission path, will result in a reduction in quality of the signal and possibly radiation of noise.
- Series terminations are generally required at fast edge rates to limit ringing.

 

- All drivers, whose trace length (in inches) is equal to or greater than the rise time (in ns), must have provision for termination.
- Differential pair return current actually flows in the reference plane below each trace not in the opposite signal.

**References:**

Beyond Design: Practical Signal Integrity – Barry Olney
Beyond Design: Pre-Layout Simulation – Barry Olney
Intro to Board-Level Simulation and the PCB Design Process – Barry Olney
Beyond Design: Impedance Matching: Terminations – Barry Olney
High-speed Signal Propagation – Howard Johnson
Electromagnetic Compatibility Engineering – Henry Ott
The ICD Stackup and PDN Planner is distributed globally by www.altium.com

**Bio -**

Barry Olney is Managing Director of In-Circuit Design Pty Ltd (ICD), Australia. The company developed the ICD Stackup Planner and ICD PDN Planner software, is a PCB Design Service Bureau and specializes in board level simulation.