

# High-Speed Serial Link PCB Design

## Beyond Design

by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

Serial communication has been used long before computers ever existed. The telegraph system using Morse code is one of the first digital modes of communication. All you need are two connections, which makes it simple and relatively robust. One wire is the signal and the other (dirty) ground. By interrupting the power with predefined patterns, information can be transferred over both short and long distances. The challenge is receiving the patterns correctly and quickly enough to be useful.

The simplest method of transferring data through the inputs or outputs (I/O) of ICs is to directly connect the data path from one IC to the next in parallel. But since most data consists

of more than one bit of information the parallel data path is multiple bits wide. This is fine for signal routing between ICs on a multilayer PCB over short distances. For instance, DDR memory devices take advantage of the fast data transfer rates of the parallel bus. However, it has two inherent problems for high-speed data transfer over long distances. The first problem is that one I/O pin is required for each data bit. The second involves meeting timing requirements. Due to these two issues, parallel data is typically transformed to a serial data stream using serializer/deserializer (SERDES) modules (Figure 1) for high-speed communication links.

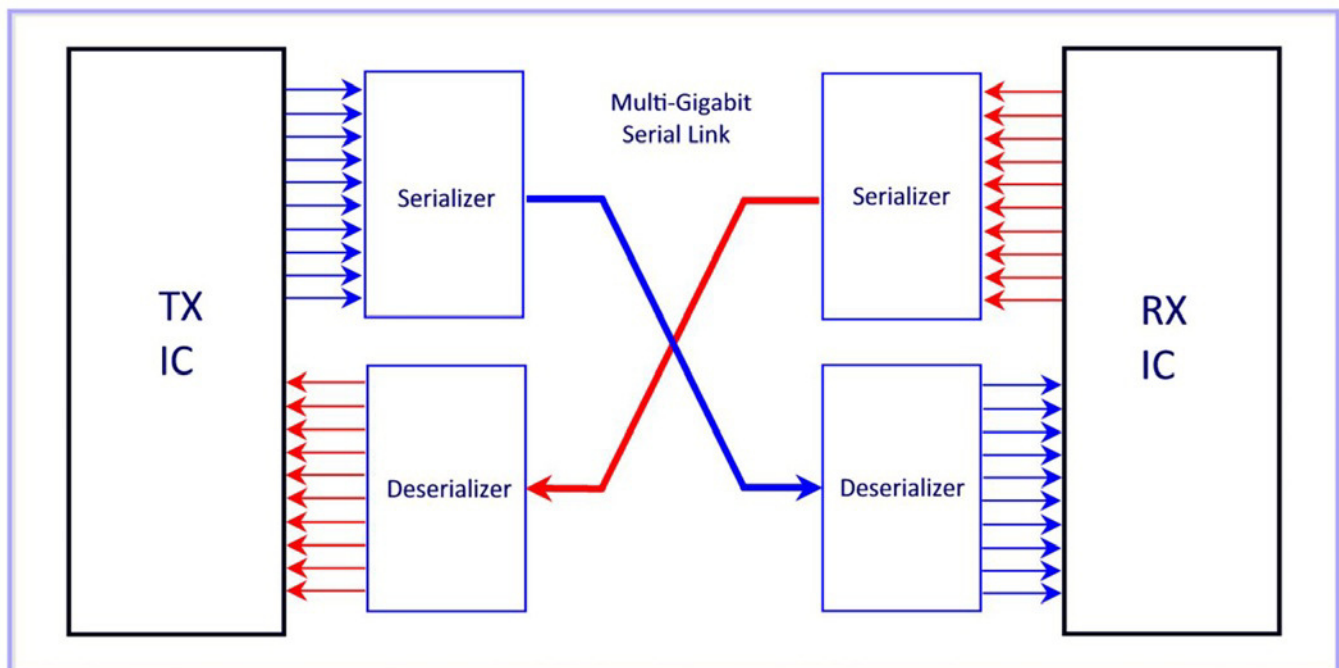


Figure 1: SERDES architecture.

Serial and parallel communications currently and historically co-exist and serve many requirements of intrasystem and intersystem data exchange. For instance, a parallel clock SERDES combo is normally used to serialize wide data-address-control parallel buses such as PCI. The choice of method is usually a tradeoff on factors such as speed, cost of materials, power consumption, and difficulty of physical implementation.

In principle, parallel communication is intrinsically faster than serial, because the speed of a parallel data link is equal to the number of symbols sent in parallel times the symbol rate of each individual path. Doubling the number of symbols sent at once doubles the data rate. For this reason, parallel communication is widely used in internal buses of integrated circuits and short distance IC-to-IC links. However, parallel communication is being replaced by serial communication in high-speed data links. These links include IC-to-IC communications on backplanes, computer networks, computer peripheral buses, long-haul communications, etc. The conventional reason to choose serial communications instead of parallel communications is cost.

High-speed SERDES devices are the dominant implementation of I/O interfaces at speeds of 2.5 Gbps and higher. Such devices are differentiated from a source-synchronous interface in that the receiver device contains a clock data recovery (CDR) circuit. This dynamically determines the optimal sampling point of the data signal based upon the transition edges of the signal. In other words, clock information is extracted directly from the data stream rather than relying on a separate clock. Also, signal integrity concerns frequently dictate that the data signal be equalized at the transmitter and/or receiver to counter the effects of the transmission channel and decode the signal properly.

Ten-bit transmission code was developed by IBM in the early 1980s. Called the 8b/10b code, the serializer maps each parallel data byte to a

10-bit code onto a serial pair. This code guarantees both multiple edge transitions every cycle as well as DC balance. It also provides a way to check for errors and send control information. Frequent edge transitions in the stream allow the receiver to synchronize the incoming data. DC balance facilitates driving AC-coupled loads, long cables, and optical modules. 8b/10b SERDES coding is well suited to serializing data such as cell or packet traffic across backplanes, cable, and fiber. Many standards such as ethernet, fiber channel, etc., use the popular 8b/10b coding at high data rates.

Implementing high-speed serial links can be challenging for the PCB designer. Any small discontinuity in the physical geometry along the transmission path can significantly degrade the signal. This degradation includes loss of amplitude, reduction of rise time, and increased jitter. As a result, one must be able to identify these discontinuities in the high-speed channel and mitigate their impact to improve the performance of the signal transmission.

A capacitor is typically placed in series with both differential signals to remove common mode voltage differences between ICs or different technologies. An “AC coupling capacitor” or “DC blocking capacitor” basically refers to the same thing. Any capacitor placed in series with the signal path tends to pass the high-frequency AC portions of the signal, while simultaneously blocking the low-frequency DC portions. These capacitors are essential to a variety of high-speed interfaces. And, as the next generation of designs target data rates of 56 Gbps and above, it becomes increasingly important to characterize channel transitions accurately to ensure a high confidence of success. As such, PCB designers need to take particular care routing serial interconnects.

It is always best to route critical signals on internal stripline layers. However, since the AC coupling capacitors are placed on the outer microstrip layer, routing on the outer layers becomes necessary to avoid discontinuities, layer transitions, and via stubs that create

reflections. The most important parameter of the AC coupling capacitor is its relative geometry with respect to the substrate. The capacitors are placed in series with high-speed traces and, as such, the capacitor body becomes a section of the transmission line.

There are two approaches to placement and routing of the AC coupling capacitors:

1. To eliminate the excess parasitic capacitance associated with surface mount lands, a portion of the reference plane that is directly beneath the component can be removed. This allows the signal that traverses through the capacitor to reference a lower plane (further away) and reduces the parasitic capacitance, thereby minimizing the impedance mismatch (Figure 2).

2. A more elegant alternative is to use a smaller capacitor such as a 01005. The explicit assumption (above) is that capacitor land width exceeds the trace width and hence represents a short section of transmission line that requires a cutout to maintain impedance. However, a 200  $\mu\text{m}$  trace can be used in conjunction with a 01005 package of 200  $\mu\text{m}$  land width to avoid the impedance mismatch altogether. In this case, the cutout is not required (Figure 3). Note that the required wider trace will reduce the impedance, so a thicker dielectric will be necessary to control impedance.

There are two compelling arguments for the placement of AC coupling capacitors. The first

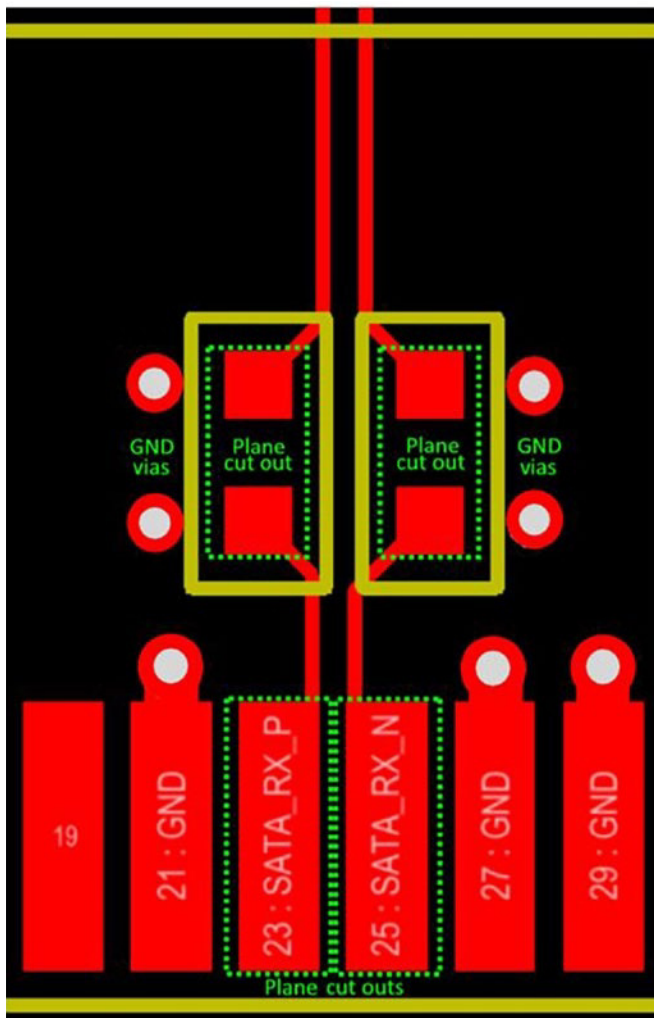


Figure 2: Plane cut-outs.

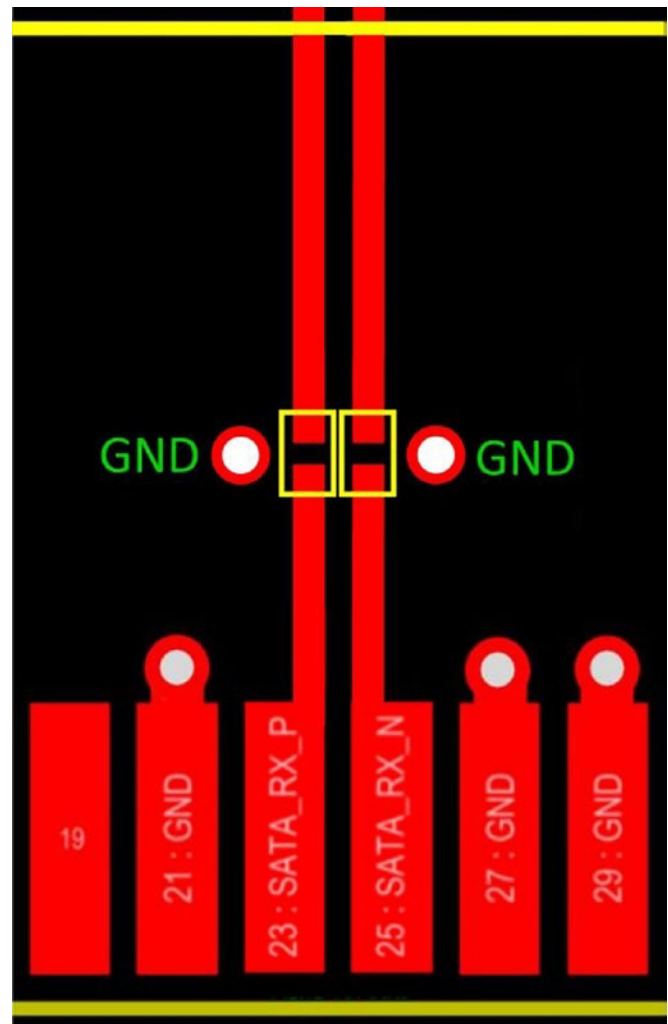


Figure 3: 200  $\mu\text{m}$  trace with 01005 capacitors.

argument is to put the AC coupling capacitor close to the receiver and you'll be good, since all of the reflections will be smaller due to transmission line attenuation. This represents a time domain view of the world. The second argument is that for most passive interconnects, S-parameters are reciprocal ( $S_{21} = S_{12}$ ). Under this pretense, for a particular topology, as long as the distance from the endpoints to the AC coupling capacitor is the same, it does not matter if you place the capacitor at the receiver or driver, because the results will be identical. This represents a frequency domain view of the world. However, in practice it's slightly arbitrary. Often it's defined by a standard and the capacitors are specified on one end or the other end or occasionally on both ends. For instance, PCIe (PCI Express) specifies the AC coupling caps on the TX side, as there are methods it uses for detecting if a downstream device is connected that depends on that particular AC coupling configuration.

The other issue with routing serial links, on outer microstrip layers, is the solder mask coating. Having solder mask on microstrip traces will make them more unpredictable since it's difficult to control the thickness of coating on the top of traces and in the valley between them. So, if the solder mask is removed around the traces, it can improve the channel performance. However, there are a few down sides to this:

1. Depending on the substrate used, you might also find that humidity can enter the substrate surrounding the traces and may impact the impedance (solder mask is a very good water seal, so you will usually not see this effect with covered traces).
2. Also, if you are using ENIG plating, be careful with how thick the gold and nickel layers are, since you might end up with narrowband resonance. At approximately 2.7 GHz, the resonant behavior of the nickel component in ENIG increases

insertion loss. This resonance is attributed to the ferromagnetic properties of the nickel layer. It is therefore wise to avoid using full body ENIG coating of microstrip traces at high frequencies. Consequently, solder mask over bare copper (SMOBC) processing should be considered for all high-speed designs. However, solder mask only impacts signal integrity above 12 Gbps.

Alternatively, to avoid the solder mask issue altogether, one could run differential serial links on the second layer of a dual build-up microstrip construction. This stabilizes the signal as it has a layer of prepreg over the traces. However, it will have impedance discontinuities due to the blind vias between layers 1 and 2 but this is practicable negligible.

When high-speed differential serial signals travel between boards, the destination location could have a different level on its ground. So, the transmitter and receiver could have different reference levels. A different ground level would cause the signal to appear to have a level shift that might make its level out of range for the receiver. AC coupling allows the receiver to change (bias) the signal reference levels to be compatible with the receiver's input levels. However, PCB designers must be able to identify any discontinuities in the high-speed channel and mitigate their impact to improve the performance of the signal transmission.

## Key Points

- The simplest method of transferring data through the I/O of ICs is to directly connect the data path from one IC to the next in parallel.
- DDR memory devices take advantage of the fast data transfer rates of the parallel bus.
- A parallel clock SERDES combo is normally used to serialize wide data-address-control parallel buses such as PCI.
- Parallel communication is intrinsically faster than serial.

- High-speed SERDES devices are the dominant implementation of I/O interfaces at speed of 2.5 Gbps.
- Implementing high-speed serial links can be challenging for the PCB designer. Any small discontinuity in the physical geometry, along the transmission path, can significantly degrade the signal.
- A capacitor is typically placed in series with both differential signals to remove common mode voltage differences between ICs or different technologies.
- Any capacitor placed in series with the signal path tends to pass the high-frequency AC portions of the signal, while simultaneously blocking the low-frequency DC portions.
- Routing serial links on the outer microstrip layers becomes necessary to avoid discontinuities, layer transitions, and via stubs that create reflections.
- The most elegant solution to AC coupling is to use a smaller capacitor such as a 01005. A 200  $\mu\text{m}$  trace can be used in conjunction with a 01005 package of 200  $\mu\text{m}$  land width, to avoid the impedance mismatch.
- The AC coupling capacitors should be placed close to the receiver unless defined by a standard whereby they are specified on one end or the other end, or occasionally on both ends.

- Solder mask on microstrip traces will make them more unpredictable since it's difficult to control the thickness of coating on the top of traces and in the valley between them.
- If you are using ENIG plating, be careful with how thick the gold and nickel layers are, since you might end up with narrowband resonance.
- Solder mask only impacts on signal integrity above 12 Gbps. **DESIGN007**

#### Resources

For more on this topic:

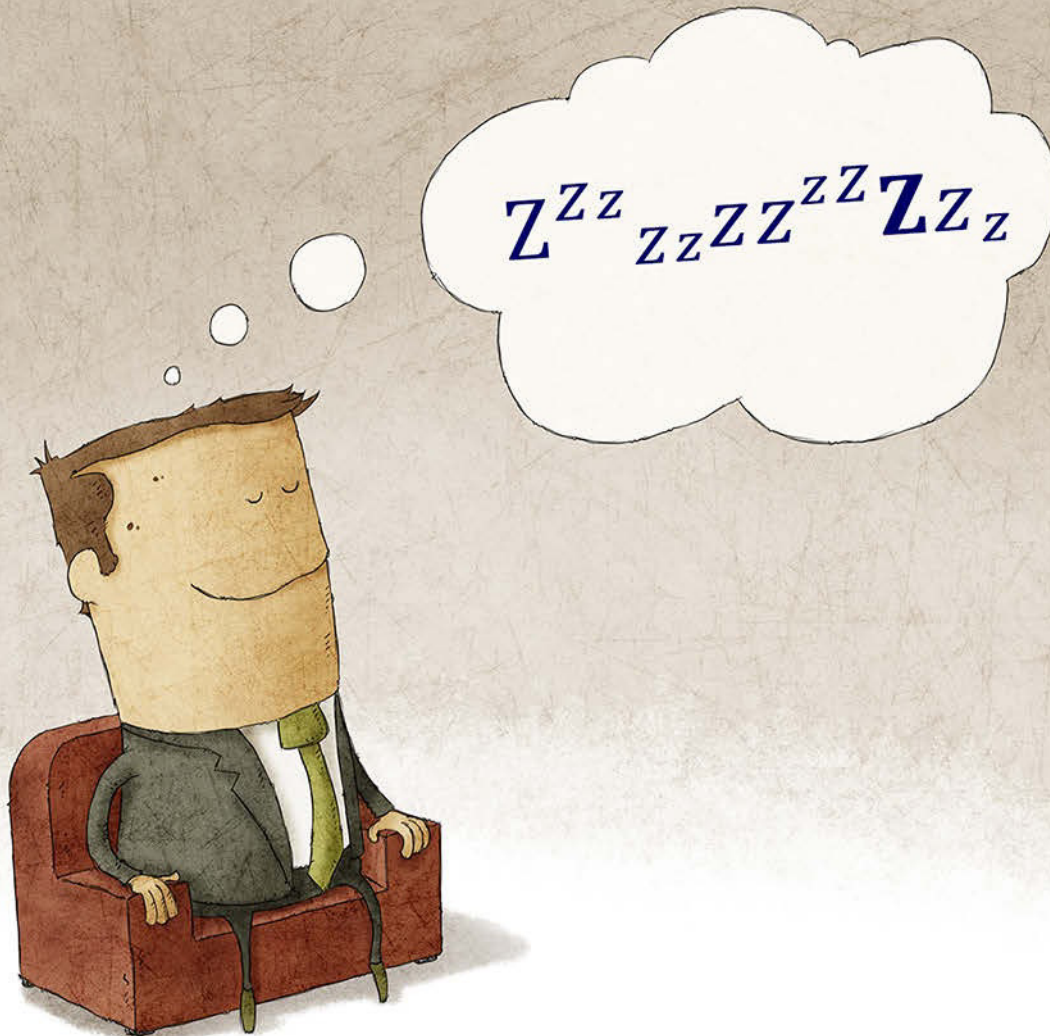
1. [Beyond Design: AC/DC is Not Just a Rock Band](#), by Barry Olney, Design007 Magazine, April 2018.
2. [Surface Finishes for High-Speed PCBs](#), by Barry Olney, The PCB Design Magazine, June 2014.
3. High speed serial link (SERDES), Introduction, Architectures and applications, by Abdallah Ashry, academia.edu.
4. Serializer and Deserializer (SerDes) for High-Speed Serial, by Dianyong Chen, et al.
5. High speed interconnect optimization, by Mallikarjun Vasa, et al.



**Barry Olney** is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded at [www.icd.com.au](http://www.icd.com.au). To read past columns or contact Olney, [click here](#).



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