Designing for the SAP Fabrication Process

Beyond Design

Feature Column by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

PCB designers are continually challenged with demands for reduced product size. However, form factor-driven design pressures have been relieved, in part, by the increased use of high-density interconnects (HDIs), which enable more functionality per unit area than conventional PCBs. Leveraging finer lines, thinner materials, and laser-drilled vias, HDIs have played a crucial role in device miniaturization. However, the traditional PCB subtractive etch processing becomes very difficult for feature sizes below 3-mil trace/space. This forces PCB designs to become more complex as electronics packages shrink—adding extra routing layers and microvia layers, and increasing the number of lamination cycles required, which impact yield, reliability, and thus cost.

As smartphone technology evolves to 5 Gbps, the PCB industry's approach to HDI manufacturing has also evolved. Vast multiple input/output antenna configurations and increasingly complex RF front-ends expand the RF content footprint. The higher bandwidth inherent to 5G requires much stricter impedance control. If not formed with extreme precision, the thinner traces of HDIs can introduce an increased risk of signal degradation. To fulfill these demands, the amount of available space for HDI PCBs, within 5G smartphones, needs to be significantly reduced.

The semi-additive process (SAP) is a production-proven method used on low dissipation loss (Df) build-up materials that enable the manufacture of ultra-fine-line circuitry. This technique utilizes additive process steps, adding copper to the base dielectric, rather than subtractive processes to create the circuit pattern. Fabricators previously only able to offer 3-mil trace/space can now reliably produce 1-mil trace/space and below. Further reductions required the adoption of various SAP manufacturing processes commonly used in the IC substrate industry, including laser direct imaging (LDI), improved laser drilling, extremely thin copper foils, via fill pattern plating, and flash etching, into a process called modified SAP (mSAP).

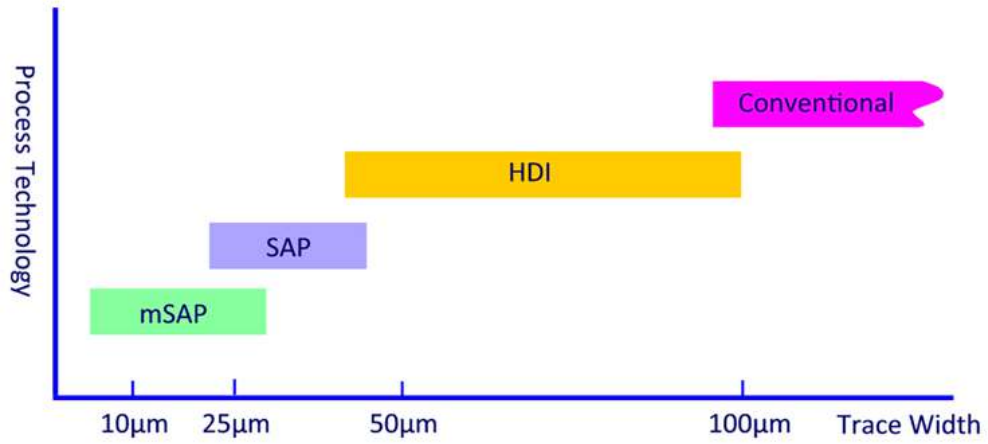

Figure 1: Trace width vs. process technology.

SAP enables the printed circuit board fabricator to employ an additive screen process instead of an edge-removal, etched process—the end result is a PCB design that can dramatically reduce area, layer

count, and weight of electronics products, as well as provide significant RF benefits. Figure 1 shows the trace width for the available technology processes.

The smartphone, tablet, and wearables markets have advanced the mSAP processes to be compatible with high volume PCB fabrication. Current designs merge both subtractive-etch processing and mSAP processing. This combination is crucial to the thinner, smaller motherboard design which frees up space for a more robust battery. A technology teardown of the Gen 11 iPhone X shows trace/space designed at 1.2 mils (30 µm) and more advanced designs have 0.4 mils (10 µm) features. That is a complete game-changer for PCB design.

SAP provides tighter line width control and straight conductor sidewalls, greatly improving impedance control. In a subtractive process, fine lines are formed by coating the copper layer with an etch resist where the copper should be retained and etching away the remaining copper. The main drawback of this approach is that the chemical etchant used to vertically etch the lines will also dissolve the copper in the trace walls. In a cross-section view, the resulting traces will appear trapezoidal (Figure 2).

With SAP, a much thinner copper layer is coated onto the laminate and plated in the areas where the resist is not applied. The thin copper remaining in the spaces between conductors is then etched away. The traces are formed with much greater precision, in straight vertical lines, yielding an almost rectangular-shaped cross-section that maximizes circuit density and enables accurate impedance control with lower signal loss. With traditional subtractive etch processes, controlled impedance is typically specified with a ±10% tolerance due to variation in the material and the process. With SAP, the line width tolerances are much more tightly controlled and controlled impedance can be held to a stricter tolerance.

The standard SAP process utilizes some roughening or texturing of the dielectric substrate to achieve sufficient adhesion; however, the rough surface at the plating/resin interface potentially increases transmission loss at high signal speeds. To promote the signal integrity of high-frequency signal transmission, the SAP process should provide high plating-to-resin adhesion as well as a very smooth interface in between. Consequently, the copper roughness should be kept under 1 µm.

Routing channels between BGA ball contact lands is progressively restricted as the contact pitch is reduced. Some suppliers of FPGAs understand the challenges facing the PCB designer in signal routing and have maintained a constant 0.30 mm contact diameter to maximize conductor routing channels on the outer surface of the circuit board. Even though smartphones and tablets may have stabilized in size and the trend is more toward system-in-chip than it is toward further shrinking, we definitely will be seeing more chips with pitches of 0.30 mm and less.

Generally, PCB designers can only route to the outer two rows of lands on the perimeter of a BGA using HDI technology. Squeezing one signal trace between BGA lands or break-

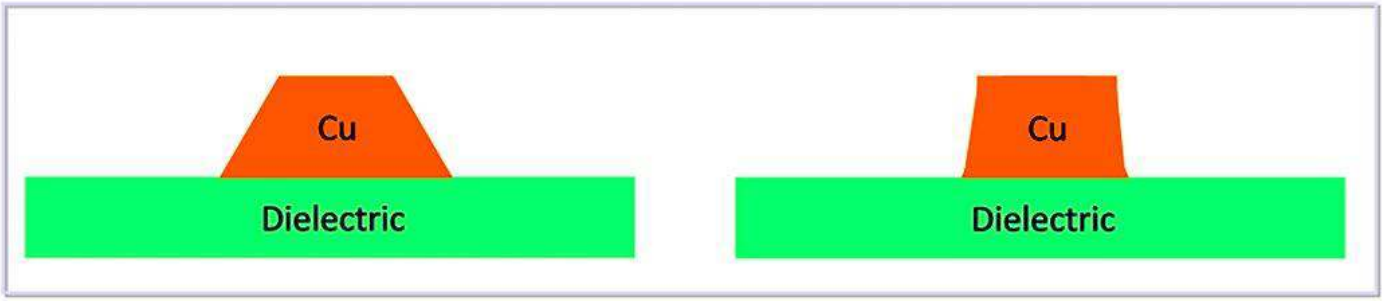

Figure 2: Trace geometry for the subtractive (left) and additive processes (right).

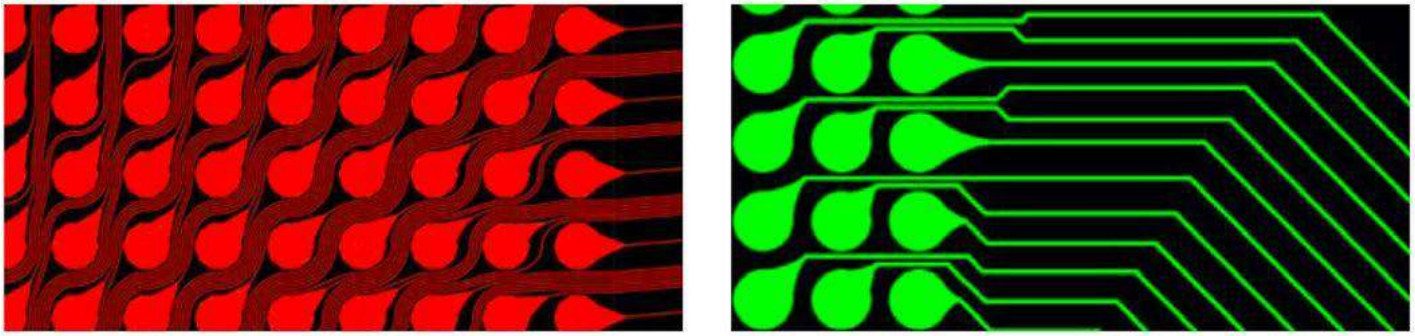

Figure 3: SAP (left) vs. HDI routing (right). (Source: Averatek)

out vias has been the unofficial limit for typical low-cost multilayer boards for many years. Although, if you choose to pay a premium, then the limits can always be stretched as in Figure 3 (right). However, the SAP process promises greater freedom with six 1/1 mil trace/space between lands. Figure 3 (left) is a drawing of multiple traces routed between 0.3 mm pitch lands. However, this may be pushing the limit, not because of physical size, but rather because of signal integrity requirements for impedance and coupling. There are a few issues with tightly routed signal traces:

1. Unintentional coupling of parallel segments is extremely strong between 1-mil spaced traces. This might be fine for grouped synchronous buses and data lanes but horrendous for unrelated signals. Figure 4 illustrates the exponential increase in crosstalk with tight coupling, particularly on outer microstrip layers.
2. The impedance of the trace must be maintained at 40–50 ohms and this is not possible with the standard dielectric thickness of HDI stackups. An extremely thin dielectric of 1 mil or less is required to maintain 50 ohms impedance with a 1-mil trace; this technology may not be suitable for standard HDI rigid boards. However, flexible circuits are ideal with Apexyl LPEN/LPET, Dupont Pyralux Flex, ThinFlex A/H, Ultrflex GTS 7800, and Rogers

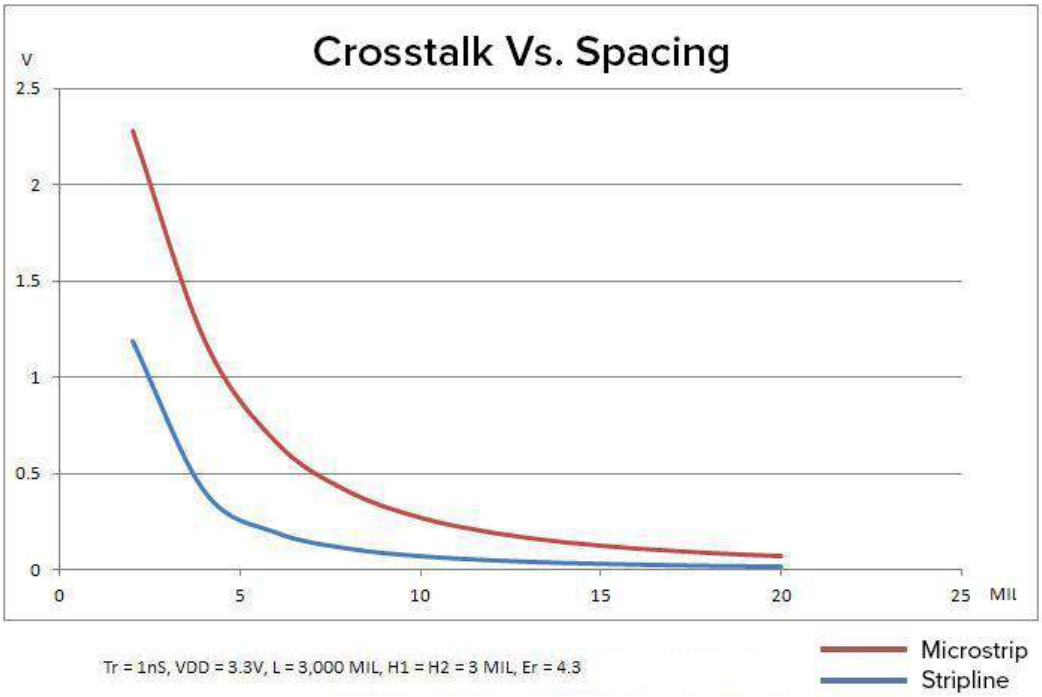

Figure 4: Crosstalk vs. spacing for microstrip and stripline layers.

R/Flex Crystal and Jade materials all providing low loss flexible materials of 1 mil thickness.

3. Unless all the routing is completed on the top (component) layer, breakout vias are still required—although the use of via-in-pad and blind vias dramatically reduce the real estate required.

There are also substantial signal integrity benefits from semi-additive processing. Tighter line width control and straight conductor sidewalls greatly improve impedance control. Also, the technology helps reduce parasitic inductance by reducing loop area, as well as increasing density. Fine-line precision RF features can also be realized with SAP technology.

3D printing of multilayer PCBs is also an additive process. With its game-changing technology, 3D printing allows free-form shapes, enabling you to find novel solutions to development challenges, thus enabling new devices and designs. It allows a seamless, one-step manufacturing process from digital design to functional devices. Plus, it enables printed 3D antennas/coils and eliminates loss-generators. Although 3D printing is currently limited to 3/4 mil trace/space construction, it has a huge advantage for prototype construction, of multilayer boards in-house, within a matter of hours.

Key Points:

- Form factor-driven design pressures have been relieved, in part, by the increased use of high-density interconnects.
- The traditional PCB subtractive etch processing becomes very difficult for feature sizes below 3 mil trace/space.
- The thinner traces of HDIs can introduce an increased risk of signal degradation.
- The SAP process is a production-proven method used on build-up materials that enable the manufacture of ultra-fine-line circuitry.
- Fabricators previously only able to offer 3 mil trace/space, can now reliably produce 1 mil trace/space and below.
- Further reductions required the adoption of various mSAP manufacturing processes.
- SAP enables the printed circuit board fabricator to employ an additive screen process instead of an edge-removal, etched process.
- SAP provides tighter line width control and straight conductor sidewalls greatly improving impedance control.
- SAP provides tighter impedance tolerance than the traditional subtractive etch processes.
- The SAP process promises greater routing density with six 1/1 mil trace/space between lands.
- Unintentional coupling of parallel segments is extremely strong between 1 mil spaced traces.
- An extremely thin dielectric of 1 mil or less is required to maintain 50 ohms impedance with a 1 mil trace.
- Breakout vias are still required with SAP–although via-in-pad dramatically reduces the real estate required. **DESIGN007**

Resources

1. Beyond Design: "Controlling the Beast" by Barry Olney
2. "SAP and mSAP in Flexible Circuit Fabrication" by Tara Dunn
3. "Achieving Fine Lines and Spaces Using mSAP" by Rich Bellemare and Jordan Kologe
4. "mSAP: The New PCB Manufacturing Imperative for 5G Smartphones" by Many Gantz
5. Nano Dimension, Dragonfly product datasheet

Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded at www.icd.com.au. To read past columns or contact Olney, click here.

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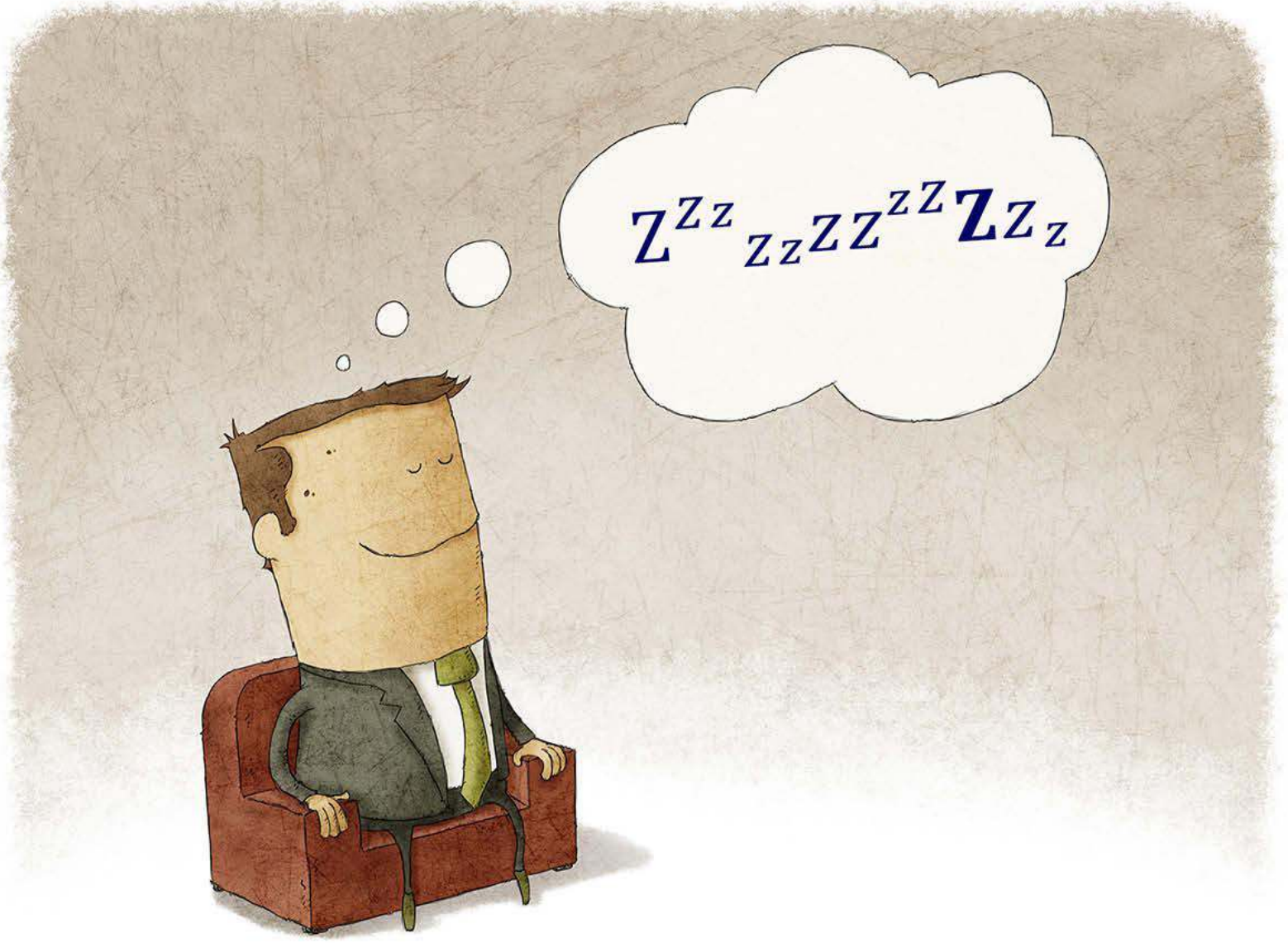

Did you know that two seemingly unrelated concepts are the foundation of a product's performance and reliability?

- Transmission line impedance and
- Power Distribution Network impedance

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