High-speed Rules of Thumb

Beyond Design

Feature Column by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

The idiom "rule of thumb" is often used in electronics design and has its origins in the practice of measuring roughly with one's thumb. Rules of thumb are easy-to-remember, broadly accurate guides or principles based on practice rather than theory. They are used to help feed our intuition to find a quick solution based on experience. We are often forced to use rules of thumb in PCB design in the absence of expensive analysis tools. We also use them to get quick ballpark figures initially and then fine-tune the numbers with further analysis. We can use rules of thumb as a sanity check to assess whether we are using our tools ent some commonly used and helpful rules for high-speed PCB design.

The most popular rule of thumb is probably that "Rules are meant to be broken." This implies that there are times when we should think for ourselves and not obey every rule presented to us blindly. I find that with every PCB design I complete, there is at least one rule that needs to be broken to accommodate a certain situation. All board designs are different.

The following is a list of rules of thumb extracted from the various columns and seminars I have written over the years. If you require clarification on any rule, please read

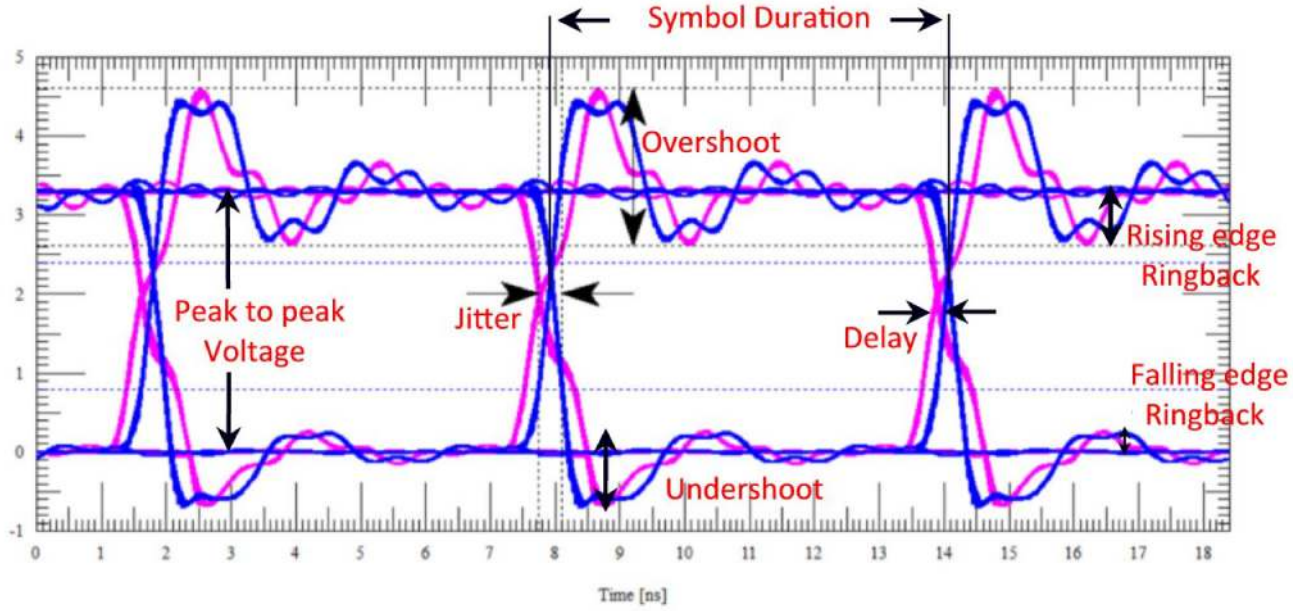

Figure 1: Eye diagram is used to evaluate the transmission line.

end of each column, you can find the "points to remember." I have grouped these into categories for easy reference.

Transmission Lines

1. Always use controlled impedance transmission lines for digital circuits.
2. For a perfect transfer of energy, the trace impedance must equal the source.
3. Series termination is used to match the source to the trace.
4. Place the series terminator close to the source (< 200 mil).
5. Terminate both ends of a trace in a multidrop (daisy chain) bus.
6. All drivers where length (in inches) is equal to or greater than the rise and fall time (in ns) must have provision for termination.
7. Mismatched impedance causes signals to reflect back and forth along the lines, which causes ringing.
8. The propagation speed of a signal is $c/\sqrt{\mathrm{Dk}}$ (~6 in/ns in FR-4).
9. Signal bandwidth is about five times the fundamental frequency (5th harmonic).
10. The skin depth of copper is 2 µm at 1 GHz. This increases with the square root of frequency.
11. Keep the mark-to-space ratio of the waveform equal as this eliminates all the even harmonics.
12. Flight times of the critical signals should be within specification. This may differ from matched lengths. Check data to strobes and address/command signals to clocks.
13. A transmission line looks very similar to a low-pass filter, which attenuates high frequencies.
14. A square wave is made up of several sinusoid waveforms of different frequencies. However, only the lower frequency components can transverse the transmission line.
15. FR-4 has a negligible loss at frequencies below 1 GHz, but since the dielectric loss is frequency dependent, at higher frequencies, the dielectric loss of FR-4 increases.
16. The maximum bandwidth of a signal is not determined by the fundamental frequency but by the rise time of the signal—5th harmonic.
17. At high frequencies (> 10 GHz), a non-uniform dielectric in the substrate can cause skew in differential signals.
18. The three common transmission line structures of a multilayer PCB are embed-

ded microstrip, symmetric, and dual asymmetric stripline configurations.

19. A transmission line is a series of conductors that guide electromagnetic energy from one point to another. It is the movement of an electromagnetic field or energy—not voltage or current.
20. It is the electromagnetic energy that propagates down the transmission line—not electron flow.
21. As the electromagnetic energy propagates along a transmission line, current is induced into the conductors. This current flows along the conductors, charging the first section's parasitic capacitance, and then flows back on the return conductor (reference plane) to the source.
22. Current always flows in a loop, but it does not flow along the transmission line to the load and then return to the source. The propagating signal charges up each section as the rising edge propagates along the transmission line.
23. A distributed system disperses elements through the substrate along the entire length of the transmission line and is characterized by delay and scattered reflections.

Stackup

1. The dielectric constant of FR-4 is ~4.0. This decreases as frequency increases.
2. The dielectric loss (dissipation factor) of FR-4 is ~0.02. This generally increases with frequency.
3. A 50-ohm microstrip will have a dielectric thickness of approximately half the trace width.
4. Solder mask covering a microstrip will decrease the impedance by 1–2 ohms.
5. Choosing the same dielectric materials as the Fab shop stocks will increase accuracy by ~5%.
6. A signal travels 13–17% faster in microstrip compared to stripline configurations.
7. All signal layers should be adjacent to a reference plane, creating a clear return path and eliminating broadside crosstalk.
8. The signal end and differential impedance for several different technologies that must share the sample layers should be determined.
9. Microstrip layers should be closely coupled to the planes, reducing crosstalk.
10. Avoid broadside coupling by separating the internal signal layers with bulk core material.

Figure 2: Six-layer stackup. (Source: iCD Stackup Planner)

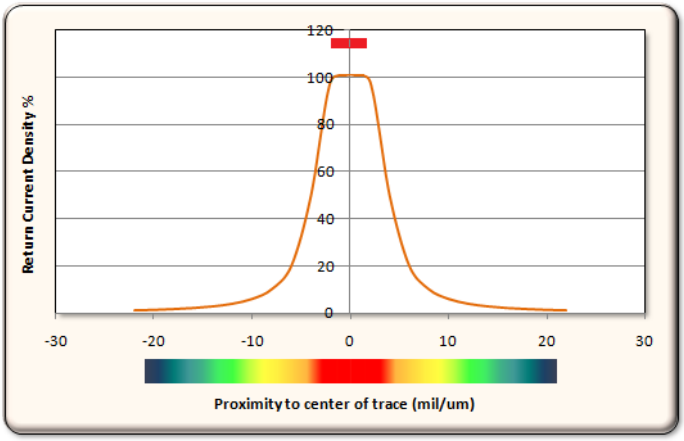

Figure 3: Proximity of return current to signal trace.

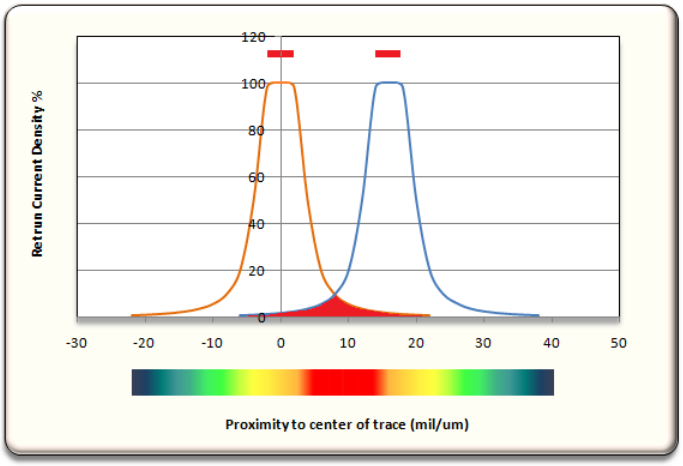

Figure 4: Differential signal return current.

Return Current Paths

1. Return current paths follow the path of least inductance rather than coupling to a plane further away.
2. For offset striplines, whichever plane is closest to the trace has the most influence on impedance. It's advisable to have a deliberate offset to eliminate this possibility and to be certain which plane will be used for the return path.
3. The impedance of broadside coupled traces is affected by the mechanical registration of layers of the substrate during the fabrication process and should be avoided.
4. Current always flows in a loop. The outbound pulse charges the local parasitic capacitance as it propagates down the transmission line and returns to the driver.
5. The ground plane is not a dumping ground for unwanted signals.
6. In a DC circuit, the return current takes the path of least resistance.
7. At high speed, the return current takes the path of least inductance, which just happens to be the reference plane (either ground or power) directly above or below the trace.
8. Return current tends to couple to the signal conductor, falling off in intensity with the square of increased distance.
9. Because of skin effect, the high-frequency fields cannot penetrate the plane.
10. The current density will be the same regardless of the frequency.
11. Placing the trace closer to the reference plane will reduce crosstalk even if the trace spacing remains the same.
12. It is important to consider how the return current propagates in the planes. When you plan your stackup, be aware of which plane(s)—either power or ground—will be the return path for your critical signals, and make sure there is an unobstructed return path.
13. Stitching vias should be used to connect ground planes or decaps between power and ground planes to provide return current paths.
14. If there are multiple ground planes, then place a stitching via as close as possible to each layer transition (signal via).
15. If power planes are also used as the reference plane, then place decoupling capacitors as close as possible to each layer transition.

Crosstalk

1. Crosstalk is the unintentional electromagnetic coupling between traces on a PCB. But crosstalk can also be induced in the return path, which often gets overlooked.
2. Tightly couple traces to reference planes to reduce crosstalk.
3. In the multilayer digital environment,

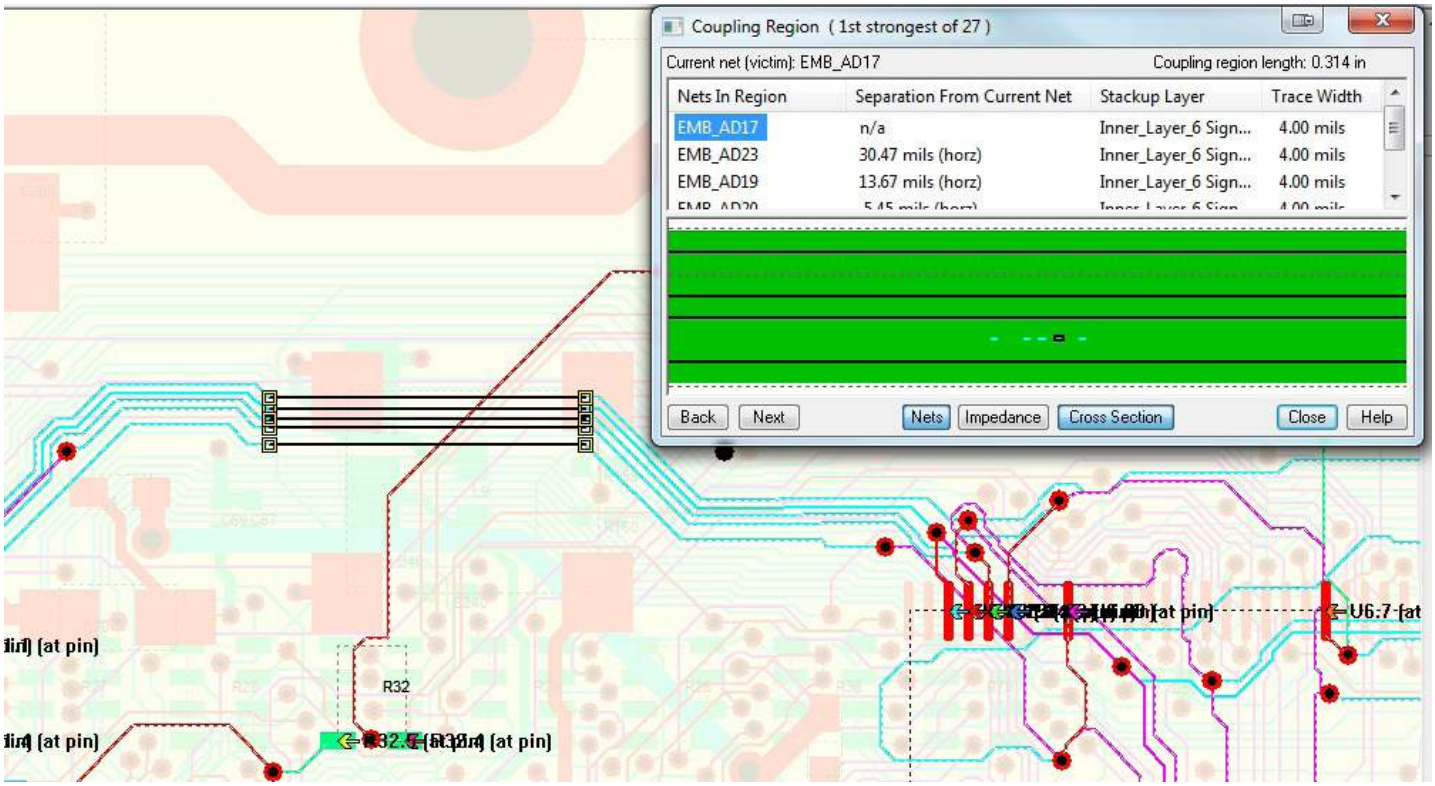

Figure 5: Parallel segment crosstalk.

ground pours do not significantly reduce crosstalk.

4. Ground pours have the disadvantage of altering the impedance of traces that run adjacent to a pour area, causing reflections.
5. If you must use copper pours to balance etching, use a 20-mil clearance from the pour to any signal trace to avoid crosstalk.
6. Crosstalk is typically picked up on long parallel trace segments. Traces should be spaced by three times the trace thickness where possible.
7. Avoid long parallel segments > 500 mils.
8. Avoid inadvertent broadside coupling on adjacent dual stripline layers.
9. Route adjacent dual striplines orthogonally to minimize coupled regions.
10. The lowest crosstalk is obtained using the narrowest traces with the highest impedance.
11. Use slow rise time signals or use a series terminator to slow the rise time.
12. Reduce the driver fanout/number of loads.
13. Reduce the driver strength. Mid-range is generally fine but should be checked by simulation.
14. Route on stripline (inner layers) rather than microstrip (outer layers). This also reduces EMI.
15. Ensure that you don't exceed the maximum crosstalk of 150 mV.
16. The propagation delay of a serpentine trace is less than the delay through an equivalent-length straight trace because of forward crosstalk.
17. Forward crosstalk or far-end crosstalk does not exist in the stripline configuration.
18. Crosstalk can be coupled trace-to-trace on the same layer or can be broadside coupled by traces on adjacent layers. The coupling is three-dimensional.
19. The higher the aggressor voltage, the more crosstalk will be induced. It is therefore best to segregate groups of nets according to their signal amplitude.
20. The easiest way to reduce crosstalk from

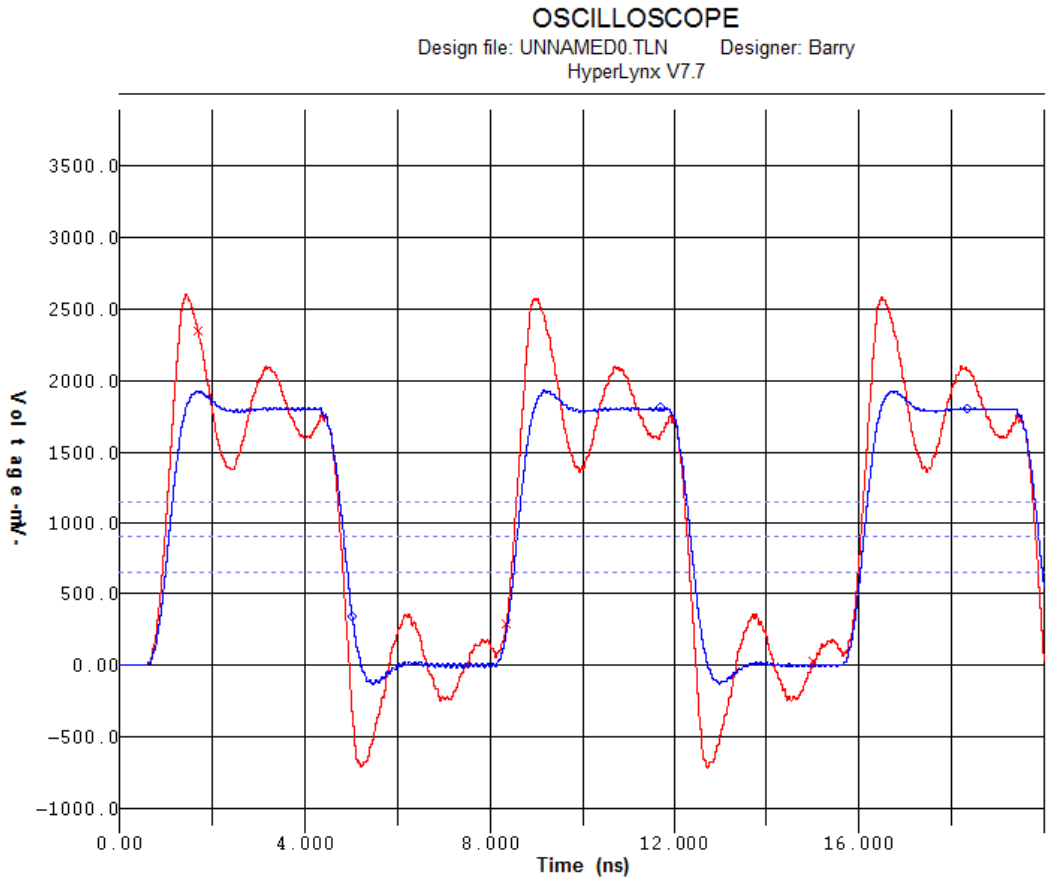

Figure 6: Ringing signal (red) and matched signal (blue).

a nearby aggressor signal is by increasing the spacing between the signals.

21. Reducing the dielectric height will also dramatically reduce crosstalk without impacting real estate.

Signal Integrity

1. Impedance is the key factor that controls the stability of a design. It is the core issue of the signal integrity methodology.
2. To reduce power consumption, IC manufacturers have moved to lower core voltages and higher operating frequencies, which of course mean high current requirements and faster edge rates. Faster edge rates mean reflections and signal quality problems.
3. The impedance of the trace is extremely important, as any mismatch along the transmission path will result in a reduction in the quality of the signal and possibly radiation of noise.
4. All drivers whose trace length (in inches) is equal to or greater than the rise time (in ns) must have provision for termination. It is the rise time rather than the frequency that is of concern.
5. Couple the signal traces closely to the plane. A 3-mil thickness dielectric material reduces the crosstalk by approximately a quarter compared to the 6-mil given the same trace spacing.
6. The goal of PDN analysis is to maintain low AC impedance on the supply voltage planes—from DC to the maximum required frequency—including harmonics.
7. Clock signals should always have the longest delay of the group as the data, address, control, and command signals need to settle down before the clock arrives at the chip sampling the bus.
8. Faster edge rates mean reflections and signal quality problems.

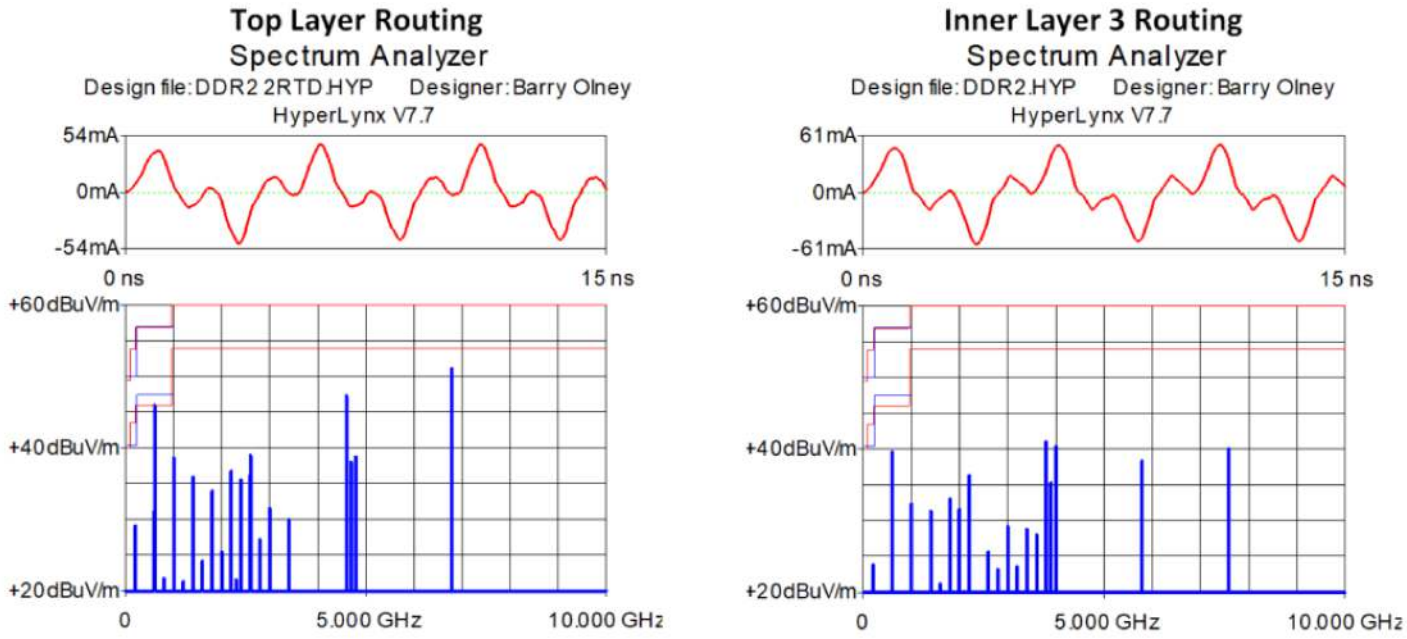

Figure 7: Microstrip vs. stripline radiation.

9. The faster edge rate for the same frequency and same length trace creates ringing in the unterminated transmission line. This also has a direct impact on radiated emissions.
10. Transmission line effects become an important design consideration when the trace length approaches 1/6 of the wavelength of the signal being transported.
11. Any mismatch in impedance along the transmission path will result in a reduction in the quality of the signal and possibly radiation of noise.
12. Series terminations are generally required at fast edge rates to limit ringing.
13. Differential pair return current flows in the reference plane below each trace, not in the opposite signal.
14. An EM carrier wave can transport information, or it can supply energy to power an IC.
15. If the trace is too narrow, then the contained energy will dissipate as heat.

EMC

1. Electromagnetic fields are produced when a logic driver delivers a high-speed, fast-rise time pulse into a trace. The electromagnetic wave propagates down the length of the trace radiating into the surrounding dielectric material and coupling energy to nearby trace segments.
2. In a multilayer board, each microstrip and each stripline configuration is isolated from the layers above or below.
3. Electric fields, which capacitively couple current into a nearby trace, are somewhat absorbed by the plane but still tend to radiate noise outward.
4. Magnetic fields refract at dissimilar dielectric boundaries and couple voltage inductively into a nearby trace.
5. A traveling, varying magnetic field is associated with a periodically changing electric field that may be conceived in terms of a displacement current.
6. EM fields do not merge but add vectorially, thereby distorting the signal. **DESIGN007**

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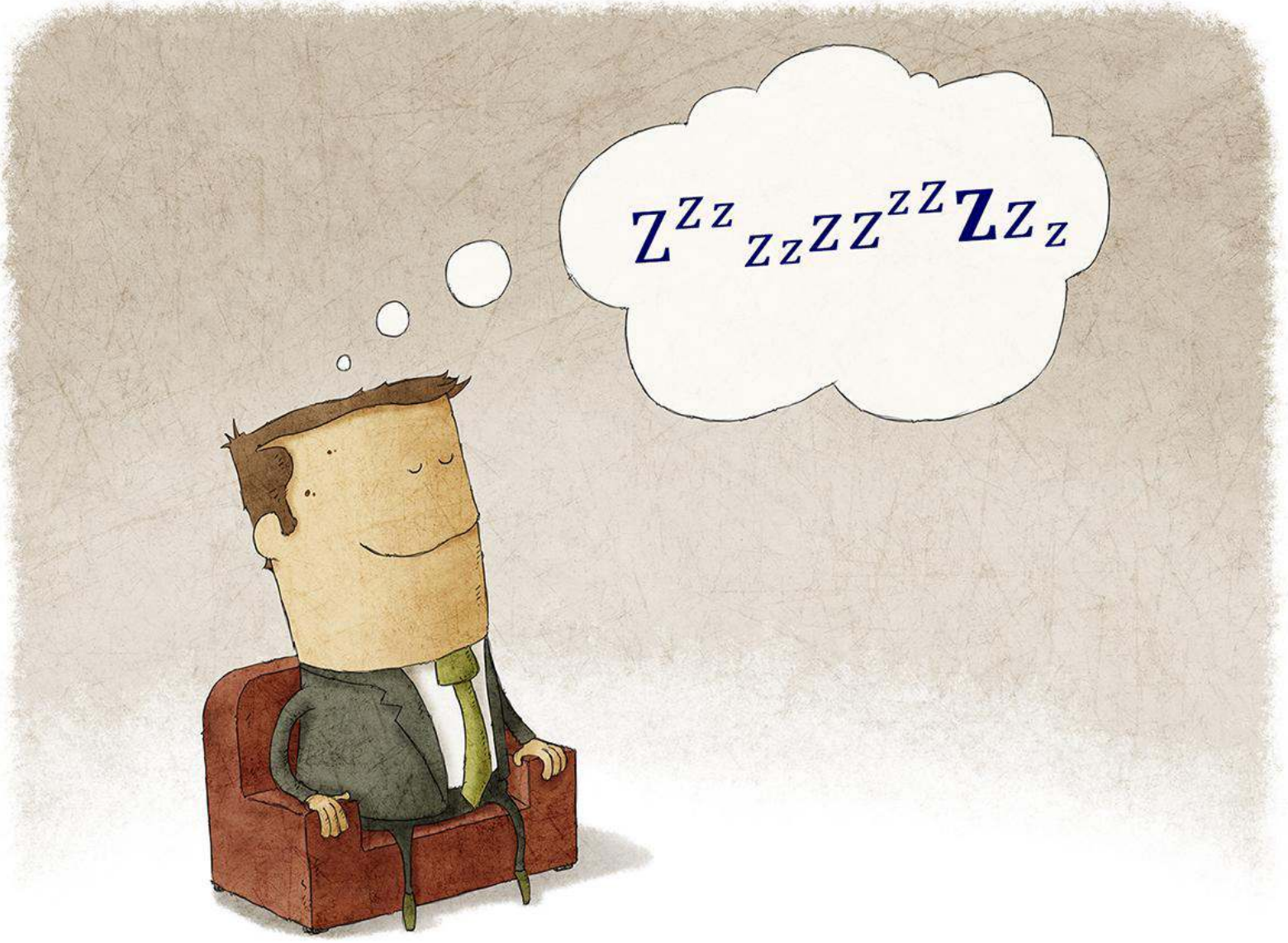

Did you know that two seemingly unrelated concepts are the foundation of a product's performance and reliability?

- Transmission line impedance and
- Power Distribution Network impedance

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