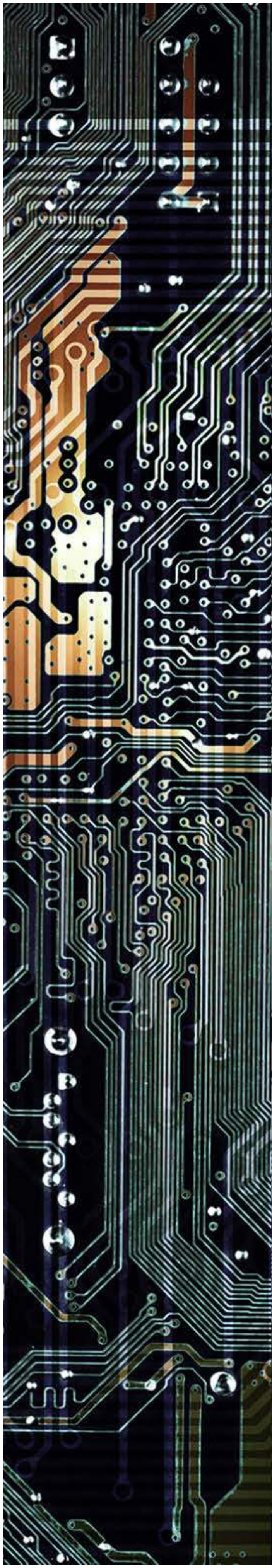

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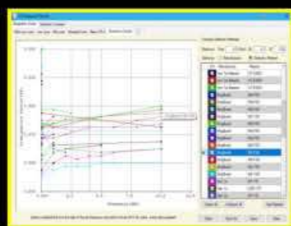

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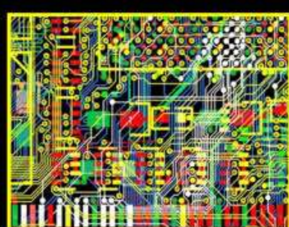

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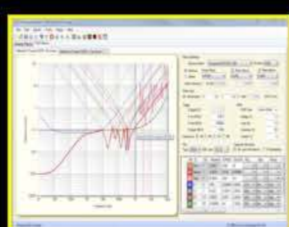

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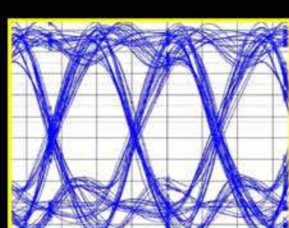

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Routing Strategies to Minimize Radiation

Beyond Design

by **Barry Olney,** IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

Electromagnetic (EM) energy propagates through the dielectric materials of a multilayer PCB guided by the signal traces between the planes, for inner stripline layers (Figure 1), but it acts slightly differently on the outer microstrip layers. Microstrip layers generally have a solid ground reference plane on one side but allow radiation from the boundless surface into the air. A well-thought-out routing strategy can avoid up to 10 dB of radiation from the substrate. Embedding signals between the planes reduces these emissions, and susceptibility to radiation, as well as providing electrostatic discharge protection. So, not only can one prevent noise from being radiated but also reduce the possibility of being affected by an external source.

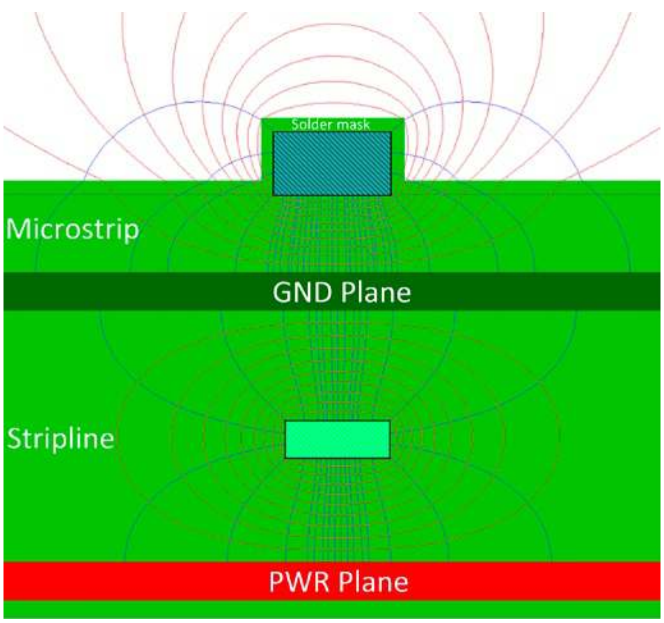

Figure 1: Microstrip EM fields (top) and stripline EM fields (bottom).

Studies conducted by Hewlett-Packard have found that there are up to 20 dB greater emissions from edge-located traces compared to traces located in the centre of the board on outer layers. Yet the same test performed on buried traces indicated no change as the traces were placed nearer the PCB edges. This implies that it is best to keep well away from the edge of the board when routing on the outer microstrip layers. The impedance changes as the reference plane decreases in the area beneath the trace.

On a multilayer PCB, critical signals should be routed on a stripline layer adjacent to a solid reference plane to reduce radiation. The spacing between the signal trace and the return plane should be as small as possible to increase coupling and reduce the loop area.

The three constraints to keep in mind:

- Keep the mark-to-space ratio of the waveform equal as this eliminates all the even harmonics.
- Route high-speed signals between the planes, fanout out close to the driver (200 mils) dropping to an inner layer, and route back up to the load again with a short fanout.
- Use the same reference plane (GND if possible) for the return signal, as this reduces the loop area and hence radiation.

Signal Flight Time

Signal Layer Number	Layer Inductance (nH/m)	Layer Capacitance (pF/m)	Layer Propagation Velocity (m/s)	Trace Length (inches)	Trace Inductance (nH)	Trace Capacitance (pF)	Flight Time (ps)
1	311	110	1.71e+8	2.0000	15.80	5.59	297.08
4	354	112	1.59e+8	2.0000	17.98	5.69	319.50
6	356	148	1.45e+8	2.0000	18.08	7.52	350.34
7	356	148	1.45e+8	2.0000	18.08	7.52	350.34
9	354	112	1.59e+8	2.0000	17.98	5.69	319.50
12	311	110	1.71e+8	2.0000	15.80	5.59	297.08
			Total	12.0000	103.72	37.60	1933.84

Enter each layer's trace length to calculate total signal flight time. Via spans may be added to the internal layer length.

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Figure 2: Relative signal propagation of microstrip and stripline (simulated in iCD Design Integrity).

The electric fields surrounding the microstrip exist partially within the dielectric material(s) and partially within the surrounding air. Since air has a dielectric constant (Dk) of one, it will speed up the signal propagation compared to the stripline. Even if the trace widths are adjusted on each layer, so as the impedance is identical, the propagation speed of microstrip is always faster than stripline—typically by 13-17%. The speed of propagation of digital signals is independent of trace geometry and impedance.

If you are aware of this issue, then the flight time (as shown in Figure 2) can be matched to compensate for the varying trace delays, so that at the nominal temperature, all signals running on either microstrip or stripline will arrive at the receiver simultaneously. Alternatively, many routers these days have matched delay routing which enables one to take the flight time variation between microstrip and stripline configurations into account. Note that matched delay is quite different from matched length routing which does not consider flight time.

For the DDR3/4 fly-by configuration, for instance, it is best to route all the critical traces on two symmetrical paired layers. In this case, the paired layers are 1 and 12, 4 and 9, plus 6 and 7. Layers 4 and 9 are best, as they are embedded and close to the plane pairs and active devices of a 12-layer PCB. There are 200-mil fanouts from the microstrip layer to these (not shown). These two layers have identical delays of 319.50 ps and are symmetrical in the stackup embedded between planes. Figure 3 shows the routing directions of the data lanes (0-3) combined with the associated differential strobes and the address, control and command (ACC) signals combined with the differential clock. One does not need to worry about layer-induced flight time skew because layers 4 and 9 are identical.

Figure 4 graphs the relative radiation between outer and inner layers. In this case, the trace routed on the inner layer 4 exhibits between 4 to 10 dB less noise than the trace routed on the top layer. Note that there are radiating harmonics above 40 dB on the top layer routing. Also, high frequency components radiate more

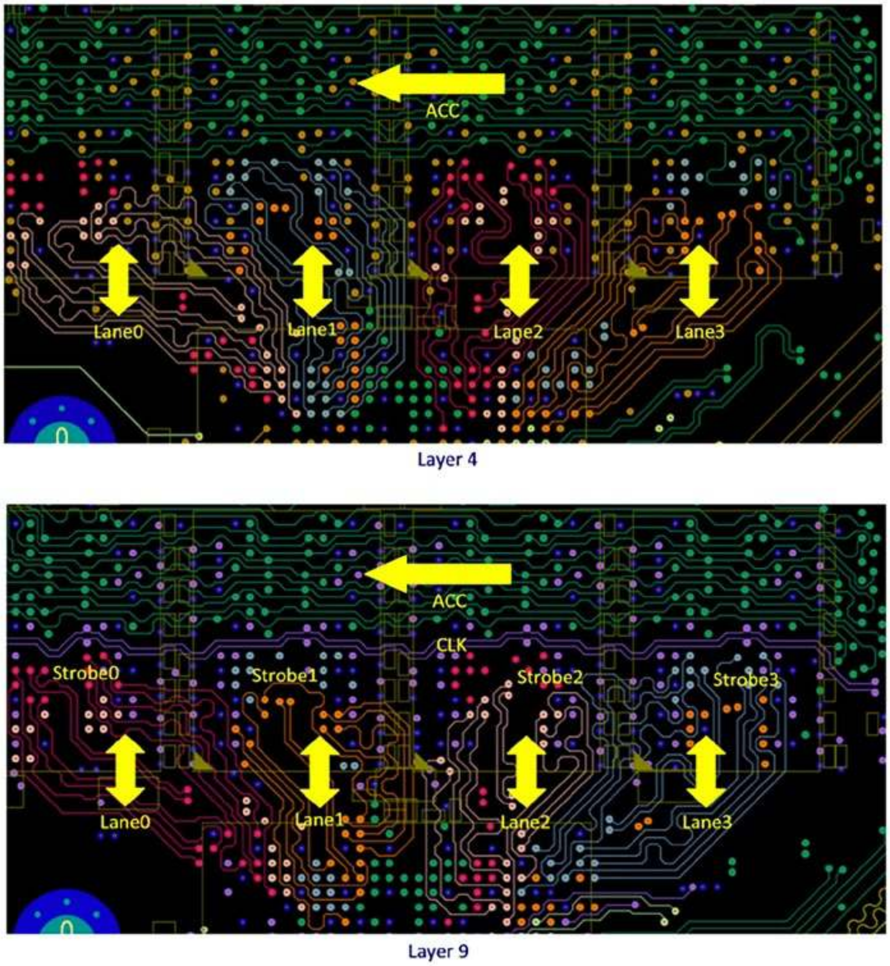

Figure 3: Routing strategy for DDR3 fly-by configuration.

readily because their shorter wavelengths are comparable to trace lengths, which act as antennas. Consequently, although the amplitude of the harmonic frequency components decreases, as the frequency increases, the radiated frequency varies depending on the trace characteristics.

So, apart from the short 200-mil microstrip fanouts, the emissions of this design are well below that of the FCC/CISPR Class B limit (lower red line). Whereas, the radiation would have been 49.73 dB at 6.76 GHz and 52.10 at 7.8 GHz if it was routed on the outer layers, possibly failing testing. If you plan your routing strategy and stackup design prior to commencing the layout, then design for electromagnetic compliance takes very little extra effort.

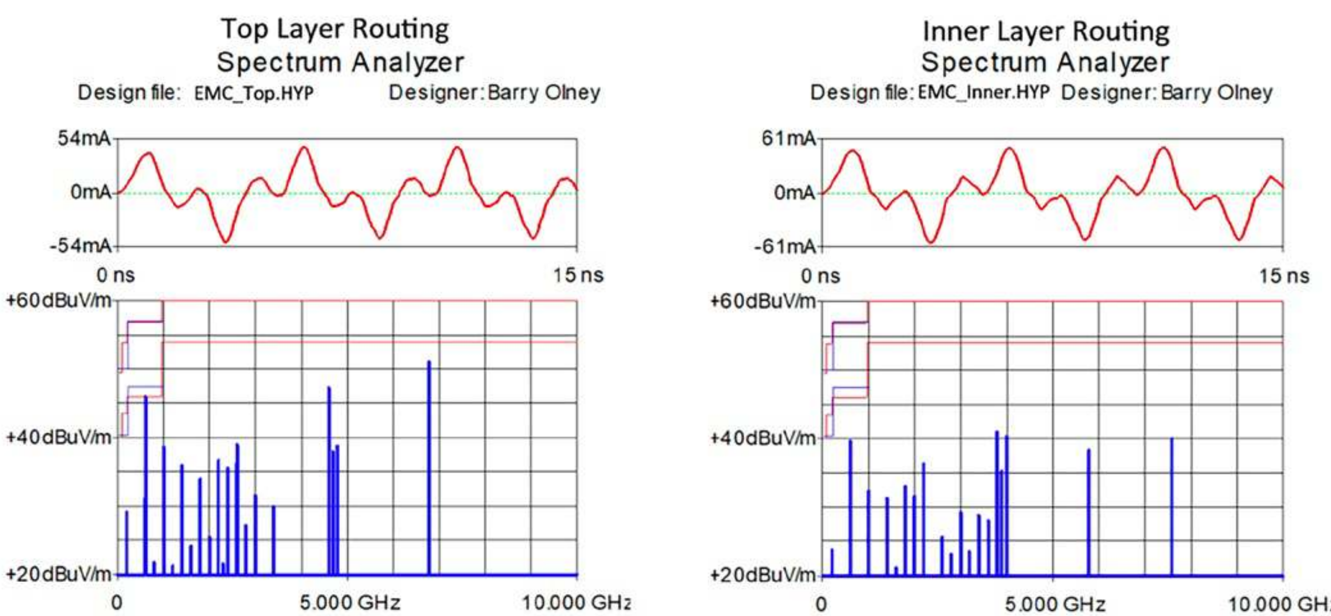

Figure 4: Comparison of radiation from signals routed on the top microstrip layer vs. inner stripline layer.

Key Points

- Embedding signals between the planes reduces these emissions and susceptibility to radiation as well as providing electrostatic discharge protection.
- It is best to keep well away from the edge of the board when routing on the outer microstrip layers.
- On a multilayer PCB, critical signals should be routed on a stripline layer adjacent to a solid reference plane to reduce radiation.
- The propagation speed of microstrip is always faster than stripline—typically by 13-17%.
- Many routers these days have matched delay routing which enables one to take the flight time variation into account.
- The trace routed on the inner layer 4 exhibits between 4 to 10 dB less noise than the trace routed on the top layer.

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Resources

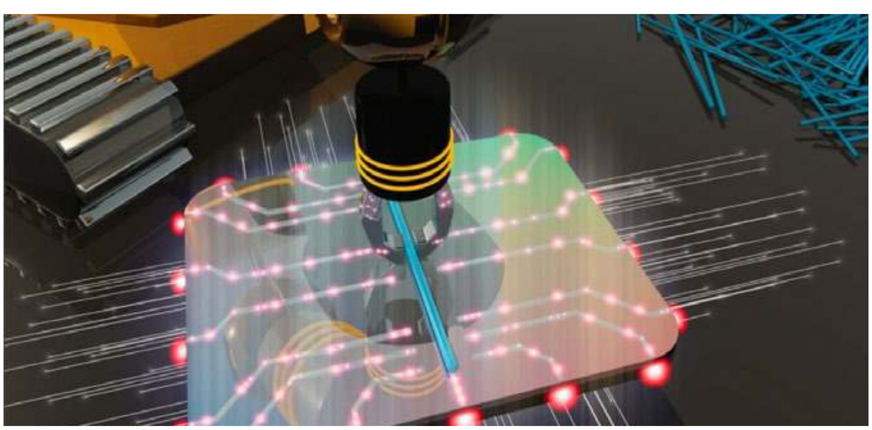
1. Beyond Design by Barry Olney: The Fundamental Rules of High-Speed PCB Design Part 4; Embedded Signal Routing; Signal Flight Time Variance in Multilayer PCBs.

Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded at www.icd.com.au. To read past columns, click here.

Discovery of New Nanowire Assembly Process Could Enable More Powerful Computer Chips

In a newly-published study, a team of researchers in Oxford University's Department of Materials led by Harish Bhaskaran, Professor of Applied Nanomaterials, describe a breakthrough approach to pick up single nanowires from the growth substrate and place them on virtually any platform with sub-micron accuracy.

This technique is readily scalable to larger areas, and brings the promise of nanowires to devices made on any substrate and using any process. This is what makes this technique so powerful.



The innovative method uses novel tools, including ultra-thin filaments of polyethylene terephthalate (PET) with tapered nanoscale tips that are used to pick up individual nanowires. At this fine scale, adhesive van der Waals forces (tiny forces of attraction that occur between atoms and molecules) cause the nanowires to "jump" into contact with the tips. The nanowires are then transferred to a transparent dome-shaped elastic stamp mounted on a glass slide. This stamp is then turned upside down and aligned with the device chip, with the nanowire then printed gently onto the surface.

Deposited nanowires showed strong adhesive qualities, remaining in place even when the device was immersed in liquid. The research team were also able to place nanowires on fragile substrates, such as ultra-thin 50 nanometre membranes, demonstrating the delicacy and versatility of the stamping technique.

(Source: University of Oxford)