

Routing Strategies for High-Speed PCB Design

Beyond Design

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As the typical PCB design becomes more complex, so do the techniques and strategies required—not only to complete the design but also to create a functioning product that performs to specification. Autorouters have improved dramatically over the past 20 years, allowing the PCB designer to produce seemingly hand-crafted results in an incredibly short time. However, the autorouter is guided by design constraints, and there are only so many rules that can be practically defined. Every situation is different, requiring unique tradeoffs. The limiting factor with any autorouter is describing just what it is that human decision-makers actually do.

PCB designers need to understand the underlying high-speed issues of the design based on simulation (Figure 1) and then translate these into corresponding design constraints. Constraints can always be altered on the fly if a particular constraint is too tight, providing the designer can justify the easing of the specification and that the product is still manufacturable.

Firstly, a pre-layout simulation defines the extent of placement. Controlling the placement of devices limits maximum trace length, reduces flight-time-delay and skew, and assists in compliance with timing specifications. To obtain a high route-completion rate, component

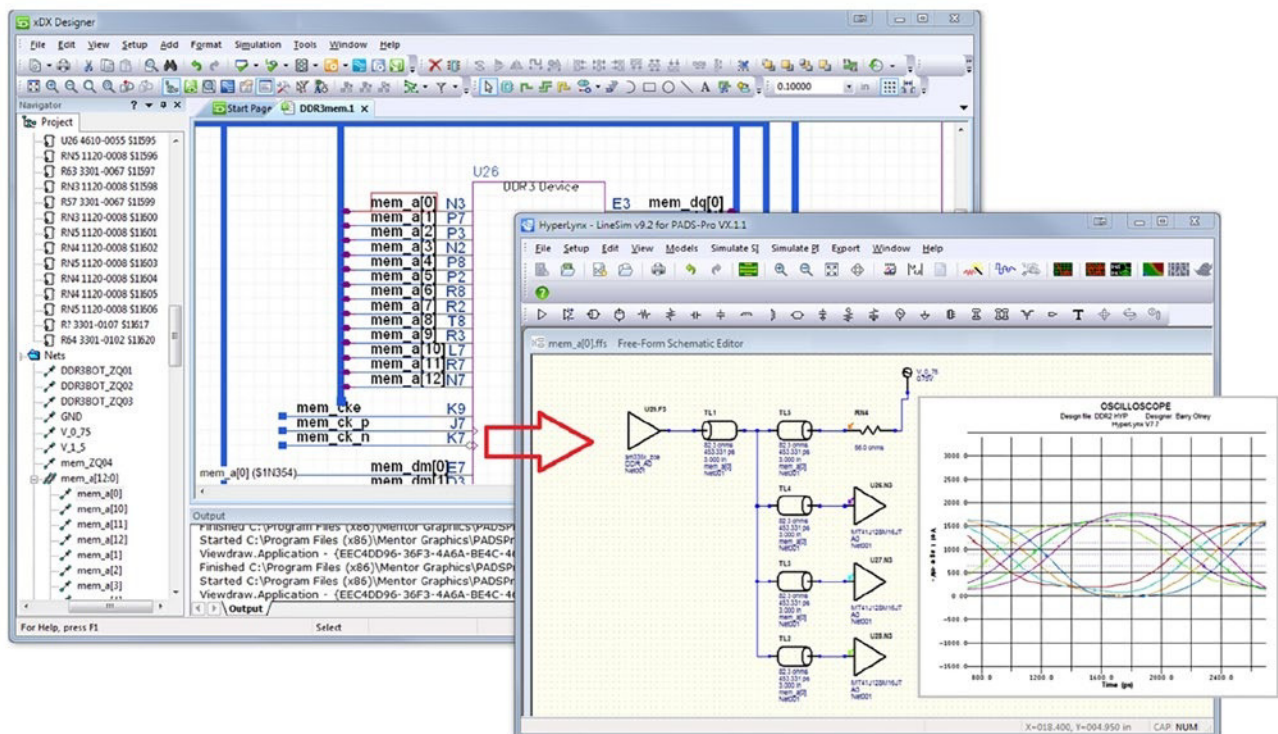


Figure 1: Develop high-speed design constraints based on pre-layout simulation.

placement is extremely important. If the board is difficult to route, it may just be the result of poor placement, slots/gates positioned all over the board, or perhaps the sequence of pins on components are flipped. We need to assist the router as much as possible by opening route channels and providing space for vias.

Secondly, there are six important issues to consider before you commence with the process of formally routing the board:

1. The stackup should be planned to ensure that controlled impedance signals have been calculated correctly and that the return current for each signal layer has a clear return path. The resulting stackup configuration should then be transferred to the design rules to define the correct trace width and clearance for each layer and to specify the differential pairs.
2. The power distribution network (PDN) should be planned and bypass and decoupling capacitors placed in the appropriate positions. The iCD PDN Planner is an ideal sandbox for this analysis. It is a good idea to color the power nets with individual colors so that they can easily be recognized without having to name the net.
3. Design rules and constraints can be passed from the schematic, which automatically sets the design rules in the PCB database, though there is always some adjustment to be done on the PCB side.

4. Via sizes for different net classes need to be defined. This is important for route completion.
5. For rules to properly support the design process, they need to be defined in the correct priority so that the most important rules prevail over rules of lesser importance.
6. Set up the routing options. It amazes me that most EDA tools do not come with the router set to the most useful functions straight out of the box. Before routing, one must tweak the route options to get the tool to do what you want. Details vary by the tool, of course, but the nuisance is near-universal.

Thirdly, most popular EDA tools have the ability to cross-probe between the schematic and the router. This is a fantastic feature that enables a PCB designer to build up an extremely dense, complex route in a couple of hours by controlling the router from the schematic rather than just pushing the autoroute button and hoping for the best.

Cross-probing can also be used as a powerful search tool, locating parts and nets on the schematic or PCB. And cross-probing is not limited to schematic and PCB. Mechanical tools allow the cross-probing between PCB and 3D MCAD database, enhancing mechanical visualization of the product.

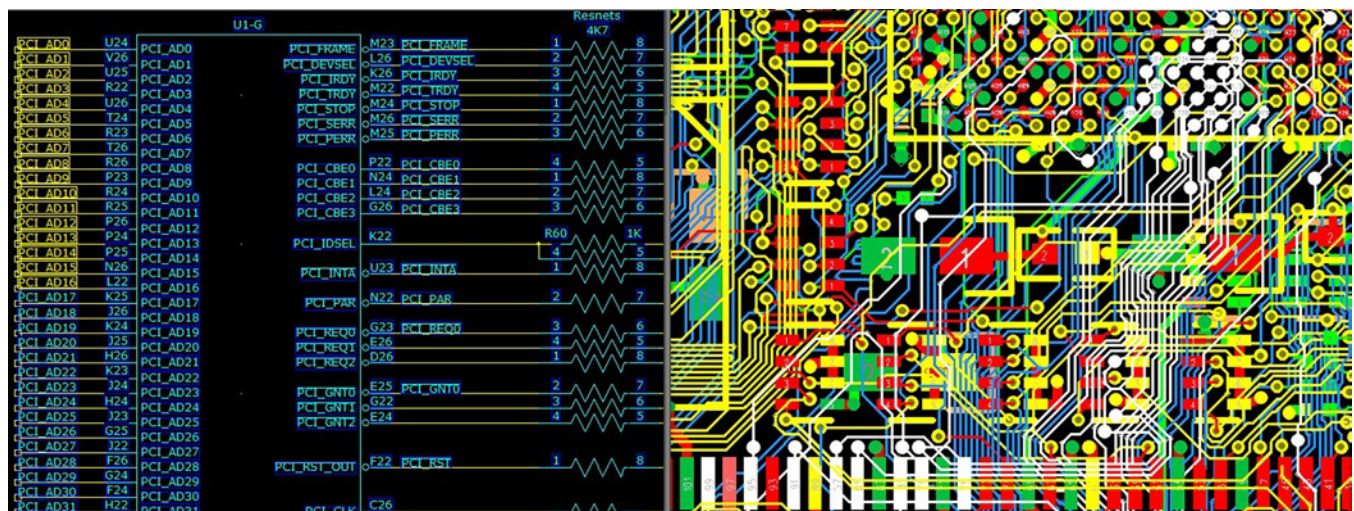


Figure 2: Cross-probing from schematic to router of part of the PCIe bus.

Finally, one should avoid routing high-speed signals on the outer microstrip layers of a multilayer PCB. This can decrease radiation by up to 10 dB. Plus, inner stripline traces are less susceptible to outside noise as they are sandwiched between two planes.

The four constraints to keep in mind are as follows:

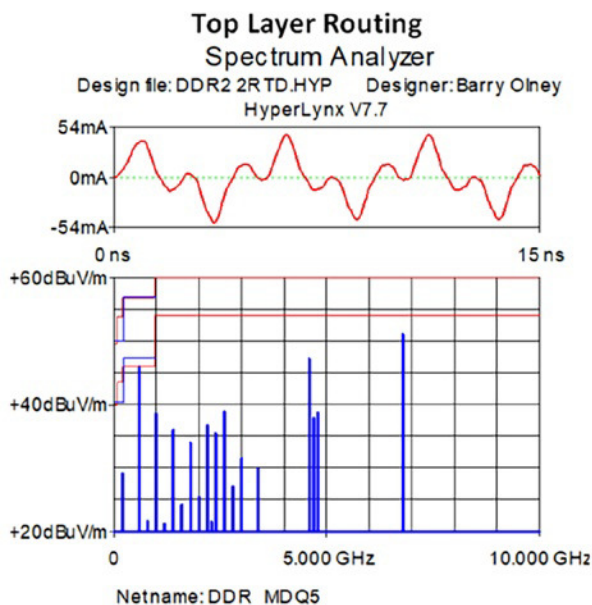
1. Keep the mark to space ratio of the waveform equal as this eliminates all the even harmonics leaving only the odd harmonics.
2. Route high-speed signals out from the center of the board where possible as any radiation will be in the opposite direction and will tend to cancel out.
3. Route high-speed signals between the planes. Fan-out close to the driver (200 mils), dropping to an inner plane, and route back up to the load again with a short fan-out.
4. Use the same reference plane for the return signals, as this reduces the loop area and hence radiation.

Let's make a comparison of the radiated noise between the top layer and inner layer routing, as in Figure 3.

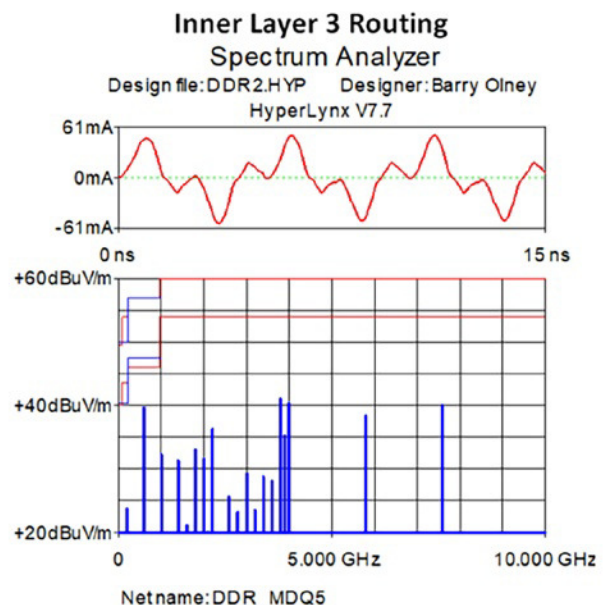
As you can see (with all other factors being equal), in this case, the trace routed on inner layer 3 exhibits 4–10 dB less noise than the trace routed on the top layer. The high-frequency components radiate more readily because their shorter wavelengths are comparable to trace lengths, which act as antennas.

You do not need to do any manual routing yourself to get an acceptable route of the non-critical nets. Of course, matched delay, differential pairs, and other critical signals should be routed with the precision they demand. This is the process:

1. Start by placing all the components by functionality, selecting the desired component on the schematic, and placing it in the best location/rotation to aid the routing.
2. Similarly, when routing, select a chip on the schematic (the nets are highlighted on the PCB) and then fan-out with the router.



Top layer Harmonics:
 46 dB @ 595 MHz
 45.65 dB @ 4.595 GHz
 49.73 dB @ 6.76 GHz



Inner layer 3 Harmonics:	Difference:
39.69 dB @ 619 MHz	6 dB
41 dB @ 3.8 GHz	4 dB
40 dB @ 7.57 GHz	10 dB

Figure 3: Comparison of radiation from microstrip and stripline routing.

3. Select the critical nets on the schematic, fan-out, and then route with the auto-router.
4. Push and shove the traces to the desired location, move on to the next group of nets, and repeat. Each group of routed traces should be verified after completion. Lock if necessary.

When you drive the router from the schematic, it's possible to see what needs to be done without entering too many conditional design rules, and you can later manipulate the traces as if they were hand-routed.

Once the routing is complete, apart from running design rule checks (DRCs), run a sanity check on the board. You can either do this in the simulation environment or the PCB database. Simply highlight each net one by one. This is tedious but gets results. You can quickly see if any nets are longer than the Manhattan length or spiral around the board before termination.

Key Points

- The autorouter is guided by design constraints, and there are only so many rules that can be practically defined. Every situation is different, requiring unique tradeoffs.
- The underlying high-speed issues of the design need to be translated into corresponding design constraints.
- A pre-layout simulation defines the extent of placement.
- If the board is difficult to route, it may just be the result of poor placement.

- The stackup configuration and PDN needed to be addressed before commencing routing.
- Cross-probing enables the PCB designer to build up an extremely dense, complex route in a couple of hours by controlling the router from the schematic.
- Cross-probing can also be used as a powerful search tool, locating parts and nets on the schematic or PCB.
- One should avoid routing high-speed signals on the outer microstrip layers of a multilayer PCB. This can decrease radiation by up to 10 dB. **DESIGN007**

Further Reading

- B. Olney, "Beyond Design: High-Speed PCB Design Constraints," *Design007 Magazine*, May 2019.
- B. Olney, "Beyond Design: Embedded Signal Routing," *The PCB Magazine*, September 2011.
- B. Olney, "Beyond Design: Interactive Placement and Routing Strategies," *The PCB Design Magazine*, December 2012.
- B. Olney, "Beyond Design: Routing Techniques for Complex Designs," *The PCB Design Magazine*, January 2013.
- B. Olney, "Beyond Design: Critical Placement," *The PCB Magazine*, September 2012.



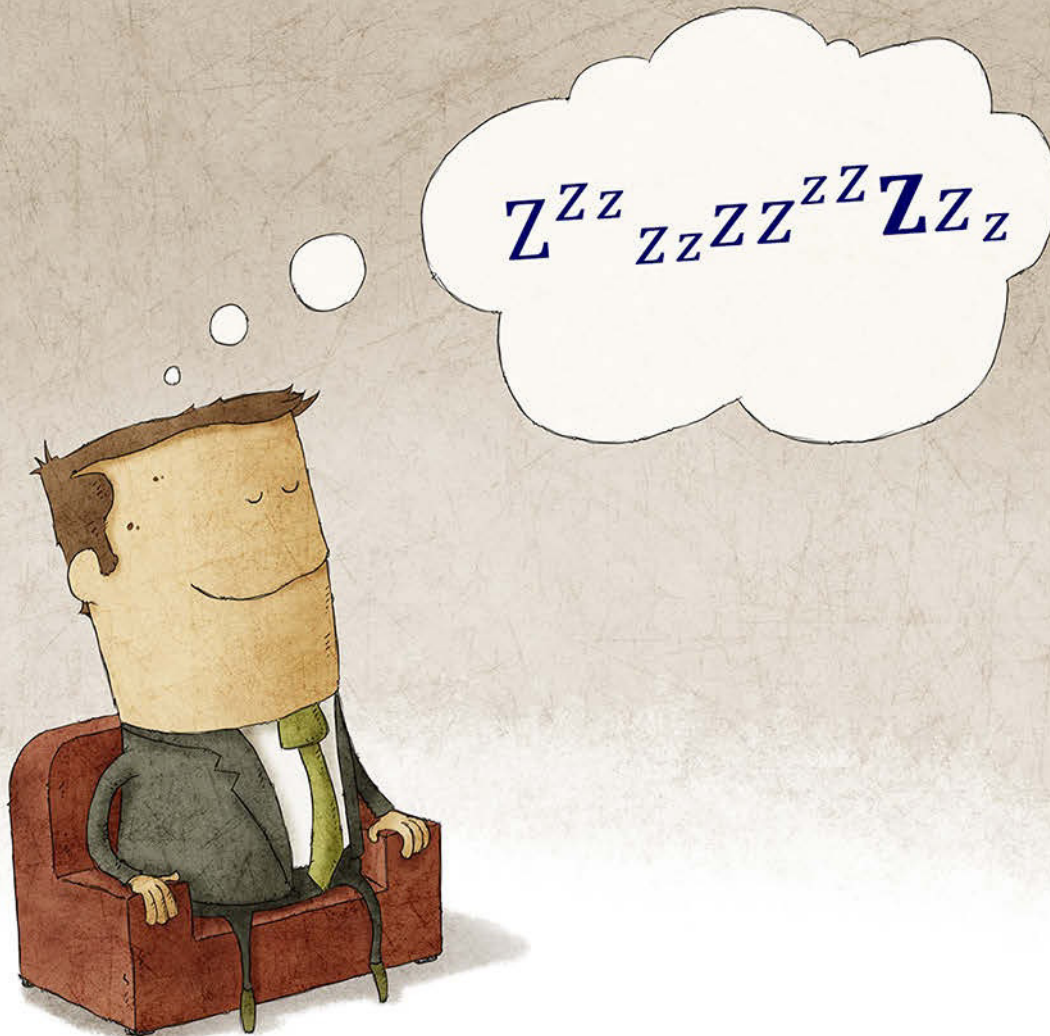
Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded at icd.com.au. To read past columns or contact Olney, [click here](#).

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