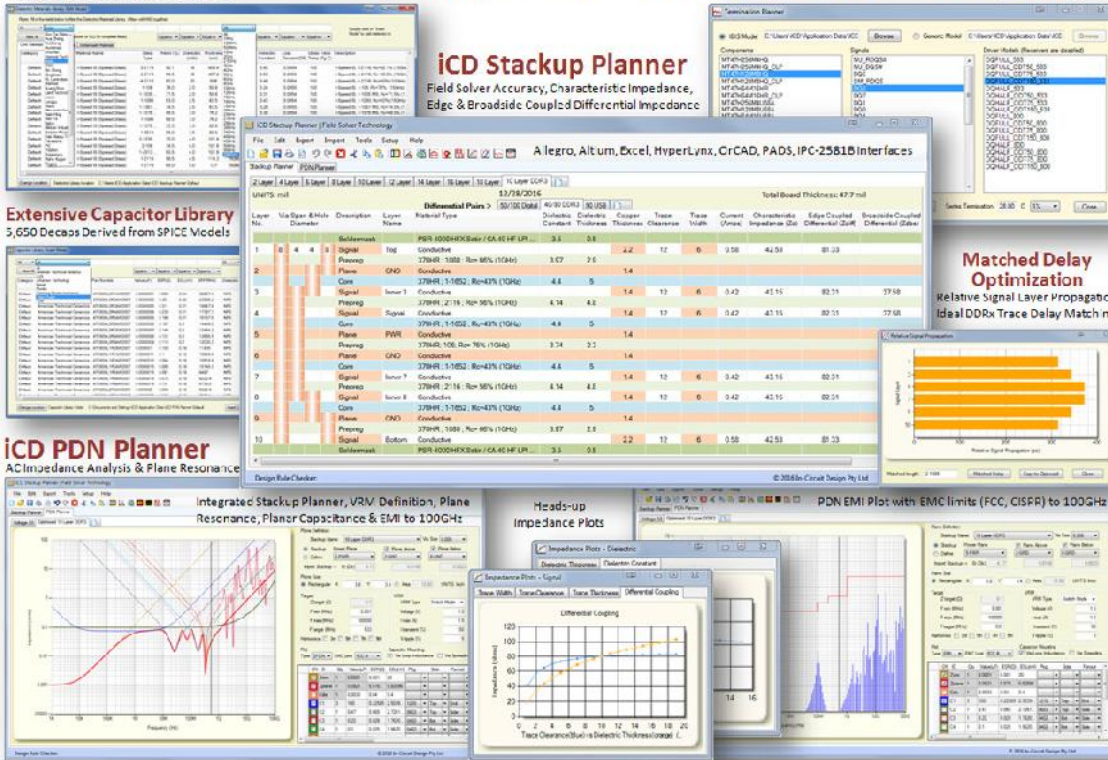


iCD Design Integrity

Incorporates the iCD Stackup and PDN Planner software. Offers PCB Designers unprecedented simulation speed, ease of use & accuracy at an affordable price

Dielectric Materials Library
30,700 Rigid & Flex Materials to 100GHz

Termination Planner
Extracts V Curves from IBIS Models
Calculates Series Terminator of the Distributed System including Loads



Extensive Capacitor Library
5,650 Decaps Derived from SPICE Models

Matched Delay Optimization
Relative Signal Layer Propagation
Ideal DDRx Trace Delay Matching

iCD PDN Planner
AC Impedance Analysis & Plane Resonance

iCD Stackup Planner

Offers Engineers & PCB Designers unprecedented simulation speed, ease of use and accuracy at an affordable price

- Industry Leading 2D (BEM) Field Solver precision
- Characteristic impedance, edge-coupled & broadside-coupled differential impedance
- Relative Signal Propagation with 'Matched Delay Optimization'—ideal for DDRx design
- Termination Planner - series termination based on IBIS models & distributed system
- Unique Field Solver computation of multiple differential technologies per signal layer
- Extensive Dielectric Materials Library—over 30,700 rigid & flexible materials up to 100GHz
- Interfaces—Allegro, Altium, Excel, HyperLynx, OrCAD, PADS, Zmetrix TDR, Zuken & PC-2581B

iCD PDN Planner

Analyze multiple power supplies to maintain low AC impedance over entire frequency range dramatically improving product performance

- Fast AC impedance analysis with plane resonance and projected EMI
- Definition of plane size, dielectric constant & plane separation
- Extraction of plane data from the integrated iCD Stackup Planner
- Definition of voltage regulator, bypass/decoupling capacitors, mounting loop inductance
- PDN EMI Plot with FCC, CISPR & VCCI Limits. Frequency range up to 100GHz
- Extensive Capacitor Library—over 5,650 capacitors derived from SPICE models

“iCD Design Integrity software features a myriad of functionality specifically developed for high-speed design.”

- Barry Olney



The Dark Side – Return of the Signal

by Barry Olney

IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

All PCB designers should be aware of the impact of crosstalk on signal integrity. As signal traces come into close proximity, of an aggressor signal, part of that signal is unintentionally electromagnetically coupled into the victim trace as noise. I have mentioned before that current flow is a round trip—the current must return to the source to complete the loop. What about crosstalk in the return path, of the reference planes, as the current weaves its way back through the expansive wasteland of copper? This month's column follows on from my April column, "Return Path Discontinuities," and elaborates on crosstalk in the unseen "dark side" of the signal.

I guess we all think of a copper plane as a thick, solid plate of copper that can basically

handle any amount of current we sink into it. It also serves to make the circuit layout easier, allowing the PCB designer to ground anything, anywhere without having to run multiple tracks. That may well be the case with DC or very low-frequency analog circuits, but certainly not in the case of high-speed design. The return current takes the path of least inductance in the nearest plane(s). Returning signal currents tend to stay in close proximity to their signal conductors, falling off in intensity with the square of increasing distance.

However, as the frequency increases, the current is forced into the outer surface of the copper, due to the skin effect, dramatically increasing loss leaving a section of unused copper in the center of the plane. This redistribution



Figure 1: See you on the dark side of the moon (Courtesy of NASA).

of current causes the resistance per length to increase and the loop inductance per length to decrease. As frequency increases beyond 1 GHz, the resistance continues to increase while the loop inductance reaches a limiting value. The higher the frequency, the greater the tendency for current to flow in the outer surface of the conductor. The skin depth is given by:

$$\delta = \sqrt{\frac{2}{2\pi f \mu \sigma}}$$

where δ is the skin depth in microns, f is the frequency in MHz, μ is the magnetic permeability ($4 \pi \times 10^{-7} \text{H/m}$) and σ is the copper conductivity, typically ($5.6 \times 10^7 \text{ S/m}$).

Looking at this equation, it is apparent that skin depth decreases with increased frequency. Figure 2 shows the skin depth compared to frequency. At low frequency (1 MHz), the skin depth is 66 μm but this decreases to 0.66 μm at 10 GHz. Above 1 GHz, only the very outer surface of the plane conducts the current. The red horizontal lines represent the plane copper weight and thickness. This shows that at about 30 MHz, a signal traveling in a 1/2oz (17.78 μm) copper plane would not use the entire plane cross-section but rather the skin effect would begin to have an impact. This implies that at high frequencies, the thickness of the copper plane is irrelevant; 1/2 oz and 3 oz copper will have the same surface conduction area and hence will only transfer the same amount of current.

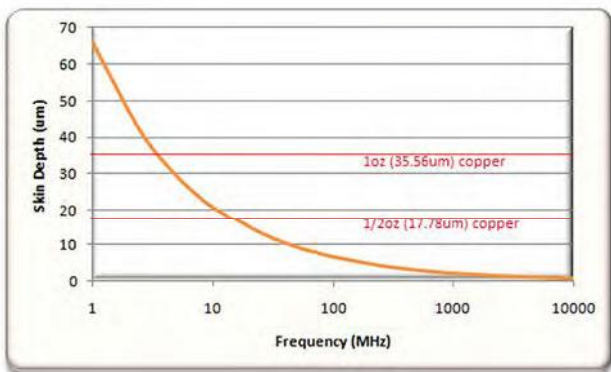


Figure 2: Skin depth (um) vs. frequency (MHz).

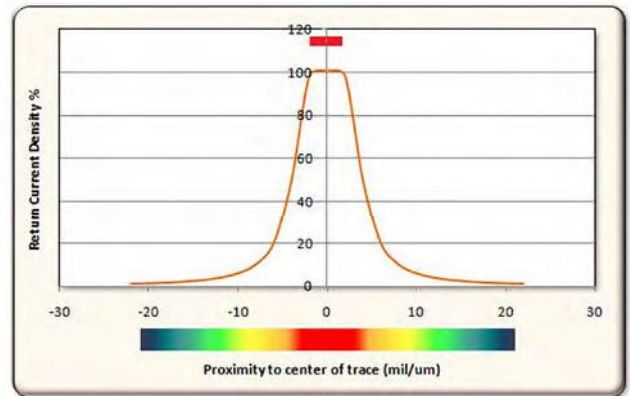


Figure 3: Microstrip return current density.

As seen in Figure 3, the return current distribution, in the plane surface of a microstrip configuration, is reduced as the distance to the center of the trace increases. Here we see a balance of two opposing forces:

- Too narrow a distribution increases inductance as narrow traces have more inductance than broad ones
- Too broad a distribution increases inductance by increasing the loop area

So, there is a sweet spot where the total energy stored in the electromagnetic (EM) field surrounding the trace is optimized. Crosstalk between two or more conductors depends on their mutual inductance and mutual capacitance. The inductance plays the major role in this coupling. The signal return currents will generate EM fields. Those EM fields, in turn, induce voltages (crosstalk) into other signals.

It can be seen in Figure 4 that the differential impedance or the coupling of two parallel traces, levels off at 100 ohms above 12 mils trace clearance (blue curve). This is simulated quickly by multiple passes of the field solver. All other factors being equal, the differential impedance will always be 100 ohms regardless of increased spacing. This also represents the point at which crosstalk (coupling) begins. This curve provides a clear map of the design space and efficiently defines the stackup configuration for single ended and coupled pairs. In this case, once the separation is less than 12 mils, the two traces begin to couple and transfer electromagnetic energy.

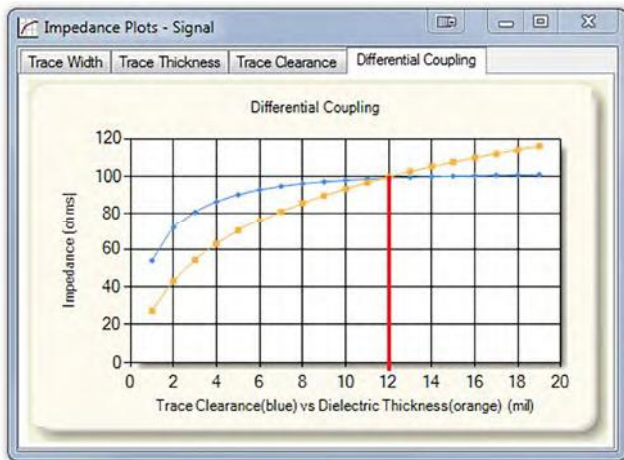


Figure 4: Coupling levels off above 12 mils separation (simulated by the iCD Stackup Planner).

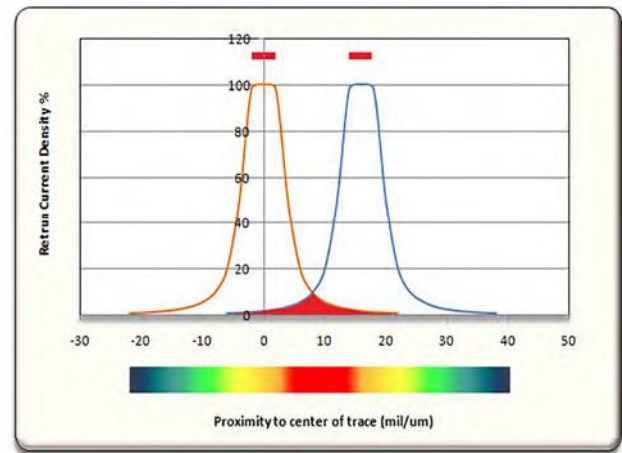


Figure 5: Parallel traces and return path crosstalk.

The easiest way to reduce crosstalk, from a nearby aggressor signal, is of course to increase the spacing between the signals in question. Doubling the spacing cuts the crosstalk to roughly a quarter of its original level. However, crosstalk is determined by the ratio of the trace separation and also the height of the trace above the plane. By varying the trace height, one can also control the coupling—hence crosstalk. If real estate is limited, then this may be a better solution rather than increasing routing density. A tight coupling (less height) results in less crosstalk.

The return current distribution of two parallel traces (Figure 5) shows an overlap of current in the surface of a microstrip plane. In fact, the overlap will be larger at lower frequencies where the return currents tend to spread out and not follow a tight path under the trace. Also, as the voltage increases so does the coupled noise. This is a good reason not to intermingle dissimilar technologies but rather keep them isolated.

If we look into it further, the degree of crosstalk is also dependent on several other factors including driver strength (which can normally be adjusted in the firmware), transmission line length, how far the segments run closely in parallel and signal rise time. In the case of long transmission line lengths, a series terminator slows the signal rise/fall time and reduces reverse-coupled

crosstalk at the near end improving crosstalk considerably.

With all of these issues, to take into account, how do we ever get high-speed transmission lines, particularly those with wide parallel buses, to work efficiently? Fortunately, synchronous buses, as typically used in DDRx designs, benefit from an extraordinary immunity to crosstalk. Crosstalk only occurs when the signals are being switched and this crosstalk only has an affect within a small window around the moment of clocking. So, providing the receiver waits sufficiently long enough for the crosstalk to settle before sampling the bus, the crosstalk has no impact on the signal quality at the receiver. It's all about timing—ensuring that the required setup and hold times are provided at the receiver.

Remember: *“Beware the dark side. Anger, fear, aggression; the dark side of the Force are they. Easily they flow, quick to join in a fight. If once you start down the dark path, forever will it dominate your destiny, consume you it will.”* —Yoda

Points to Remember

- Current must return to the source to complete the loop.
- Returning signal currents tend to stay in close proximity to their signal conductors, falling off in intensity with the square of increasing distance.

- As the frequency increases, the current is forced into the outer surface of the copper, due to the skin effect.
- Skin depth decreases with increased frequency.
- At high frequencies, the thickness of the copper plane is irrelevant—½ oz. and 3 oz. copper will have the same surface conduction area.
- There is a sweet spot where the total energy stored in the electromagnetic field surrounding the trace is optimized.
- The signal return currents generate EM fields. Those EM fields, in turn, induce voltages (crosstalk) into other signals.
- The easiest way to reduce crosstalk is to increase the spacing between the signals in question.
- Crosstalk can also be controlled by varying the trace height, above the plane. A tight coupling (less height) results in less crosstalk.
- The return current distribution of two parallel traces shows an overlap of current in the surface of a microstrip plane.
- To minimize crosstalk do not to intermingle dissimilar technologies but rather keep them isolated.

- Synchronous buses, as typically used in DDRx designs, benefit from an extraordinary immunity to crosstalk.
- Ensure that the required setup and hold times are provided at the receiver.

References

1. Barry Olney's Beyond Design columns: [Return Path Discontinuities](#), [The Dumping Ground](#), [Controlling the Beast](#), [Effects of Surface Roughness on High-speed PCBs](#), [Uncommon Sense](#).
2. [High-Speed Digital System Design](#), by Steven H. Hall, Garrett W. Hall, and James A. McCall
3. [High-Speed Digital Design](#), by Howard Johnson and Martin Graham



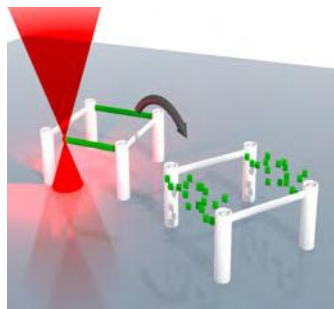
Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN and CPW Planner, is a PCB design service bureau and specializes in board-level simulation. The software can be downloaded from www.icd.com.au. To contact him or read past columns, [click here](#).

Erasable Ink for 3D Printing

Researchers of Karlsruhe Institute of Technology (KIT) have now developed a method to erase the ink used for 3D printing. In this way, small structures of up to 100 nm in size can be erased and rewritten repeatedly. This development opens up many new applications of 3D fabrication in biology or materials sciences.

"Developing an ink that can be erased again was one of the big challenges in direct laser writing," Professor Christopher Barner-Kowollik of KIT's Institute for Chemical Technology and Polymer Chemistry says.

The process was developed in close cooperation with the group of Professor Martin Wegener at the Institute of Applied Physics and the



Institute of Nanotechnology of KIT.

Structures written with erasable ink can be integrated into structures made of non-erasable ink: Support constructions can be produced by 3D printing, which are similar to those used when building bridges and removed later on. Recently, such structures were designed by KIT to grow cell cultures in three dimensions on the laboratory scale.

"During cell growth, parts of the 3D microstructure could be removed again to study how the cells react to the changed environment," Wegener explains. According to the scientists, it is also feasible to produce reversible wire bonds from erasable conducting structures in the future.