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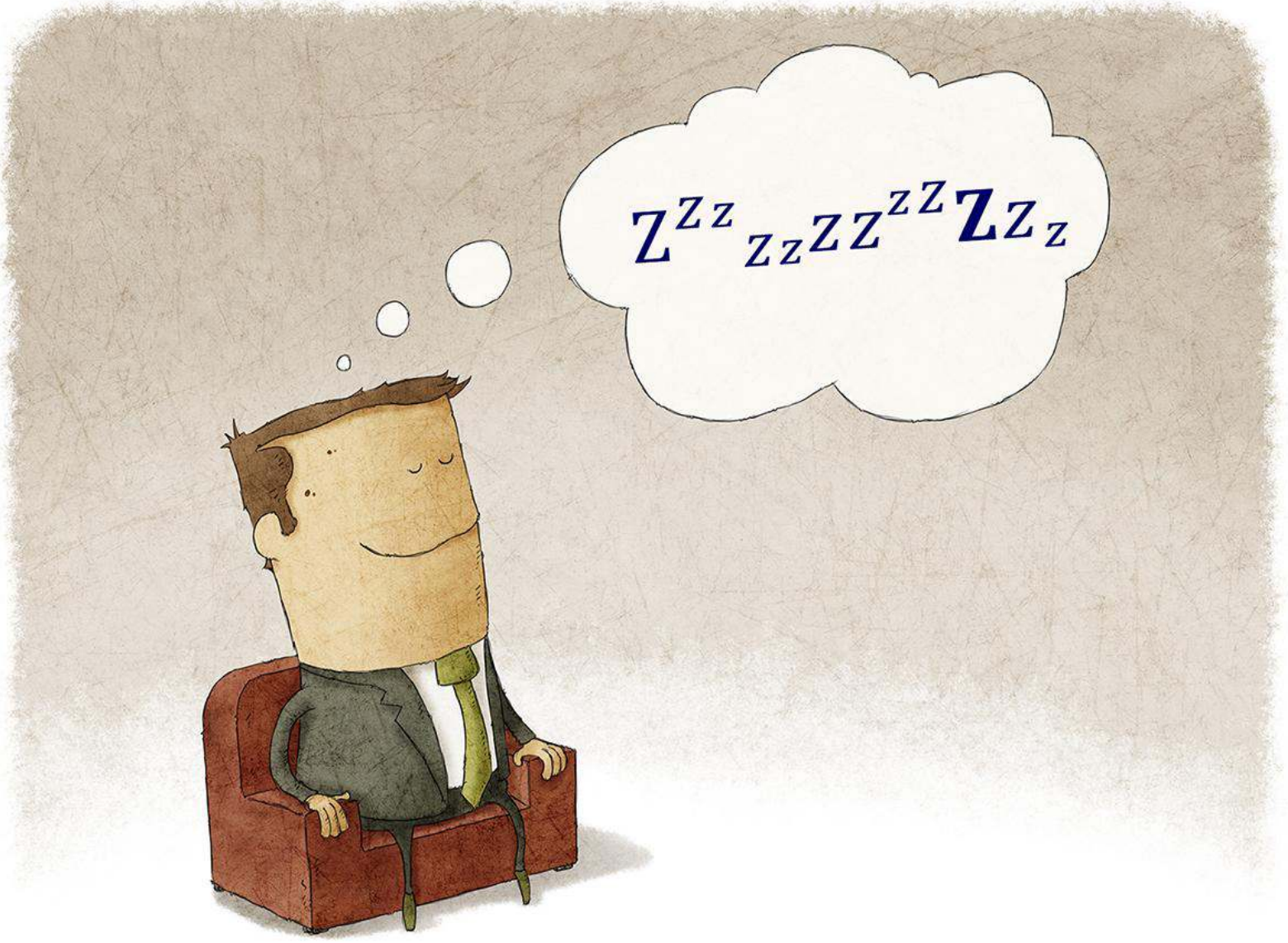

Did you know that two seemingly unrelated concepts are the foundation of a product's performance and reliability?

- Transmission line impedance and
- Power Distribution Network impedance

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Return Path Optimization

Beyond Design

by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

High-speed PCB design is not as simple as sending a signal from the driver to the receiver over a transmission line. One should also consider the presence and interaction of the power distribution network (PDN) and how and where the return current flows. A logic schematic diagram masks detail crucial to the operation of unintentional signal pathways vital to the understanding of signal performance, crosstalk, and electromagnetic emissions. The PCB designer needs to be able to visualize the connectivity of the return current flow to avoid large loop areas that increase series inductance, degrade signal integrity, and increase crosstalk and electromagnetic radiation.

We think of a copper plane as a thick, solid amount of current we sink into it. It also serves to make the circuit layout easier, allowing the PCB designer to ground anything anywhere without having to run multiple tracks. That may well be the case with DC or very low-frequency analog circuits, but certainly not in the case of high-speed design. The return displacement current takes the path of least inductance in the nearest plane(s). Returning signal currents tend to stay near their signal conductors, falling off in intensity with the square of increasing distance.

Ground impedance is at the root of virtually all signal and power integrity problems; low ground impedance is mandatory for both. This is readily achieved with a continuous ground

difficult with the addition of more and more plane layers on a multilayer PCB. A ground plane serves well as a signal return, provided the ground is continuous under the signal path. But even with a continuous return path, there may be enough voltage drop across the plane to generate a common mode voltage.

If left unchecked, it may escape as electromagnetic emissions via the signal or power/ground conductors. Return path discontinuities have a huge impact on supply bounce of single-ended signals. Fortunately, differential signaling dramatically reduces this effect. Serial interfaces also significantly reduce the number of interconnects, which is another advantage over the use of parallel buses for high-speed design.

Small discontinuities, such as vias and nonuniform return paths on a bus, are becoming an important factor for the signal integrity and timing of high-speed systems. These produce impedance discontinuities due to the local return inductance and capacitive changes. Impedance discontinuities create reflected noise, contribute to differential channel-to-channel noise, and may promote mode conversion. In the case of differential pairs, the transformation from differential-mode to common-mode typically takes place on bends and non-symmetrical routing near via and pin obstructions, but can also be caused by small changes in impedance due to return path issues.

One must also understand the importance of referencing and how to control the return displacement current flow of a signal. Each signal layer should be adjacent to, and closely coupled to, a reference plane, which creates a clear, uninterrupted return path and eliminates broadside crosstalk. As the layer count increases, this concept becomes easier to implement but decisions regarding return current paths become more challenging.

Although power planes can be used as reference planes, ground is more effective as local stitching vias can be used for the return current transitions, rather than stitching decoupling capacitors

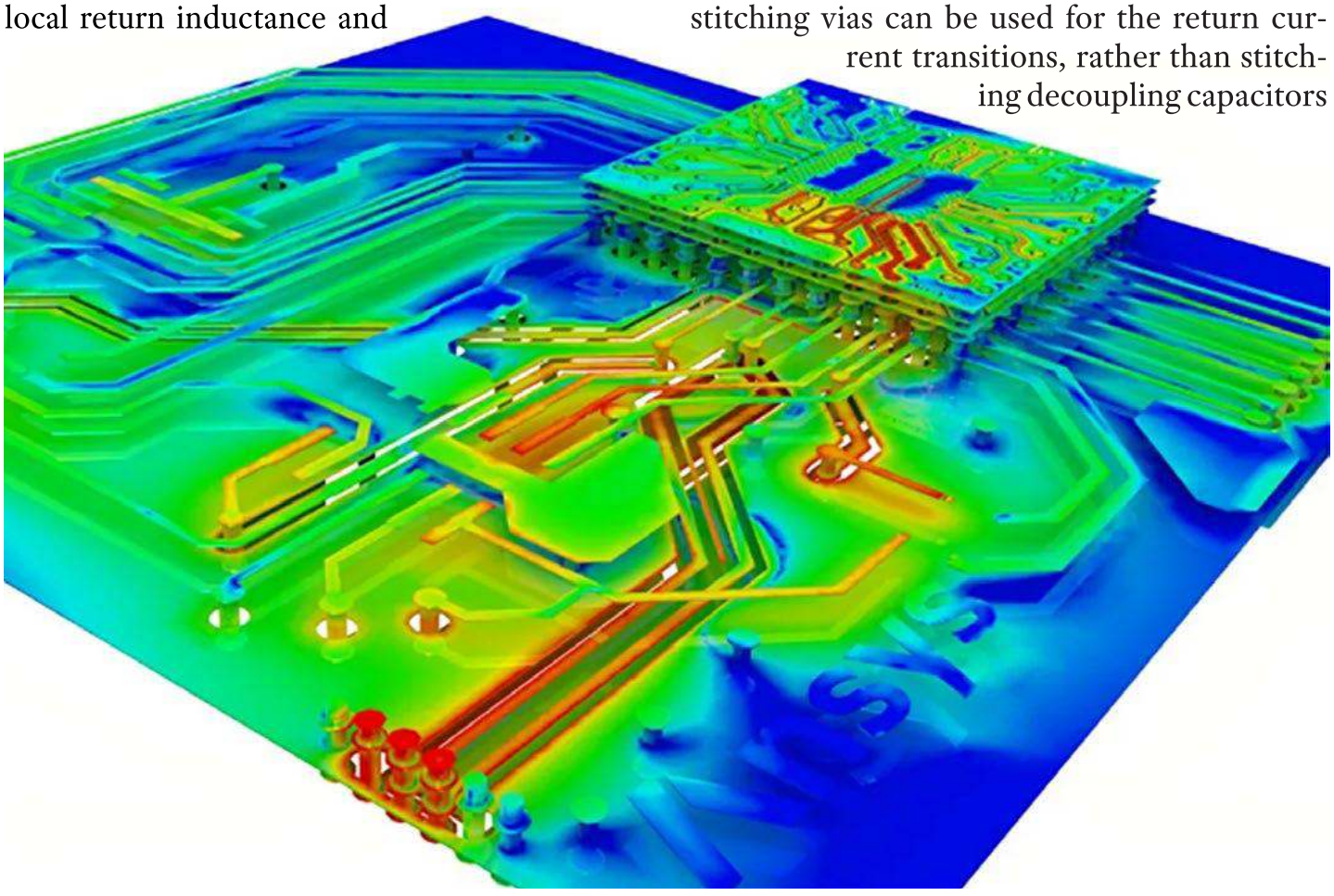


Figure 1: HFSS simulation of return paths. (Source: Ansys)

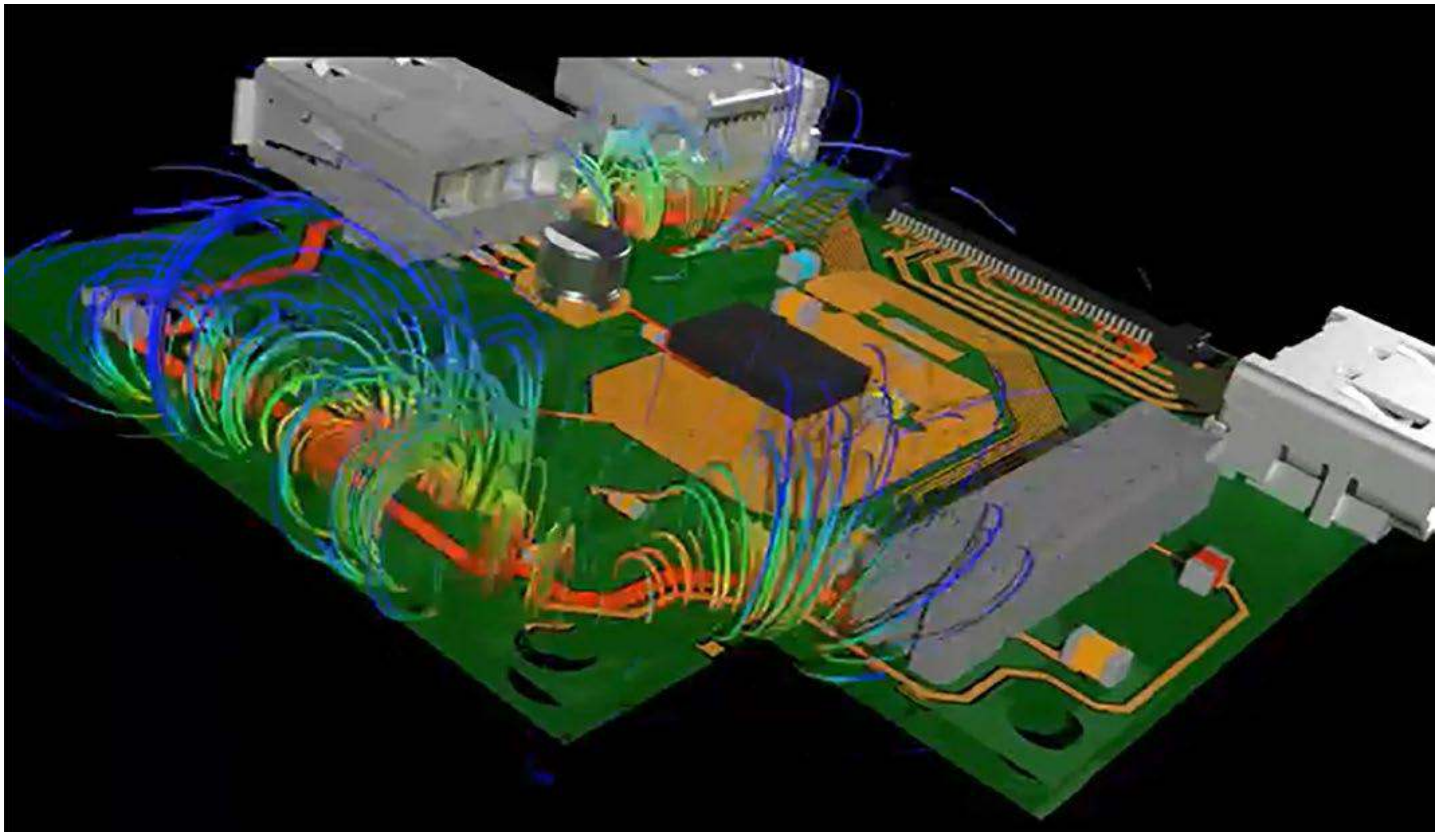


Figure 2: HFSS simulation of electromagnetic energy in microstrip. (Source: Juliano Mologni)

which add inductance. This keeps the loop area small and reduces radiation. As the stackup layer count increases, so does the number of possible combinations of the structure. But if one sticks to the basic rules then the best-performing configurations are obvious.

Figure 2 shows the electromagnetic fields emanating from signal traces in a microstrip configuration. Electric fields terminate when they come into contact with a solid plane but will radiate into the surrounding volume while magnetic fields tend to radiate unless they are shielded by the planes. But in a stripline configuration, the fringing fields still radiate from the board edges.

The return current of a high-speed, fast-rise time digital signal will always follow the path of least inductance, which is directly beneath the signal path. However, discontinuities tend to divert the return current increasing the loop area, inductance, and delay, which is not desirable. The best way to identify the discontinuities is to follow the signal path and imagine the return path closely coupled on the nearest plane. If there are multiple planes present in the layer stack, then the displacement current will still take the path of least inductance and follow closely coupled to the signal trace. If a discontinuity interrupts this return flow, then the return current will be forced into a distant plane where it has a clear run, creating increased inductance.

A via that provides the connection between signal traces, referenced to different planes, creates discontinuities. In other words, the return current has to jump between the planes to close the current loop, which in turn increases the inductance of the current loop, affecting the signal integrity. This return current also excites the parallel plate mode, causing significant EMI. If the reference planes are at the same DC potential, then they can be connected by stitching vias near the signal via transition to provide shorter paths for return currents. However, if the planes are at different DC potentials, then decoupling capacitors must be connected across the planes at these

points. In addition, some of the return current flows through the interplane capacitance to close the loop.

To avoid these issues, there are fundamental rules to follow such as:

- Never allow a high-speed signal to cross a gap or split in the plane. This creates a large return path loop area and tends to radiate.
- Never route a high-speed signal near the edge of the reference plane. The fringing fields may wrap around the edge of the board and radiate.
- Never place an IC over a split plane (with the exception of DAC/ADC). The IC substrate is like a miniature multilayer PCB and may rely on a solid plane placed beneath the IC to provide a continuous return path.
- Each signal layer should be adjacent to, and closely coupled to, a reference plane, which creates a clear, uninterrupted return path and eliminates broadside crosstalk.
- A ground via needs to be placed close to every layer transition to provide a clear path for the return current.

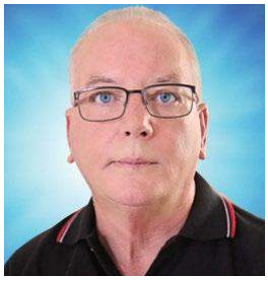
Unfortunately, discontinuities can never be totally eliminated but we can take steps to significantly minimize the effects. As with PDN planning, it is all about inductance. If the return path loop area is increased in any way, then the inductance will also increase.

Key Points

- A logic schematic diagram masks detail crucial to the operation of unintentional signal pathways.
- The PCB designer needs to be able to visualize the connectivity of the return current flow in order to avoid large loop areas.
- The return displacement current takes the path of least inductance in the nearest plane(s).
- Ground impedance is at the root of virtually all signal and power integrity problems; low ground impedance is mandatory for both.
- A ground plane serves well as a signal return, provided the ground is continuous under the signal path.
- Return path discontinuities have a huge impact on supply bounce of single-ended signals.
- Small discontinuities, such as vias and non-uniform return paths on a bus, are becoming an important factor for the signal integrity and timing of high-speed systems.
- One must also understand the importance of referencing and how to control the return displacement current flow of a signal.
- As the stackup layer count increases, so does the number of possible combinations of the structure.
- Discontinuities tend to divert the return current increasing the loop area, inductance, and delay. **DESIGN007**

Resources

1. Beyond Design: "The Dark Side-Return of the Signal," "Return Path Discontinuities," by Barry Olney.



Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded at www.icd.com.au. To read past columns, click here.