

Reflecting on Reflections

Beyond Design

by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

When a transmission line is perfectly matched to the driver and load, the signals propagating electromagnetic (EM) energy are totally absorbed by the load. This is the perfect scenario that all electronics designers strive for. However, this is rarely the case and reflections do occur whenever the impedance of the transmission line changes along its length. This can be caused by unmatched drivers/loads, layer transitions, different dielectric materials, stubs, vias, connectors, and IC packages. By understanding the causes of these reflections and eliminating the source of the mismatch, a design can be engineered to perform reliably.

There are many ways to dampen reflections in high-speed PCB design, as listed below:

Drive Strength

Reflections can be caused by using a drive strength that is too high for the load. Driver

strengths typically range from 4 mA to 16 mA. A 16 mA driver is generally required for multiple loads—for instance, a DDR4 signal driving multiple SODIMM memory cards. In this case, the transmission lines are longer and the capacitive load higher, so simulation is necessary to confirm the required driver's current strength. To dampen the signal, terminations are typically placed on the memory card itself. However, if the signal is delivered to only one or two on-board memory devices, then the signal strength can usually be reduced to a minimum of 8 mA to prevent reflections.

The simulation in Figure 1 shows a clean signal with a wide eye opening, but there is a slight over-and undershoot of the signal (top and bottom) and a small amount of timing jitter (horizontal misalignment). The over/undershoot can be attributed to either over-driving the transmission line using a higher

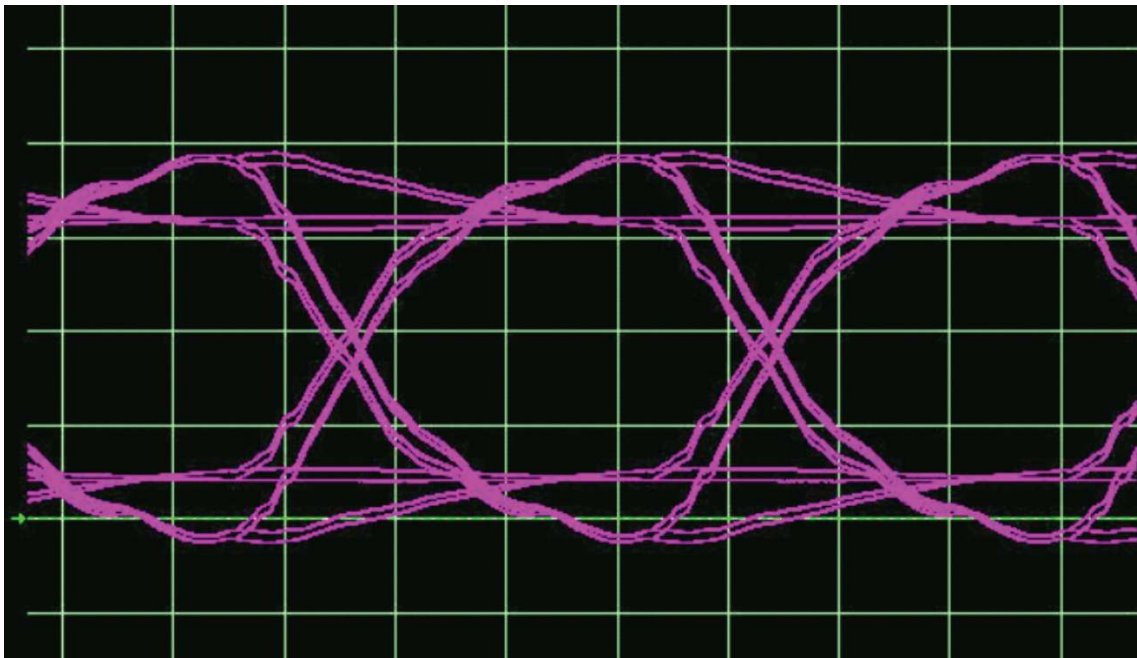


Figure 1: Reflections cause over/undershoot when the transmission line is over-driven.

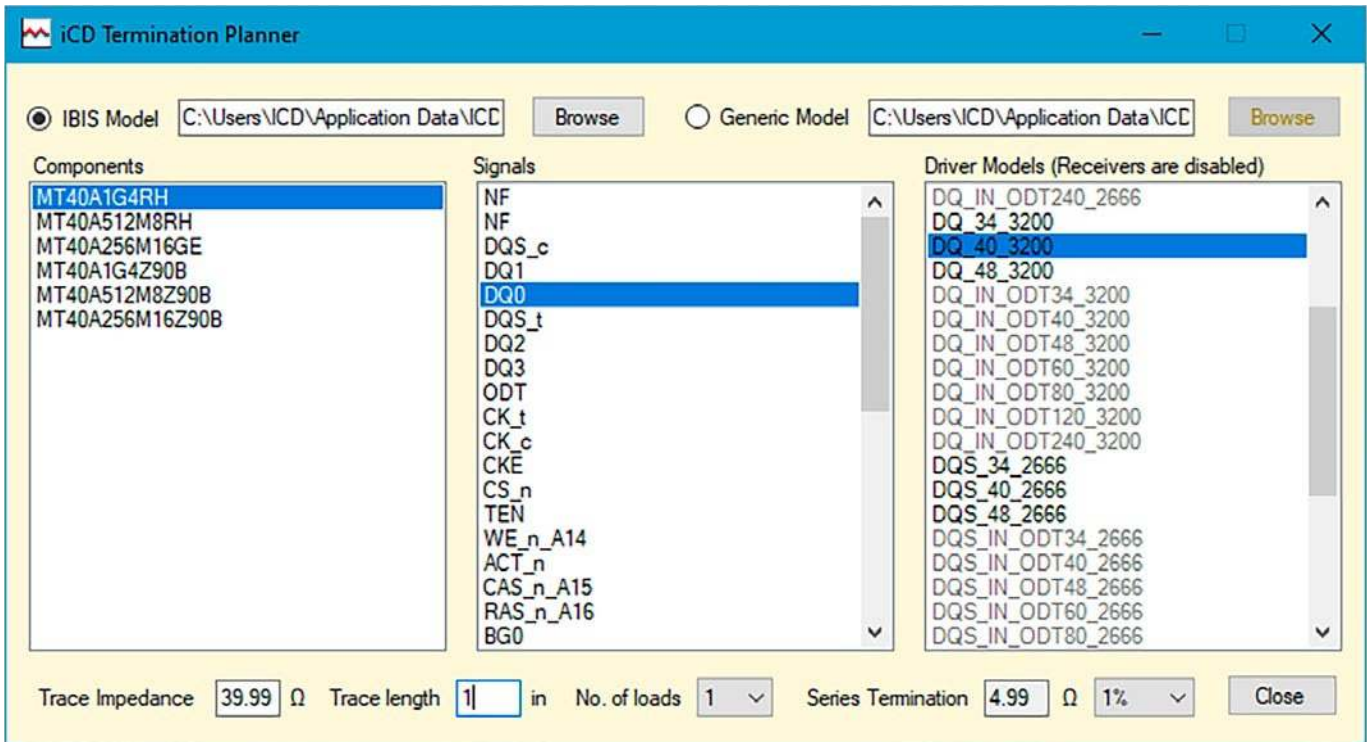


Figure 2: Micron 4 Gb DDR4-3200 SDRAM with ODT. (Source: iCD termination Planner)

drive strength than required or over-termination on the receiver side by using an external resistor value that is higher than the characteristic impedance of the transmission line. The degradation of the signal due to overdriving the transmission line might be sufficient to result in system failure.

On-Die Termination

On-die terminations (ODT) can be used with some memory devices to match the transmission line and dampen the reflections. Incorporating a resistive termination within the DRAM device improves the signaling environment by reducing the electrical discontinuities introduced with off-die termination. DDR4 and DDR5 technology, like DDR3, include ODT on the data I/O pins. This feature is controlled by the ODT pin and consumes additional power when activated. The ODT and the output driver on DDR4 devices include additional mode register settings over the previous DRAM to increase system flexibility and optimize signal integrity. The ODT impedance can vary from

34–240 Ω in receive mode and 34–48 Ω in transmit mode in Figure 2. DDR4 signal-ended signals are normally routed on 40 Ω transmission lines so, for short trace lengths with one load, a 40 Ω ODT is perfect. However, since the ODT and driver strength are software selectable, one can validate and tune the strength during the testing phase of development.

Series Termination

Unfortunately, drivers do not have the same impedance as the transmission line (typically 10–35 Ω) so series terminations are used to balance the impedance, match the line, and minimize reflections, particularly on long traces where ODT is not provided. Impedance matching slows down the rise and fall times, reduces the ringing (over/undershoot) of signal drivers, and enhances the quality of a high-speed signal. The ringing is dramatically reduced by adding a series terminator as in Figure 3. From this, we can see that the impedance has to be matched—but to what value?

In Figure 4, using a 12 mA LVCMOS 1.8V

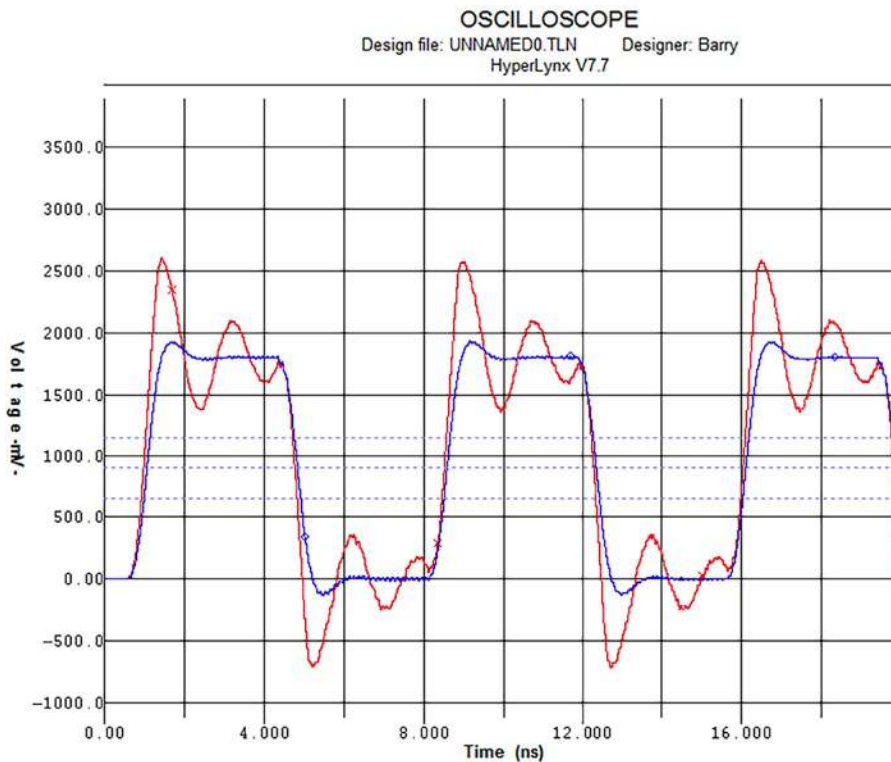


Figure 3: Unmatched (red) vs. matched (blue) transmission lines.

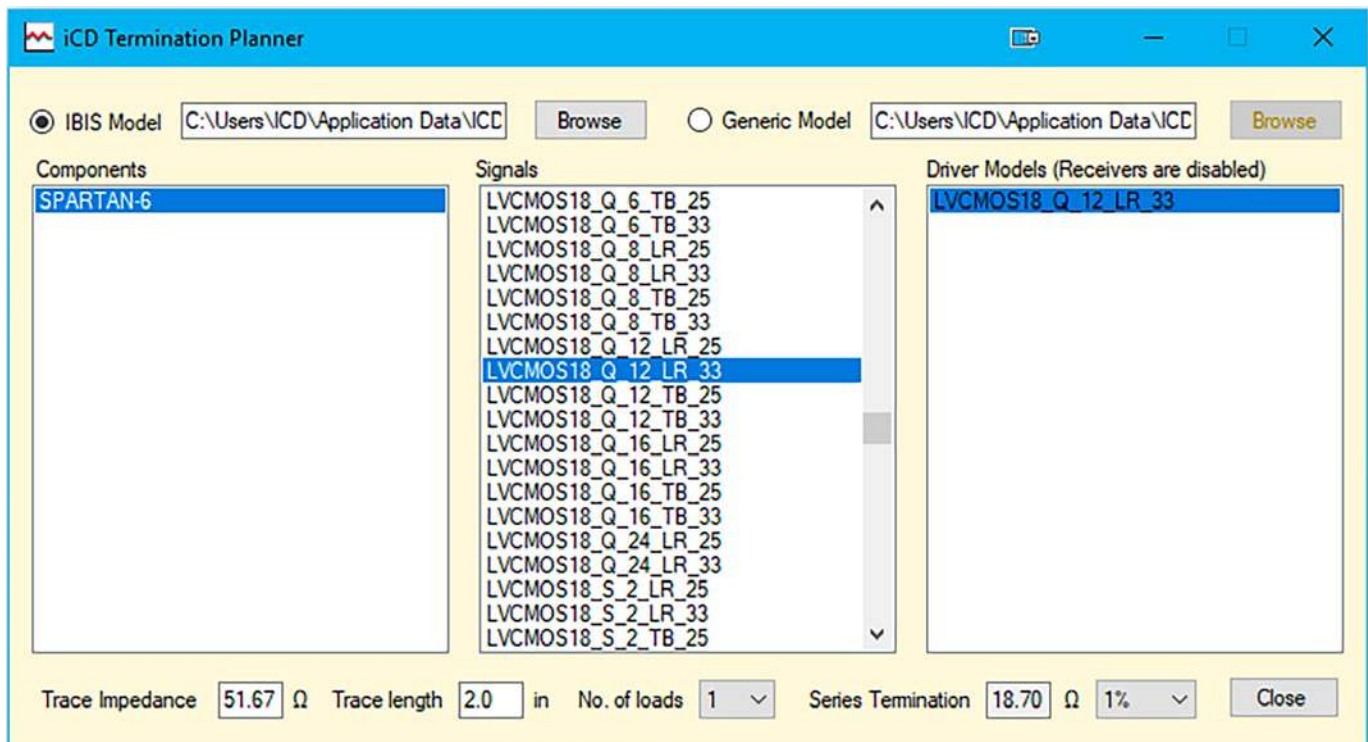


Figure 4: Matching the Spartan 6 driver to the transmission line. (Source: iCD Termination Planner)

driver of a Spartan 6 FPGA, an 18.7 Ω series resistor is required to match the driver to the 51.67 Ω trace on the outer layer. This is auto-

atically derived from the IV curves of the Spartan 6 IBIS model by the iCD Termination Planner (Figure 4).

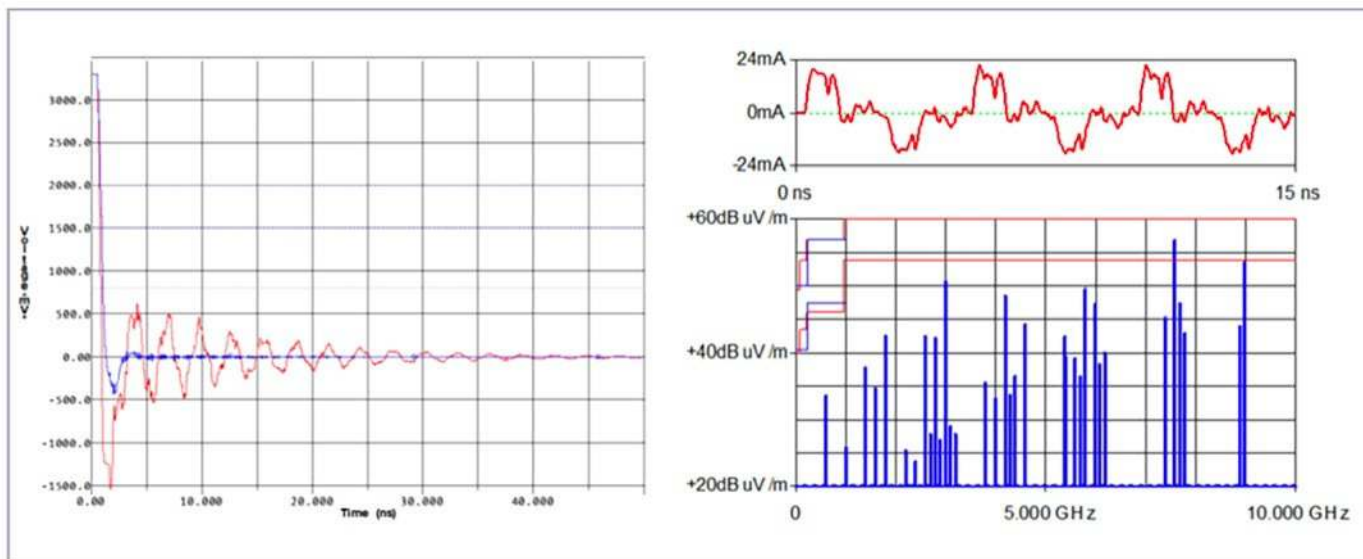


Figure 5: Ringing and radiation are reduced dramatically by adding a series terminator.

Figure 5 (left) illustrates the ringing (red) in an unmatched transmission line. This ringing, which also causes electromagnetic radiation (right), is dramatically reduced by terminating the transmission line with an 18.7 Ω series resistor.

Crosstalk

Another culprit is crosstalk, particularly on long parallel trace segments. Crosstalk arises as a result of the unintentional coupling of electromagnetic fields and causes both forward and reverse reflections. The easiest way to reduce crosstalk from a nearby aggressor signal, of course, is by increasing the spacing between the signals in question. Crosstalk falls off very rapidly with distance. Crosstalk plummets roughly quadratically with increased separation. Doubling the spacing cuts the crosstalk to roughly a quarter of its original level. A good rule of thumb for this is $\text{Gap} = 3 \times \text{trace width}$. However, in today's complex designs it is not always possible to use up valuable real estate to satisfy the above. Reducing the signal trace to reference plane dielectric thickness can also reduce crosstalk while not requiring additional space. Also, different technologies should not be mixed as higher voltages create higher crosstalk.

And long parallel trace segments should be avoided.

Crosstalk also depends on the load which may vary considerably when driving banks of memory modules, for example. Keep in mind that the total crosstalk on each victim trace is the total crosstalk from each of several nearby aggressors, all of which sum to produce the maximum value.

Plane Cavity Resonance

Plane pairs, in multilayer PCBs, are essentially unterminated transmission lines—just not the usual traces or cables we may be accustomed to. They also provide a very low impedance path, which means that they can present logic devices with a stable reference voltage at high frequencies. But, as with signal traces, if the transmission line is mismatched or unterminated, there will be standing waves—ringing. The bigger the mismatch, the bigger the standing waves and the more the impedance will be location-dependent.

When the cavity has open end boundary conditions, resonances arise when a multiple of half wavelengths can fit between the ends of the cavity. Figure 6 shows the cavity resonance of a plane pair with a resonant frequency of 1 GHz. If the signal clock frequency (or har-

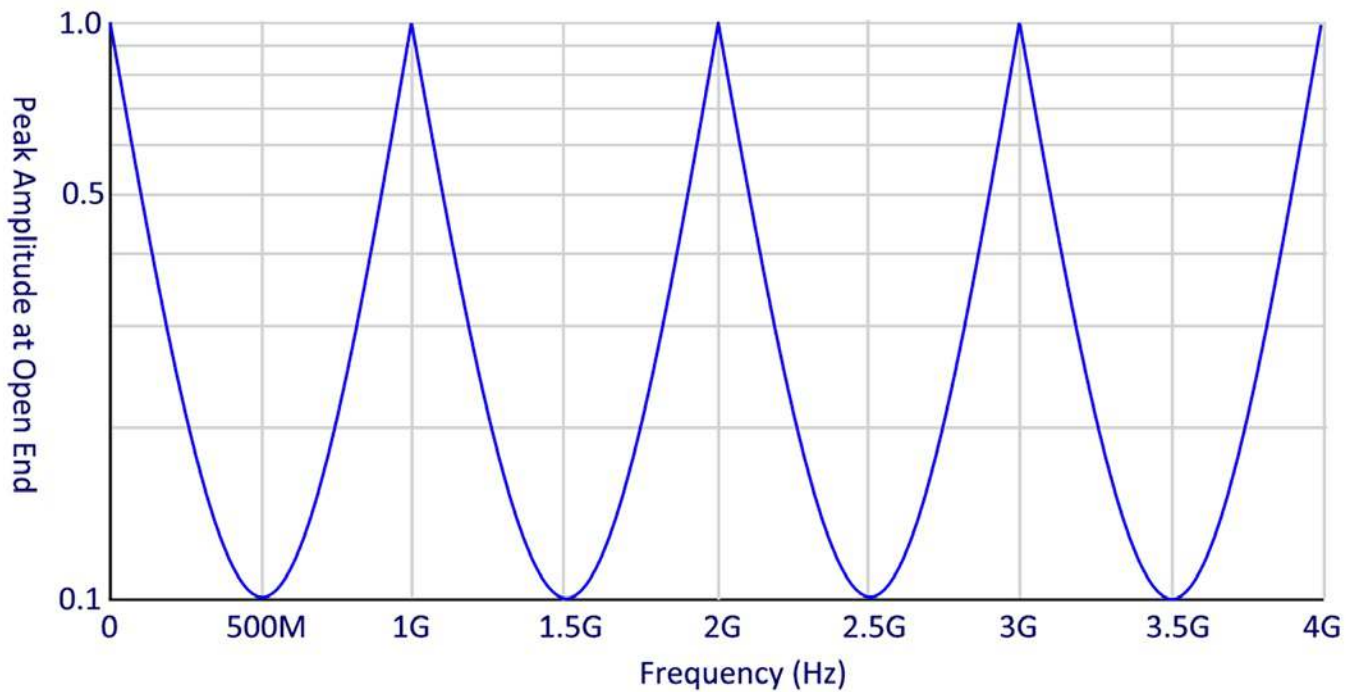


Figure 6: Amplitude, at the far end of planes, as the input frequency is swept. (Source: Eric Bogatin)

monics) is multiples of 1 GHz, then noise can be injected into the plane cavity. When the clock or data harmonics overlap with the cavity resonant frequencies, there is the potential for long-range coupling between any signals that run through the cavity, thus affecting signal integrity as a consequence of inadequate power integrity.

Plane cavity resonance and emissions can be reduced as follows:

1. A thin dielectric, in the plane cavity, is the most effective way of reducing the peak amplitude of the modal resonance. It reduces spreading inductance and the impedance of the cavity, and also reduces the resonance peaks by damping the high-frequency components.
2. RC terminations, of 3R5 in series with 10nF connected across the plane pair and placed along the board edges, are generally sufficient to reduce the resonance peaks.
3. The parallel resonant frequencies, of the cavity, can be pushed up above the

maximum bandwidth of the signals by reducing the plane size and by adding stitching vias between (similar) planes of a cavity.

When a signal's EM energy propagates from the driver to the receiver along a transmission line, it changes along its length. The original signal will be received with varying degrees of distortion and degradation. This signal distortion happens due to factors such as impedance mismatch, reflections, ringing, crosstalk, dielectric loss, jitter, and ground bounce. The PCB designer's primary objective should be to minimize these issues at the source, so that any signal distortion is eliminated.

Key Points

- Reflections can be caused by using a drive strength that is too high for the available load.
- Over/undershoot can be attributed to overdriving the transmission line using a higher than required drive strength setting on the driver.

- On-die terminations (ODT) can be used with some memory devices to match the transmission line and dampen the reflections.
- Drivers do not have the same impedance as the transmission line (typically 10–35 Ω) so series terminations are used to balance the impedance, match the line, and minimize reflections.
- The easiest way to reduce crosstalk from a nearby aggressor signal is by increasing the spacing between the signals.
- Reducing the signal trace to reference plane dielectric thickness can also reduce crosstalk while not requiring additional space.
- Plane pairs in multilayer PCBs are essentially unterminated transmission lines.
- If the plane cavity is mismatched or unterminated, there will be standing waves—ringing. **DESIGN007**

Resources

1. [Beyond Design](#) columns by Barry Olney: “The Fundamental Rules of High-Speed PCB Design, Part 2;” “Stackup Configurations to Mitigate Crosstalk;” “Controlled Impedance Design;” “Plane Cavity Resonance;” “Dampening Plane Resonance with Termination;” “Signal Integrity, Part 3.”

Errata: In the February 2021 issue of Design007 Magazine, the Beyond Design column, “Stackup Configurations to Mitigate Crosstalk,” contained two errors in equations 1 & 2. The term $Lm/Ctotal$ should have been $Lm/Ltotal$. Please download the revised PDF to replace your library copy today.



Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD

Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded at www.icd.com.au. To read past columns or contact Olney, [click here](#).

U-Boat Worx Launches 9-person Flagship Lithium-ion Battery Submersible NEXUS



Dutch submersible manufacturer U-Boat Worx breaks the mould with the launch of the NEXUS series. U-Boat Worx is the market leader in private and commercial submersibles.

The NEXUS series comprises two models featuring an ultra-large elliptical acrylic pressure hull with unrivalled passenger comfort. Seating up to eight passengers and one pilot, the NEXUS provides 25% more interior space than competing models. The NEXUS subs are depth-rated to 200 meters (650 feet).

Equipped with the latest lithium-ion battery technology, the subs can operate for up to 18 hours and dive up to ten times a day. 80 guests can participate in an unforgettable sub-sea adventure daily.

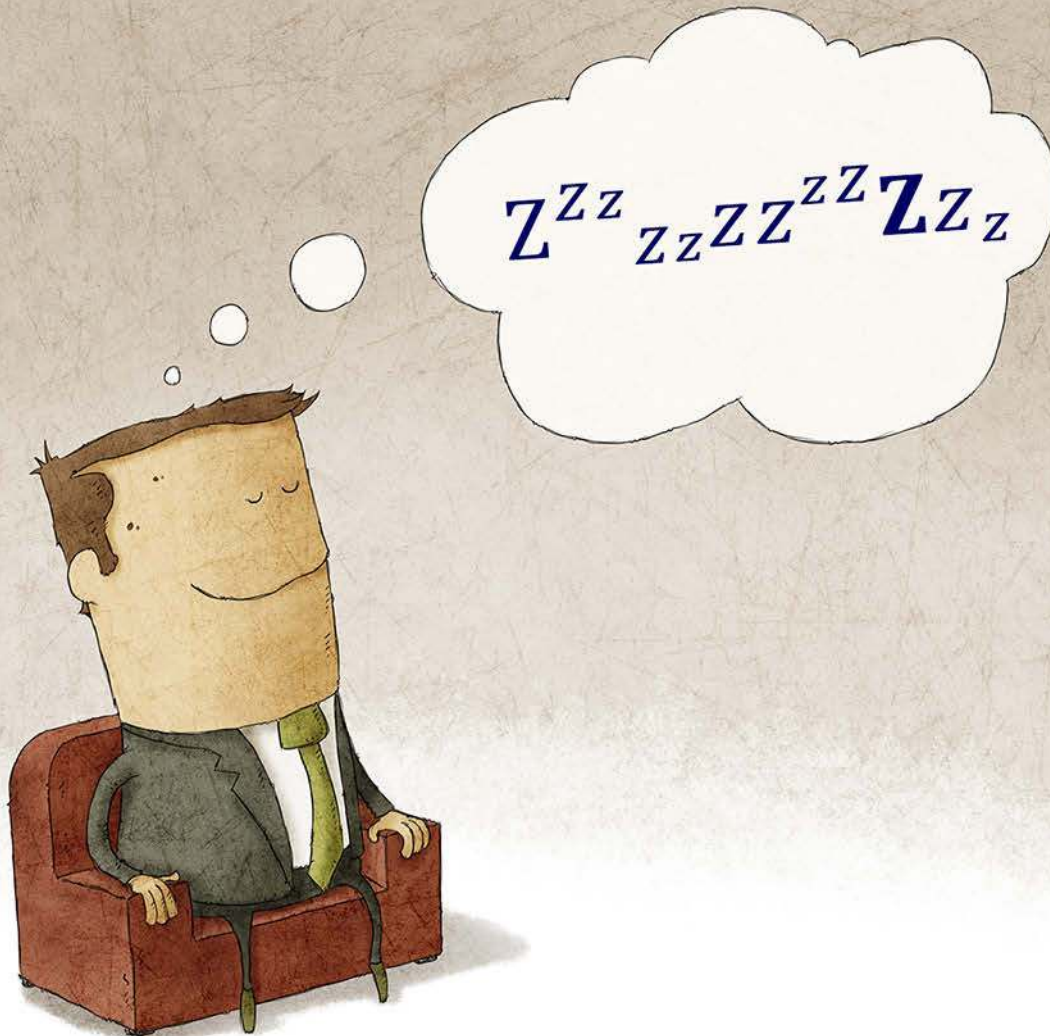
The unique revolving seating arrangement featured in the Cruise Subs has been replicated in the NEXUS. Passengers therefore always enjoy the best view, regardless of the direction the submarine is travelling. The NEXUS subs are designed as multi-directional, meaning they can manoeuvre in any direction without compromise. This is a distinguishing capability only achieved in U-Boat Worx submersibles. Ten silent thrusters provide the power required for top performance and unmatched speed.

The experience and knowledge gained from the development of the Cruise Subs has evolved the new features in the NEXUS series, including an XXL entrance hatch, the largest ever incorporated on a submersible of this size.

The NEXUS is optimised for ship-based launch and recovery and can also be deployed from land and transported to dive sites.

(Source: ACN Newswire)

We **DREAM** Impedance!



Did you know that two seemingly unrelated concepts are the foundation of a product's performance and reliability?

- Transmission line impedance and
- Power Distribution Network impedance

DISCOVER MORE

iCD software quickly and accurately analyzes impedance so you can sleep at night.

iCD Design Integrity: Intuitive software for high-speed PCB design.

iCD
In-Circuit Design Pty Ltd

"iCD Design Integrity software features a myriad of functionality specifically developed for PCB designers."

– Barry Olney



www.icd.com.au