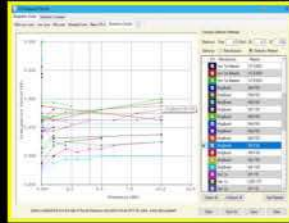


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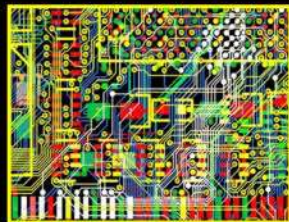


### A Comprehensive Report Includes:

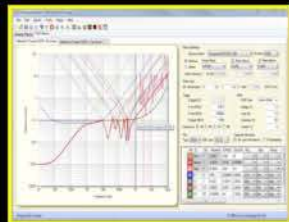
Material Selection for Cost/Performance to Required Frequency and Bandwidth, Design Constraint Review



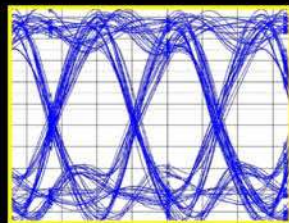
Stackup Impedance Analysis, Single-ended, Differential Pairs and CPW Blind and Buried Via Definition, Reference Plane Assignment Validation



Critical Placement and Routing, Plane Pour Definitions, Return Current Paths, Plane Cross-overs and Broadside Coupling Review



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# PCB Design Strategies to Reduce Costs

## Beyond Design

Feature Column by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

There are numerous ways to improve the PCB design and production processes and thereby reduce costs, from fundamental improvements involving a standard form factor and reducing the board size and complexity, to technology choices and simulation to reduce iterations. A good starting point would be the IPC standards developed by the electronics industry to enhance manufacturability, testability, and assembly. Anyone new to PCB development should initially begin with these standards and then fine-tune them to capture the essence of their design style.

The adoption of surface mount technology (SMT) and the increased use of high-density

interconnects (HDIs) has enabled more functionality per unit area than conventional plated through-hole (PTH) PCBs. The semi-additive process (SAP) takes this one step further by reducing the size of wearable devices. These technologies are also ideal for high-speed design as they reduce transmission line length, hence, reflections and lower inductance of the power/ground system. With no component leads the assembly can be automated, dramatically reducing production time and cost.

Via technology is another consideration. Plated through-hole vias are the most affordable and should be used whenever possible. Blind and buried vias will increase your costs.

They're only necessary on high-density and high-frequency complex boards, so you should typically not need them. Microvias are relatively costly for simpler designs, but for more sophisticated PCBs and prototypes, they are the prime solution. They also reduce layer count which is a cost-saving. Blind and buried vias are also used to reduce the board aspect ratio. The minimum via hole is determined by drill size as well as the aspect ratio, which is the thickness of the PCB divided by the diameter size of the drilled hole. There is usually an additional manufacturing cost for aspect ratios higher than 8:1 for PTH and 0.8:1 for microvias.

The efficiency and design freedom provided by blind and buried microvias are some of the reasons why PTHs are rapidly becoming a thing of the past for complex designs, especially since most of the components that require PTHs to be mounted on a PCB are bulky and space-consuming, whereas dense BGA designs are more suited to the use of microvias.

Cost is also relative to the trace/clearance requirements of the technology employed. The larger the trace/clearance, the less the cost. Going below 4/4 mil technology will incur a cost premium. The use of mixed signal/power planes can reduce the need for additional plane layers to keep the layer count down. Look for different design options to make sure your board is as simple as possible. Not only do you want to optimize the elements of the board, but you'll also want it on a small form factor that still provides appropriate clearance for every element.

Material selection is another cost consideration. When each material is used for the right target application, the resultant PCB will have the lowest possible cost while still satisfying the design and performance goals of the project.

In Figure 1, I have selected a 10 GHz Isola TerraGreen material with a Dk of 3.3 and a dissipation factor (Df) of 0.003 for its low loss capabilities. Now, this may be necessary for our high-speed DDR4 signals but is not a

Layer No.	Via	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)
		Soldermask		PSR-4000 HFX Satin / CA-40 HF LPI ...	3.5	0.5							
1	8	Signal	Top	Conductive			2.2	12	4	0.43	52.6	100.76	
		Prepreg		TerraGreen; 1035; Rc=70% (10GHz)	3.22	2.6							
2		Plane	GND	Conductive			1.4						
		Core		KB-6150; 1-1080; (1MHz)	4.6	3							
3		Plane	PWR	Conductive			1.4						
		Prepreg		TerraGreen; 1086; Rc=68% (10GHz)	3.26	4.3							
4		Signal	Signal	Conductive			1.4	10	4	0.31	41.43	82.06	
		Core		TerraGreen; 2-1067; Rc=63% (10GHz)	3.37	4							
5		Plane	PWR	Conductive			1.4						
		Prepreg		KB-6050; 1078LD; Rc=61% (1MHz)	3.92	2.6							
6		Plane	GND	Conductive			1.4						
		Core		TerraGreen; 2-1067; Rc=63% (10GHz)	3.37	4							
7		Signal	Signal	Conductive			1.4	10	4	0.31	41.43	82.06	
		Prepreg		TerraGreen; 1086; Rc=68% (10GHz)	3.26	4.3							
8		Plane	PWR	Conductive			1.4						
		Core		KB-6150; 1-1080; (1MHz)	4.6	3							
9		Plane	GND	Conductive			1.4						
		Prepreg		TerraGreen; 1035; Rc=70% (10GHz)	3.22	2.6							
10		Signal	Bottom	Conductive			2.2	12	4	0.43	52.6	100.76	
		Soldermask		PSR-4000 HFX Satin / CA-40 HF LPI ...	3.5	0.5							

Figure 1: Ten-layer high-speed PCB stackup. (Source: iCD Stackup Planner)

good pick for planar capacitance. For fast rise time signals, we need a low dissipation factor with low loss. However, for planar capacitance (between power/ground planes), we need a very thin dielectric with a high dielectric constant. The capacitance (C) of a parallel plate capacitor (plane) is relative to plane area (A), the dielectric thickness (d), and the dielectric constant (Dk).

$$C = Dk \cdot A/d$$

For a high distributed capacitance, we need a high Dk, so I have chosen a low-cost King-board material (highlighted) with a high Dk of 4.6. Not only will this help reduce the cost but will also help reduce the AC impedance of the power distribution network. You do not have to use the same expensive material throughout the stackup; in this case, the low-cost King-board material performs better for its application.

Utilizing efficient EDA tools can also streamline the PCB development cycle. Many improvements in EDA software have helped to structure the design flow effectively and have reduced expenses. The availability of an elaborate component library reduces the rebuilding time and effort. Team sharing software can also drive comprehensive design reviews to improve the quality of the product.

Following the best design constraints won't necessarily produce a premium product. Across multiple sectors, fields, and disciplines, simulation is having a profoundly positive effect. One of the primary advantages of using simulation software is the fact that it enables one to obtain valuable feedback when designing real-world circuits. Furthermore, this feedback does not come with the time or expenditure typically required to procure this much-needed design insight. This, in turn, allows the designer to determine the efficiency and integrity of their designs without the need to build the product first. Lifecycle Insights (September 2018) found that the average number of respins per project was 2.9, and the average

cost of a respin was \$28,482. That's an incredible \$82,598 for each new product.

Simulation also allows the designer to explore the worthiness of alternate designs without ever building the actual product. Moreover, examining the effects of your design decisions during the design phase rather than the construction phase saves iterations, time, and money, as well as increases design quality.

The cost of development is dramatically reduced if simulation is employed early in the design cycle. If changes are made late in the design process, then it takes more time, people, material, and therefore money, to complete the project. The advantage of simulation is that it identifies issues early in the design process and rectifies them before they become a major problem.

Design changes that occur:

- In the conceptual stage it costs nothing
- During the design stage it requires just a little extra time
- During the test stage means that you must regress one stage
- During production, or worse still, in the field, can cost millions to fix and possibly damage the company's reputation

Having the project completed on time and within budget, means that costs are cut by reducing the design cycle and generating higher profits due to shorter time-to-market and an extended product life cycle. Having validated the design by simulation, you can be assured of reliable performance.

## Key Points

- Anyone new to PCB development should initially begin with the IPC standards and then fine-tune them to capture the essence of their design style.
- The adoption of SMT and the increased use of HDIs have enabled more functionality per unit area than conventional PTH PCBs.

- Plated through-hole vias are the most affordable and should be used whenever possible. Blind and buried vias will increase your costs.
- Dense BGA designs are more suited to the use of microvias.
- The larger the trace/clearance, the less the cost. Going below 4/4 mil technology will incur a cost premium.
- When each material is used for the right target application, the resultant PCB will have the lowest possible cost while still satisfying the design and performance goals of the project.
- Utilizing efficient EDA tools can also streamline the PCB development cycle.
- Simulation enables one to obtain valuable feedback when designing real-world circuits.
- The cost of development is dramatically reduced if simulation is employed early in the design cycle.

- The advantage of simulation is that it identifies issues early in the design process and rectifies them before they become a major problem. **DESIGN007**

#### Reference

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**Barry Olney** is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the

iCD Stackup, PDN, and CPW Planner. The software can be downloaded at [www.icd.com.au](http://www.icd.com.au). To read past columns or contact Olney, [click here](#).

## ClearBuds: First Wireless Earbuds That Clear Up Calls Using Deep Learning

As meetings shifted online during the COVID-19 lockdown, many people found that chattering roommates, garbage trucks and other loud sounds disrupted important conversations.

This experience inspired three University of Washington researchers, who were roommates during the pandemic, to develop better earbuds. To enhance the speaker's voice and reduce background noise, "ClearBuds" use a novel microphone system and one of the first machine-learning systems to operate in real time and run on a smartphone.

"ClearBuds differentiate themselves from other wireless earbuds in two key ways," said co-lead author Maruchi Kim, a doctoral student in the Paul G. Allen School of Computer Science & Engineering. "First, ClearBuds use a dual microphone array. Microphones in each earbud create two synchronized audio streams that provide information and allow us to spatially separate

sounds coming from different directions with higher resolution. Second, the lightweight neural network further enhances the speaker's voice."

With ClearBuds, each earbud sends a stream of audio to the phone. The researchers designed Bluetooth networking protocols to allow these streams to be synchronized within 70 microseconds of each other.

The team also tested ClearBuds "in the wild," by recording eight people reading from Project Gutenberg in noisy environments, such as a coffee shop or on a busy street. The researchers then had 37 people rate 10- to 60-second clips of these recordings. Participants rated clips that were processed through ClearBuds' neural network as having the best noise suppression and the best overall listening experience.

(Source: Sarah McQuate, UW News)

