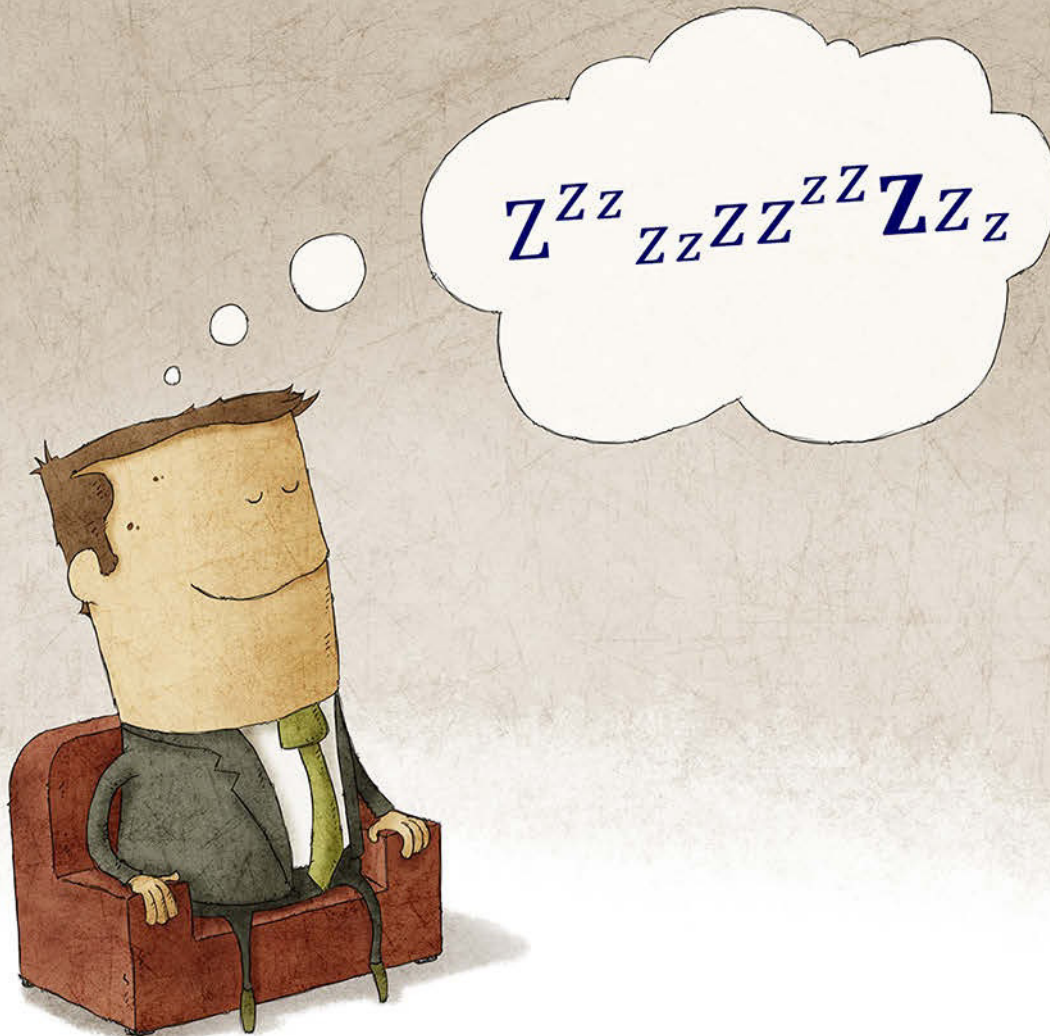


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The Impact of Signal Rise Time on Bandwidth

Beyond Design

by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

The term bandwidth was first used years ago in the RF world to represent the range of frequencies in a signal. In digital electronics, we also use the term to describe the signal spectrum since square waves are made up of numerous sine waves (harmonics) of the fundamental frequency (Figure 1). For digital signals, the lowest frequency is always the DC component (zeroth frequency) and the highest frequency component is the maximum frequency that is significant (typically the fifth harmonic). The shorter the rise time in the time domain, the higher the bandwidth in the frequen-

cy domain, and the more closely the waveform resembles an ideal square wave. In this month's column, I will look at the relationship between signal rise time and the bandwidth of a digital signal.

Rise time describes how quickly a digital signal can change from a low state to a high state. A signal must have a fast enough rise time to accommodate the data being processed. Otherwise, information in the waveform (circuit timing) may be lost. However, a signal does not have to have a faster rise time than is required by the system. Faster is not necessarily better as it may create ground bounce, reflections, crosstalk, and electromagnetic radiation.

In an ideal world, one should limit the bandwidth so that the system performs to expectations, but at the same time, avoid high-frequency effects, which cause electromagnetic compatibility issues.

This is exactly what a series impedance termination does. The resistor, close to the source, combines with the input capacitance of the receiver IC(s) to create a low pass filter (Figure 2). This filter rolls off the high-frequency components of

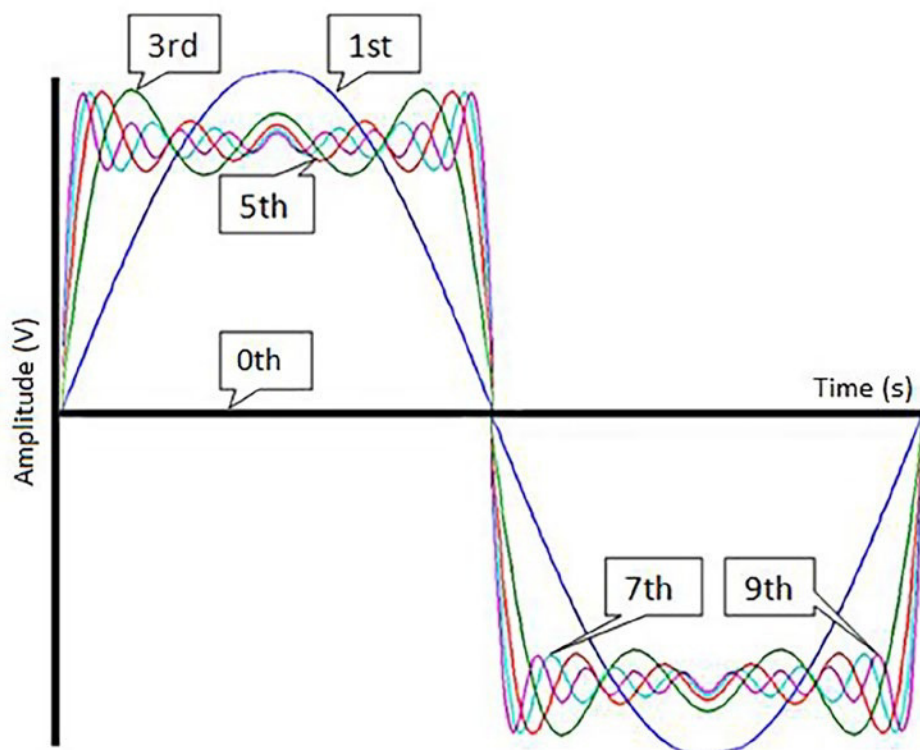


Figure 1: Harmonic content of a square wave. Higher harmonics have faster rise times.

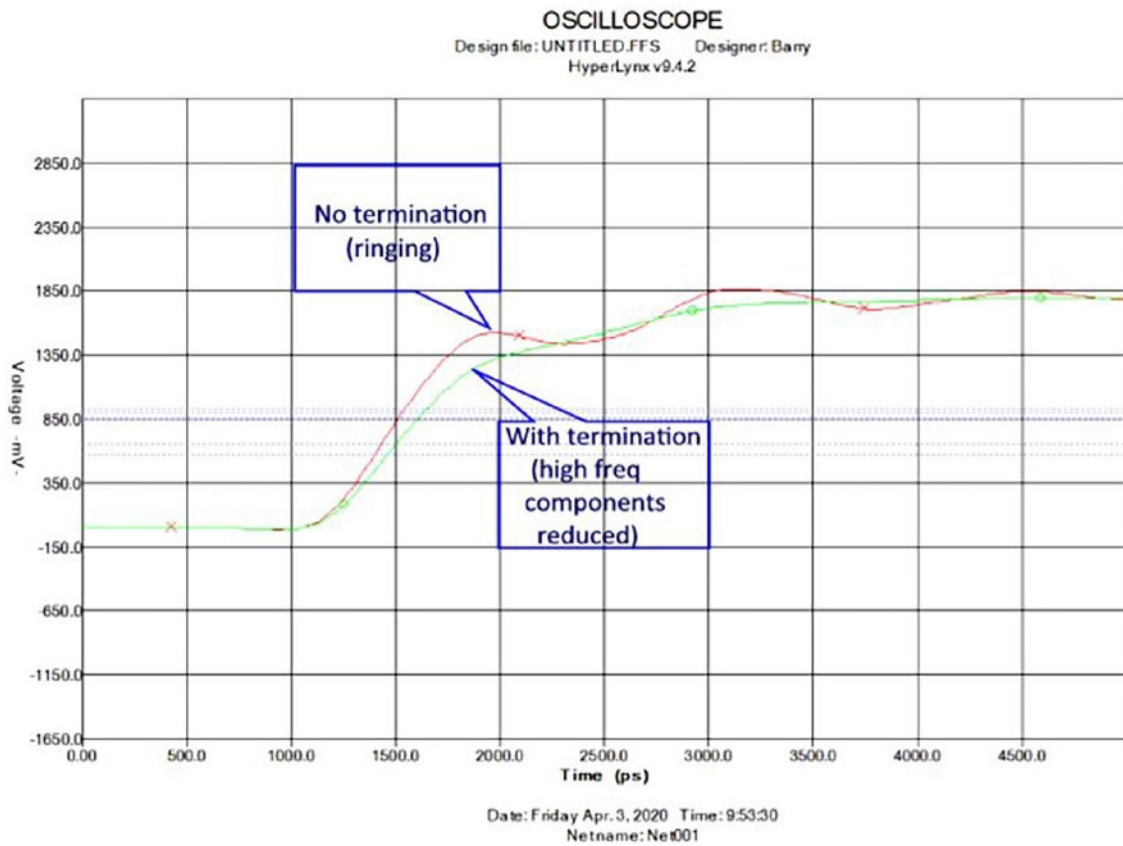
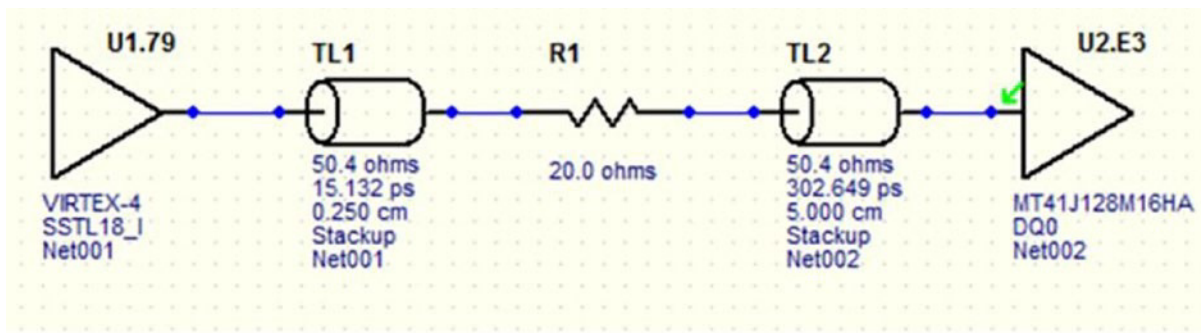


Figure 2: Series terminator rolls off the high-frequency components to reduce ringing (simulated in HyperLynx).

the waveform, reducing reflections. Providing we choose the right value to match the impedance of the transmission line, the circuit functions perfectly, although the higher frequencies are dampened.

Depending on the logic family, the fall time is usually slightly shorter than the rise time. This is due to the design of typical CMOS output drivers. For the same feature size transistor, an n transistor can turn on faster than a p transistor. This means switching from high to low, the falling edge will be shorter than the rising edge. In general, signal integrity prob-

lems are more likely to occur when switching from a high-to-low transition than from a low-to-high transition. This is something to look out for when using double data rate (DDR) memory, where the device is clocked on both the rising and falling edges of the waveform.

In the time domain, the most important merit for a signal is the rise time. The rise time is typically measured from the 10% point to the 90% point on the rising edge of the signal, although the industry is moving toward 20–80% to eliminate the distortion at the extremities. The shape of the rising edge strongly influenc-

es the interpretation of the rise time. The rise time of a signal is inversely proportional to its bandwidth.

$$BW (3dB) = \frac{0.35}{Rt} \quad \text{Equation 1}$$

BW is the bandwidth in GHz, and
Rt is the rise time in ns.

The bandwidth of the signal in the frequency domain is where we arbitrarily define the bandwidth as the -3 dB point. This is the frequency at which the signal amplitude, through the circuit, is reduced down to 70% of the amplitude of the input signal. Higher frequencies are attenuated even more.

In practice, the signal rise time has an impact on the maximum signal bandwidth. Understanding the frequency band, that really matters, for digital design is very important. Traditionally, we used Equation 1 for the upper bandwidth, assuming one can ignore all the frequency components above the bandwidth and not lose any valuable information about the time domain response.

$$BW (6dB) = \frac{0.5}{Rt} \quad \text{Equation 2}$$

However, as rise times become faster, a more accurate approach is to use the upper knee frequency (which is down -6.8 dB), as in Equation 2. This forms a useful translation between

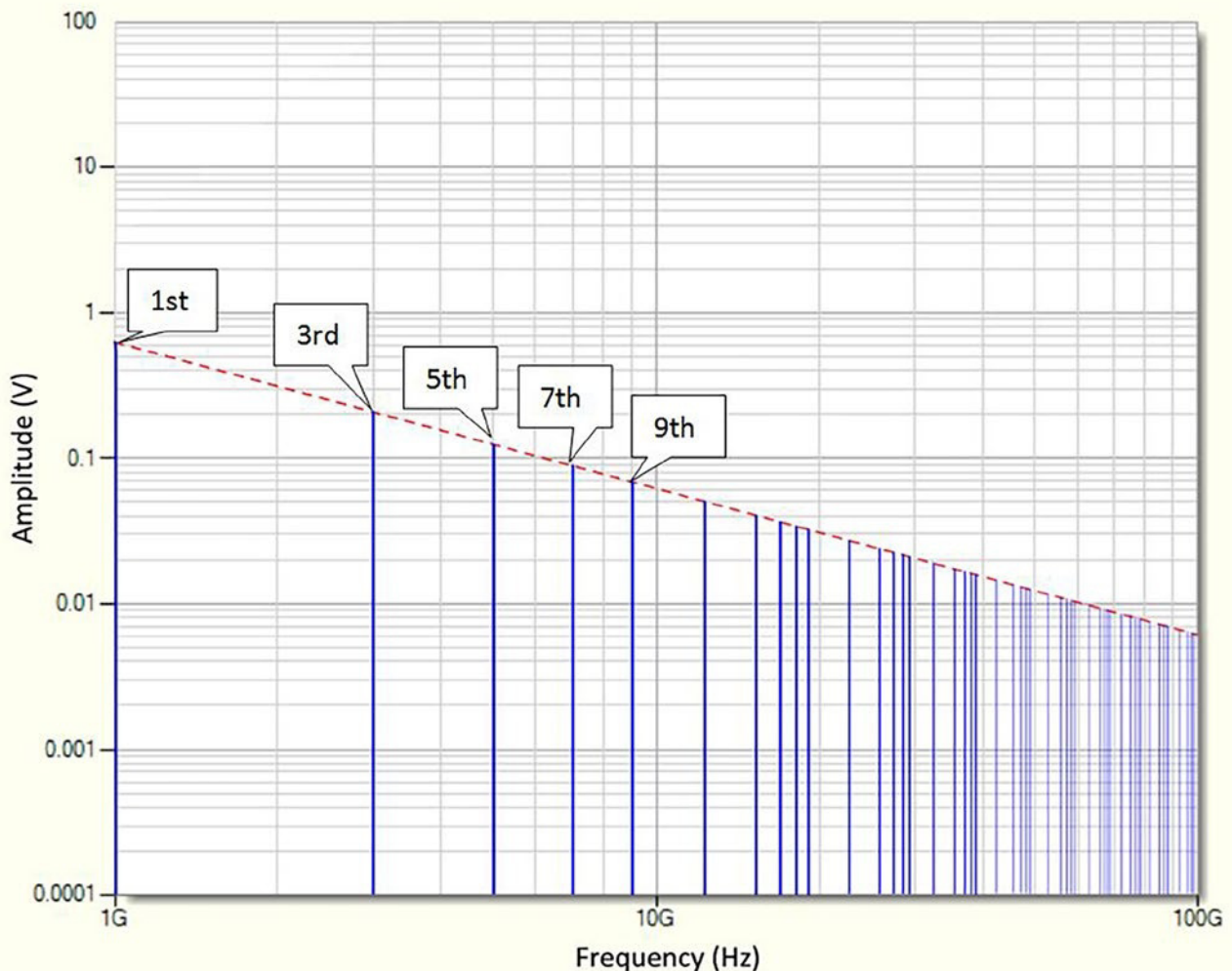


Figure 3: Odd harmonics of a 1 GHz fundamental clock in the frequency domain.

the time and the frequency domains. The knee frequency is an estimate of the highest frequency content of the signal, which depends upon the rise time of the signal. For instance, if the rise time is 100 ps, then the upper bandwidth is actually 5 GHz regardless of the clock frequency. It is possible to have two different waveforms, with exactly the same clock frequency but different rise times and, therefore, different bandwidths.

When selecting the most appropriate dielectric materials for a stackup design, one should consider the bandwidth up to the fifth harmonic. For the 1 GHz fundamental frequency in Figure 3, the maximum bandwidth to consider is the fifth harmonic at 5 GHz if the rise time is unknown. This assumes the worst case of a 100 ps rise time. For high-frequency signals, it is more accurate to use the actual rise time to evaluate bandwidth, but unfortunately, we do not always have the luxury of that information.

It is important to note that the concept of bandwidth is inherently an approximation. It is roughly where the amplitude of the frequency components in a waveform begins to drop off faster than an ideal square wave.

One simple but often overlooked method of minimizing noise in a system is to limit the system bandwidth to only that required by the intended signal. The use of higher bandwidth than required allows additional noise into the system. The same principle also applies in the case of digital circuits. High-speed logic with a fast rise time is much more likely to generate and be susceptible to high-frequency noise than its lower speed counterpart.

Key Points

- The shorter the rise time in the time domain, the higher the bandwidth in the frequency domain.
- A signal must have a fast enough rise time to accommodate the data being processed.
- A fast rise time may create ground bounce, reflections, crosstalk, and electromagnetic radiation.
- One should limit the bandwidth so that the system performs to expectations, but

at the same time, avoid high-frequency effects, which cause electromagnetic compatibility issues.

- Depending on the logic family, the fall time is usually slightly shorter than the rise time.
- Signal-integrity problems are more likely to occur when switching from a high-to-low transition than from a low-to-high transition.
- The rise time is typically measured from the 10% point to the 90% point on the rising edge of the signal.
- The 3 dB point is where the signal is reduced down to 70% of the amplitude of the input signal.
- As rise times become faster, a more accurate approach is to use an upper knee frequency.
- The knee frequency is an estimate of the highest frequency content of the signal, which depends upon the rise time of the signal.
- When selecting the most appropriate dielectric materials for a design, one should consider the bandwidth up to the fifth harmonic. **DESIGN007**

Further Reading

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- E. Bogatin, *Signal and Power Integrity: Simplified*, Prentice Hall, 2008.
- H. W. Johnson & M. Graham, *High-Speed Digital Design: A Handbook of Black Magic*, Prentice Hall, 1993.



Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded at icd.com.au. To read past columns or contact Olney, [click here](#).