Beyond Design: Return Path Discontinuities

by Barry Olney | In-Circuit Design Pty Ltd | Australia

Simultaneous switching noise (SSN) is a major problem in high-speed systems. But, the underlying issue is really the management of transmission line return currents that flow on the nearby reference planes, causing the planes to bounce. High-speed design is not as simple as sending a signal from the driver to the receiver, over an interconnect. But rather, one should also consider the presence and interaction of the power distribution network (PDN) and how and where the return current flows. A logic schematic diagram, masks details crucial to the operation of unintentional signal pathways vital to your understanding of signal performance, crosstalk and electromagnetic emissions.

PCB designers, generally, take great care to ensure that critical signals are routed exactly to length from the driver to the receiving device pins, but take little care of the return current path of the signal. Current flow is a 'round trip' and the important issue is delay not length. If it takes one signal longer for the return current to get back to the driver–around a gap in the plane for instance–then there will be skew between the critical timing signals. Return path discontinuities (RPDs) can create large loop areas that increase series inductance, degrade signal integrity and increase crosstalk and electromagnetic radiation.

There are four factors that need to be considered in order to mitigate the RPDs:

1. Recognize the impact of RPDs.
2. Understand the importance of referencing.
3. Identify the location of the RPDs–path of least inductance.
4. Take corrective action to mitigate the RPDs.

1. Recognize the impact of RPDs

Ground impedance is at the root of virtually all signal and power integrity problems–low ground impedance is mandatory for both. This is readily achieved with a continuous ground reference plane, but becomes increasingly difficult with the addition of more and more plane layers on a multilayer PCB. A ground plane serves well as a signal return, provided the ground is continuous under the signal path. But, even with a continuous return path, there may be enough voltage drop, across the plane, to generate a common mode voltage. And if left unchecked, may escape as electromagnetic emissions via the signal or power/ground conductors. RPDs have a huge impact on supply bounce of single ended signals. Fortunately, differential signaling dramatically reduces this affect. Serial interfaces also significantly reduce the number of interconnects, which is another advantage over the use of parallel buses for high-speed design.

Small discontinuities, such as vias and non-uniform return paths on a bus, are becoming an important factor for the signal integrity and timing of high-speed systems. RPDs produce impedance discontinuities due to the local return inductance and capacitive changes. Impedance discontinuities create reflected noise, contribute to differential channel to channel noise and may promote mode conversion. In the case of differential pairs, the transformation from differential-mode to common-mode typically takes place on bends and non-symmetrical routing, near via and pin obstructions, but can also be caused by small changes in impedance due to RPDs.

RPDs also impact on power integrity because of the impedance shift in the PDN. Different techniques need to be adopted, in order to minimize problems such as ground bounce noise and parallel plate waveguide resonances, in multilayer PCB planes.
Furthermore, RPDs tend to cause timing push-outs. A timing push-out (or expansion) is an increase in the flight time of a signal compared to an ideal interconnect. Often seen as a ledge in the rising/falling

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edge or a diminished rise time at the receiver, these push-outs consume valuable timing budgets allocated to the designer. Any type of non-ideal return path will introduce additional timing uncertainties, into the system, which degrade timing budgets and signal integrity. Therefore, the ability to identify the specific mechanisms, that contribute to the performance degradations, is essential to a good design methodology.

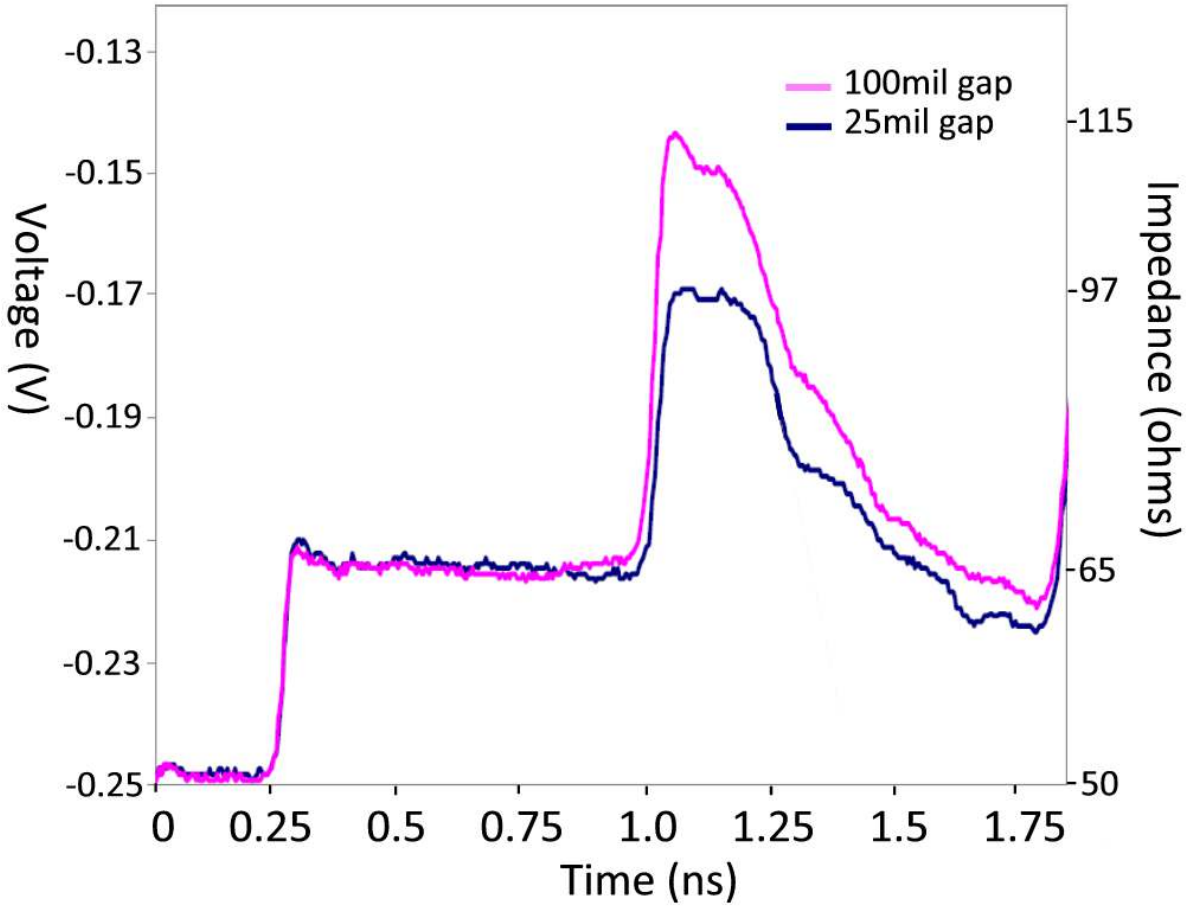

Figure 1 – Inductive spike for 25 & 100mil gaps (source– Byers)

In the case of a split in the reference plane, the most disruptive effect is a significant inductive spike as seen in Figure 1. This plot compares a 25 and 100mil gap in the return plane. This disruption is caused by the increase in current loop area which corresponds to an increase in inductance following the relationship:

$$L = \frac{\Phi}{I}$$

Where L is the inductance, Φ is the flux defined by the magnetic field, and the area between the trace and plane, and I is the loop current. As the gap forces the return current to diverge, the flux loop defined but the signal trace current and plane current increases, thus increasing the inductance. This spike can pose a serious problem since it will degrade the signal integrity at the receiver, filter the edge rate and increase inter-symbol interference. If this degradation is severe enough, it may cause a false trigger at the receiver or extend the timing enough to violate the setup and hold times.

But most importantly, RPDs typically manifest themselves as intermittent operation and degrade the performance of the product which can be extremely difficult to debug.

2. Understand the importance of referencing

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Each signal layer should be adjacent to, and closely coupled to, a reference plane, which creates a clear, uninterrupted return path and eliminates broadside crosstalk. As the layer count increases, this concept becomes easier to implement but decisions regarding return current paths become more challenging.

Although power planes can be used as reference planes, ground is more effective as local stitching vias can be used, for the return current transitions, rather than stitching decoupling capacitors which add inductance. This keeps the loop area small and reduces radiation. As the stackup layer count increases, so does the number of possible combinations of the structure. But, if one sticks to the basic rules then the best performing configurations are obvious.

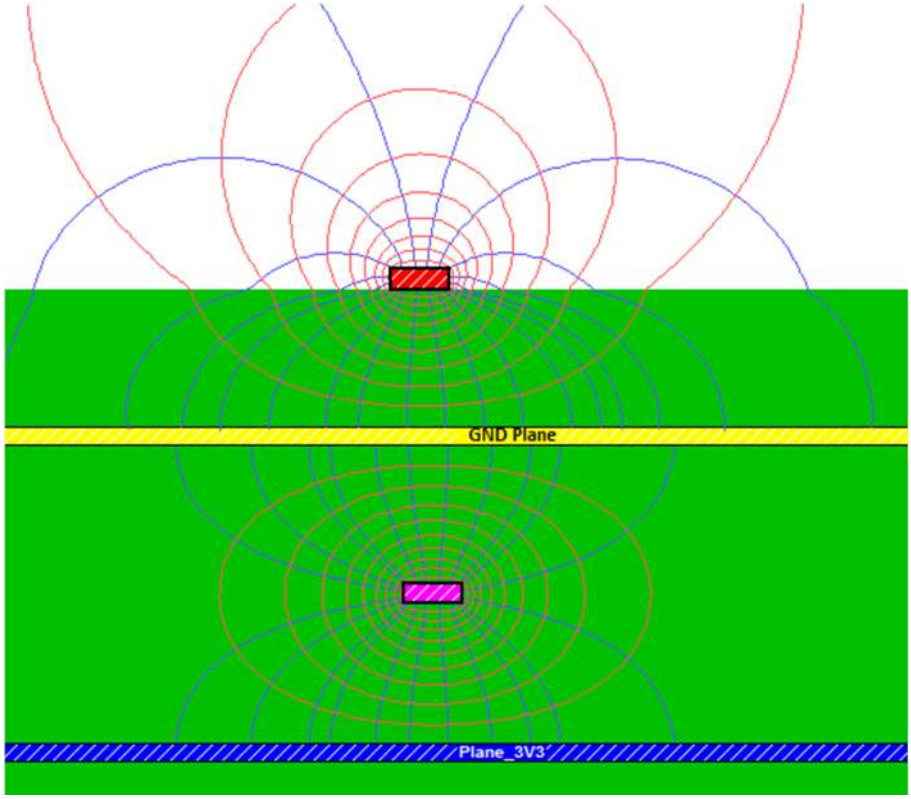

Figure 2 – Electric (blue) and Magnetic (red) Fields – (source HyperLynx)

Figure 2 shows the electric and magnetic fields emanating from a signal trace in both a microstrip and stripline configuration. Electric fields (blue) terminate when they come into contact with a solid plane, while magnetic fields (red) are shielded by the planes but the fringing fields still tend to radiate from the board edges.

3. Identify the location of the RPDs

The return current of a high-speed, fast rise time digital signal will always follow the path of least inductance which is directly beneath the signal path. However, RPDs tend to divert the return current increasing the loop area, inductance and delay–which is not desirable. The best way to identify the RPDs is to follow the signal path and imagine the return path closely coupled on the nearest plane.

A via that provides the connection between signal traces, referenced to different planes, creates RPDs. In other words, the return current has to jump between the planes to close the current loop, which in turn increases the inductance of the current loop, affecting the signal integrity. This return current also excites the parallel plate mode, causing significant EMI. If the reference planes are at the same

DC potential, then they can be connected by stitching vias near the signal via transition to provide shorter paths for return currents. However, if the planes are at different DC potentials, then decoupling capacitors must be connected across the planes at these points. In addition, some of the return current flows through the interplane capacitance to close the loop.

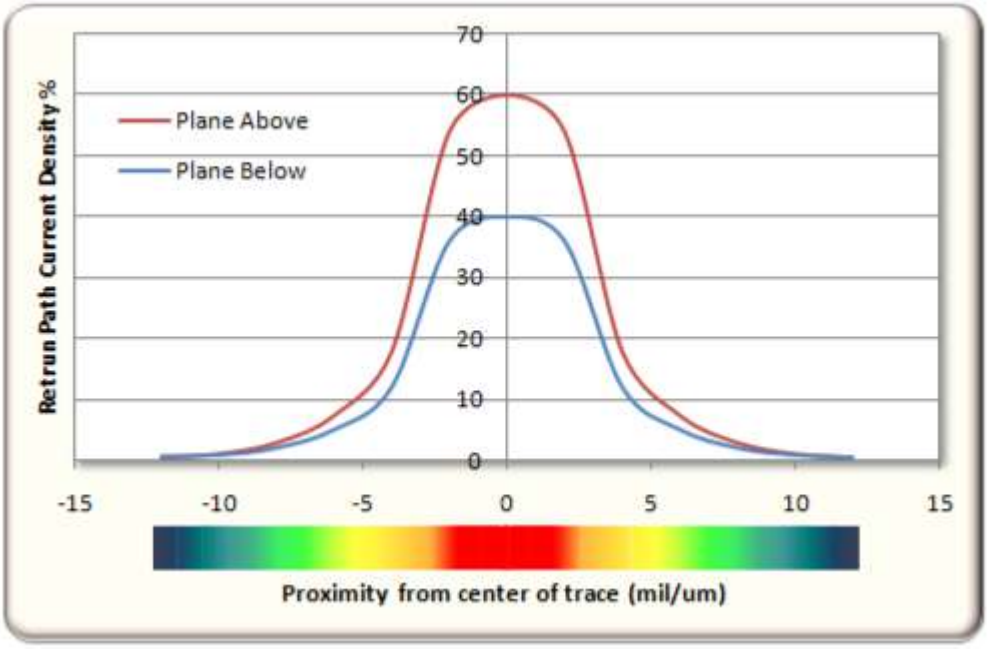

Figure 3 – Return path current density for asymmetric stripline (source iCD Design Integrity)

Figure 3 illustrates the spreading of return current density across the planes above and below the signal path. As the frequency approaches a couple of hundred megahertz, the skin effect forces the return current to the surface closest to the signal trace. It is important to have a clearly defined return current path and to know exactly where the return current will flow. This is particularly critical with asymmetric stripline configurations where one signal layer is sandwiched between two planes. Which plane does the return current flow on?

4. Take corrective action to mitigate the RPDs

Unfortunately, RPDs can never be totally eliminated but we can take steps to minimize the effects significantly. As with PDN Planning, it is all about inductance! If the return path loop area is increased, in any way by RPDs, then the inductance will also increase.

There are the obvious rules to follow such as:

- Never allow a high-speed signal to cross a gap or split in the plane. This creates a large return path loop area and tends to radiate.
- Never route a high-speed signal near the edge of the reference plane. The fringing fields may wrap around the edge of the board and radiate.
- Never place an IC over a split plane. The IC substrate is like a miniature multilayer PCB and may rely on a solid plane placed beneath the IC to provide a continuous return path.

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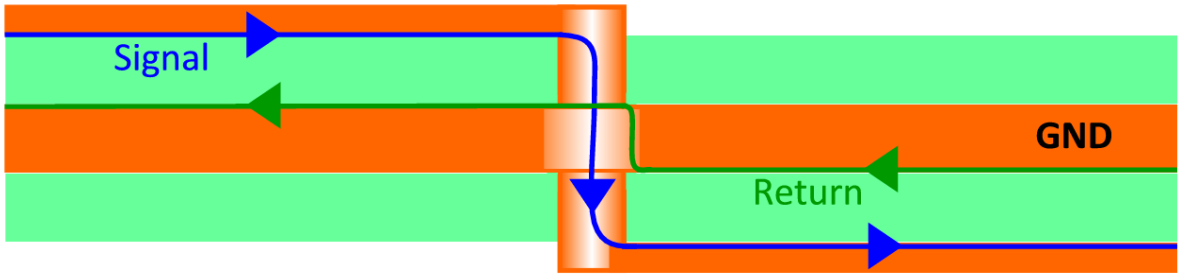

Figure 4 – Central GND plane return path structure

If there are sufficient planes in the substrate, or you have the freedom to add more, then the use of a number of central GND plane structures, with signals on both sides, will mitigate the RPDs as the return path will be in the same plane–albeit on opposite sides. As mentioned, at high frequencies the skin effect forces the return current into the surface of the plane, closest to the signal trace, as shown in Figure 4. So as the signal transitions from one signal layer to the other, about the common GND Plane, the return current also needs to change planes sides. This is achieved through the outer surface of the via antipad, on the plane, creating only a small RPD due to the variation of impedance between the signal layer and via.

Also, when a signal propagates from the driver to the receiver, it creates noise in the power/ground plane cavity. As a result energy is being lost to the PDN, creating effects such as RPDs and increasing insertion loss. By reducing the size of the cavity with a thin, high dielectric constant *(Dk*) material between the planes, ringing at low frequencies is reduced and the cavity resonance moves to the upper band which is above the maximum bandwidth.

Points to Remember

- SSN is a major problem in high-speed systems. But, the underlying issue is really the management of return current paths.
- Current flow is a 'round trip' and the important issue is delay not length.
- Ground impedance is at the root of virtually all signal and power integrity problems–low ground impedance is mandatory for both.
- A ground plane serves well as a signal return, provided the ground is continuous under the signal path.
- RPDs have a huge impact on supply bounce of single ended signals. They produce impedance discontinuities due to the local return inductance and capacitive changes and cause timing push-outs.
- RPDs typically manifest themselves as intermittent operation and degrade the performance of the product which can be extremely difficult to debug.
- Each signal layer should be adjacent to, and closely coupled to, an uninterrupted reference plane, which creates a clear, uninterrupted return path.
- Although power planes can be used as reference planes, ground is more effective as local stitching vias can be used, for the return current transitions, rather than stitching decoupling capacitors which add inductance.
- The return current of a high-speed, fast rise time digital signal will always follow the path of least inductance.
- RPDs tend to divert the return current increasing the loop area, inductance and delay–which is not desirable.
- A via that provides the connection between signal traces, referenced to different planes, creates RPDs.
- The skin effect forces the return current to the surface closest to the signal trace.

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- It is important to have a clearly defined return current path and to know exactly where the return current will flow.
- RPDs can never be totally eliminated but we can take steps to minimize them significantly.
- It is all about inductance! If the return path loop area is increased, in any way by RPDs, then the inductance will also increase.
- The use of a number of central GND planes, with signals on either side, will mitigate the RPDs.
- By reducing the size of the cavity with a thin, high dielectric constant *(Dk*) material, ringing at low frequencies is reduced and the cavity resonance moves in to the upper band.

References:

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High Speed Digital Design – Howard Johnson

Bio:

Barry Olney is Managing Director of In-Circuit Design Pty Ltd (iCD), Australia. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN and CPW Planner, is a PCB Design Service Bureau and specializes in board level simulation. The software can be downloaded from www.icd.com.au