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Pre-layout Simulation

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Summary: *Pre-layout simulation allows a designer to identify and eliminate signal integrity, crosstalk and EMC issues early in the design process. This is the most cost-effective way to design a board.*

Today's high-speed processors, SERDES interfaces and decreased time-to-market requirements are pushing design teams toward more nimble development processes. But there is no point in completing a design on time if it does not work! My motto is: "Simulate twice – build once."

Figure 1 illustrates a Band-Aid solution which may be applied to fix a signal integrity (SI), crosstalk or radiation issue. This is obviously an after-thought and is not the most elegant solution to a problem. Unfortunately, simulation is engaged too often at the end of the design cycle to try and fix a problem, rather than before and during the process—fixing the problem at the source—to ensure design integrity.

Complex multilayer boards should be designed using a proven design methodology, incorporating pre-layout simula-

tion before placing a single chip on the board. Simulation tools can be used to analyze various SI issues like reflections due to impedance mismatches, crosstalk, signal attenuation and power distribution network (PDN) noise—all of which can impact interconnect performance.

Simulation of a PCB design after placement and routing is recommended, but simulation early in the design process is even better. Both are, in fact, essential. Pre-layout analysis allows critical interface topologies, termination schemes, and I/O buffer selection to be defined and analyzed for synchronous, source-synchronous and clock recovery interfaces before placement and routing. This opens your eyes to what the circuitry is actually doing. It also leads to an enhanced perception of what might be a potential issue once the system is built.

Pre-layout simulation also allows a designer to identify and eliminate signal integrity, crosstalk and EMC issues early in the design process. This is the most cost-effective way to design a board with fewer iterations, rather than starting with the find-and-fix-based post-layout simulation.

There are multiple facets to pre-layout analysis, including:

- Stackup planning for controlled impedance, SI, crosstalk, and cost control
- Dielectric material selection for manufacturing yield, and high-frequency operation
- PDN optimization
- I/O buffer and drive strength selection
- Topology optimization
- Termination strategy
- Floor planning for critical components
- Deriving layout routing constraints, including trace width, spacing and length matching
- Signal Integrity analysis to meet the design specifications, with respect to noise margins, timing, skew, crosstalk, and signal distortion

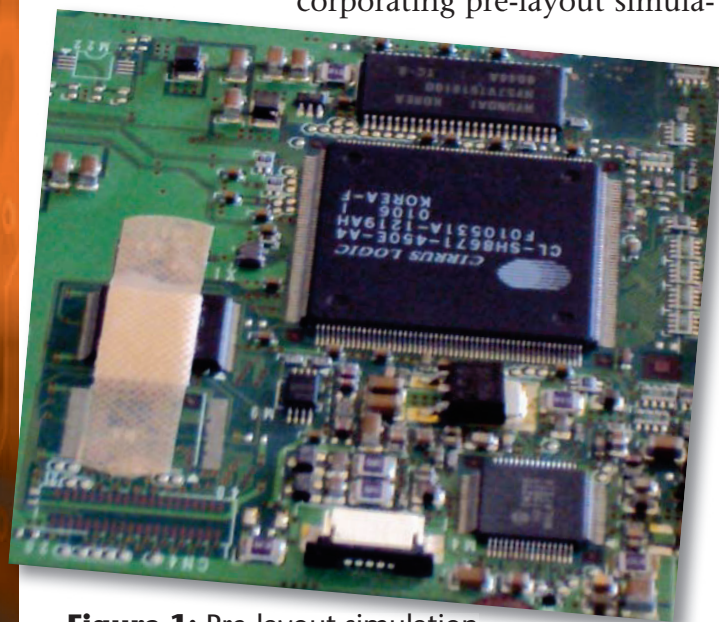


Figure 1: Pre-layout simulation can eliminate more-costly Band-Aid solutions on the back end of the design process.



Figure 2: DDR2 data signal with series terminator.

Since I have already addressed the first three sections in previous articles, I will move on from there. I recommend using the ICD Stack-up Planner and PDN Planner to simulate the design before diving into the steps described in the following paragraphs.

I/O Buffer and Drive-strength Selection

I/O buffer and drive-strength selection can be analyzed in pre-layout simulation. A vendor-provided IBIS model should contain all available drivers for each model, and may, for example, include buffer models with 8 mA, 12 mA, and 16 mA drive current. The mid-level 12 mA signal is generally required, unless there is a long transmission line with multiple loads. This may be the case on a mother board when driving a number of DIMM modules, for instance.

Topology Optimization

The schematic description that includes the arrangement of a network, its nodes, sequence, and connecting transmission lines is generically referred to as the interconnect topology. In order to avoid signal quality and timing problems, and to minimize manufacturing costs, thorough topology analysis is critical to the successful implementation of a high-speed interconnect. Ideally, this analysis should be done up-front before placement and routing.

Topology optimization involves:

- Selecting optimal topology style for signal integrity, timing and EMC
- Shortening traces and stubs to their critical length or shorter, where possible

The most basic topology is a simple point-to-point connection between a driver and receiver. This topology is commonly used for busses or otherwise grouped traces. A good example of this would be the data banks of DDR memory. Left unterminated, these traces may be too

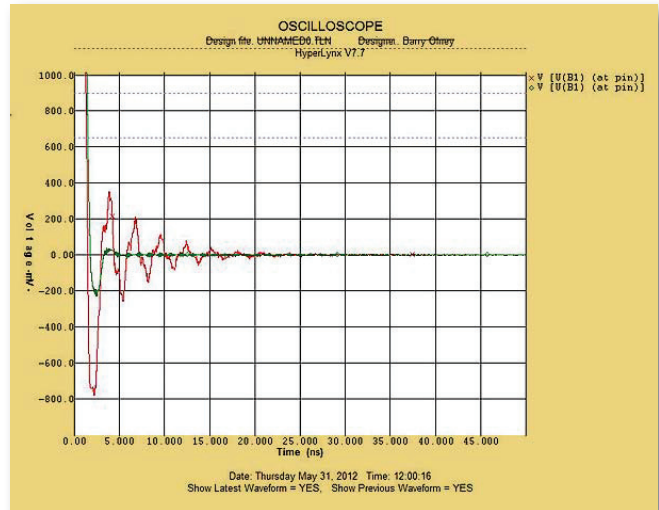


Figure 3: Ringing of the data signal due to reflections.

long (more than 1/10 rise time), and reflections become a problem.

Figure 2 illustrates a Xilinx Virtex 4 transceiver driving a DDR2 data signal into a 53-ohm transmission line. The interconnect is three inches long—a little bit longer than normal. Initially, the signal was simulated with no series termination, resulting in the red waveform in Figure 3.

Reflections deteriorate signal quality and timing, and contribute to both crosstalk and radiation. Figure 3 shows 790 mV of ring back (red waveform) caused by reflections. It should be noted that reflections are only of concern for interconnect lengths that exceed 1/10 of the driver’s rise time (in nanoseconds). Since a signal in a typical dielectric travels at about 6 inches per nanosecond (5.8 inches per nanosecond, if you want to be exact), you can divide the end-to-end interconnect length in inches by six to get the interconnect length in nanoseconds. If the driver’s edge rate is more than 1/10 this number, termination will be required, more often than not.

Termination Optimization

There are four primary types of termination types for single-ended signals, including DC parallel (a.k.a., a pull-up resistor), AC parallel, Thevinin, and Series termination. In this article, we will focus on DC parallel and series termination, which are commonly employed

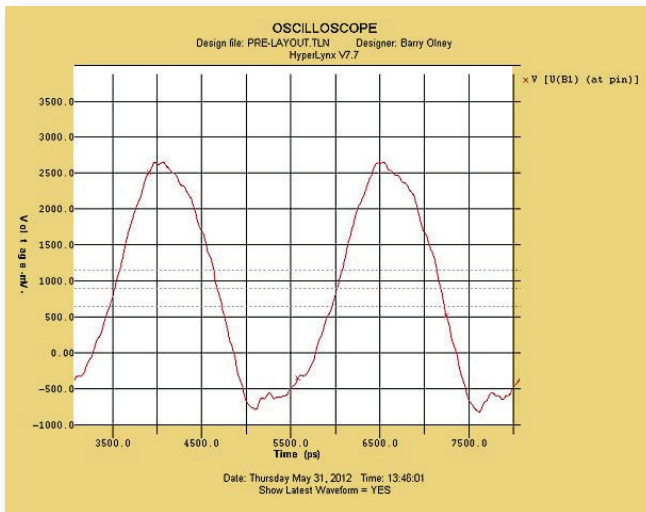


Figure 4: Pre-layout simulation of the data signal (MDQ0).

in high-speed design. The value of the series terminator is calculated using the following relationship:

$$R_{series} = \text{Line Impedance} - \text{Source Resistance}$$

The ICD Stackup Planner can be used to calculate the transmission line impedance. The source resistance should be available in the driver datasheet, or can be obtained from the IBIS model.

Adding a 33-ohm series terminator close to the driver dampens the ringing to 200 mV, as shown by the green waveform in Figure 3.

Figure 4 shows the results of pre-layout simulation of a typical DDR2 data signal. In this case, the data signal did not need termination, saving a component, and a bit of board space, which is a savings that can add up on a high-volume product.

Another topology type is the multi-drop or daisy chain—commonly used when signals are distributed to multiple components. DDR2 address and clock lines are sometimes routed

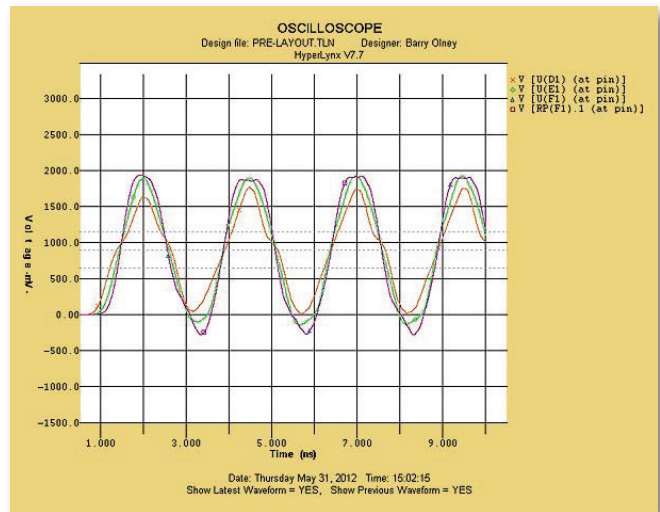


Figure 6: Pre-layout address simulation results (MA0).

in this way. Far-end, DC parallel termination is often useful in multi-drop connections. In the DDR2 address case of Figure 5, this would be a VTT pull-up resistor at the end of each address line.

Pre-layout simulation results for an address line shown in Figure 6 include the effect of a 22-ohm series terminator near the driver, and a 200-ohm pull-up at the end of the line to VTT (0.9V). The VTT pull-up is typically between 100 – 200 ohm and is determined by simulation.

Establishing Routing Rules

Before starting placement and routing, detailed interconnect-routing constraints should be established. These are of course based on the pre-layout simulation. The matched length data, address, strobe/clocks, command and control signals should be setup in the constraints editor, along with differential pair rules, clearance between signal groups (to prevent crosstalk) giving priority to critical signals. Furthermore, return paths should be

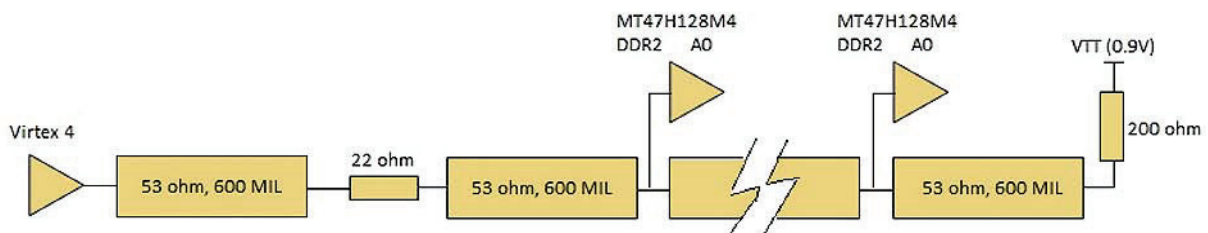


Figure 5: DDR2 address signal model.

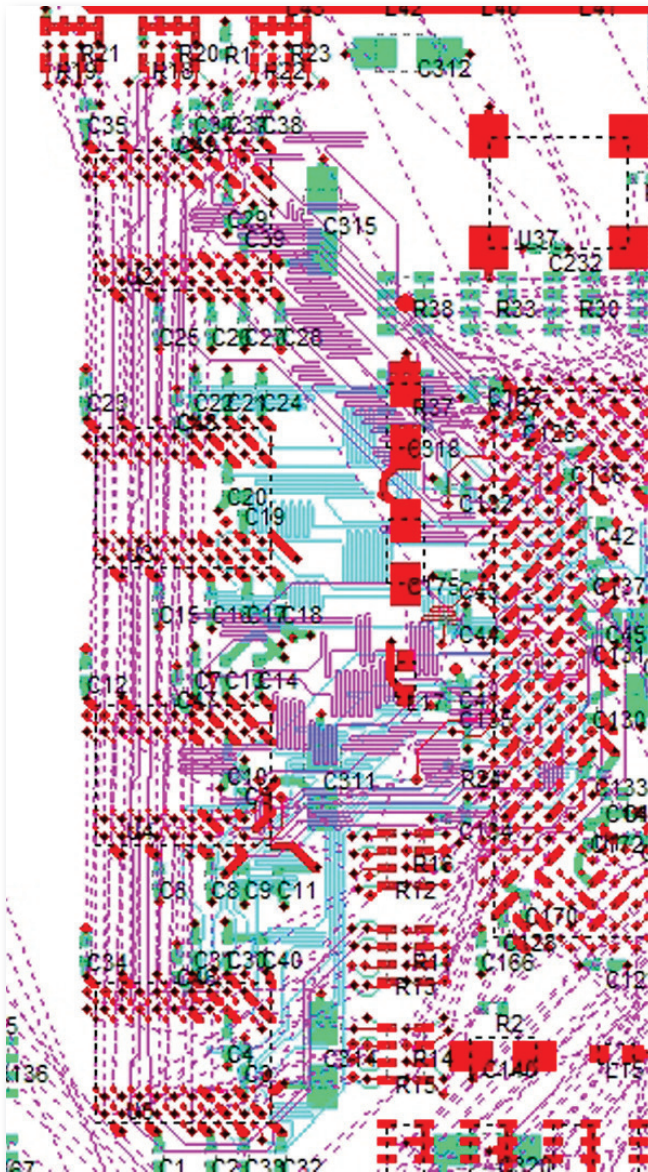


Figure 7: Data and strobe lines for each data lane.

checked to ensure that there are no split planes or obstacles to delay the return current. Further details of the tolerances required are highlighted in my previous article “PCB Design Techniques for DDR, DDR2 & DDR3.”

Figure 7 shows the data lane routing for a DDR2 design. The trick is to closely match the data signals, data masks and associated strobe (which act as the data clocks). Results of pre-layout simulation of the data signals in Figure 4 show very close correlation with post-route simulation of the same signals in Figure 8.

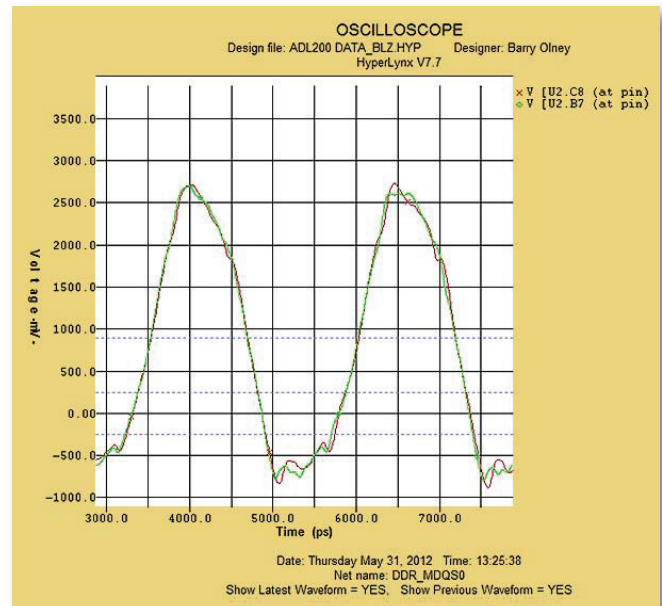


Figure 8: Shows close timing between the data signals (MDQ0) and the data strobe (MDQS0) for a DDR2 interface.

Figure 9 shows the results of the routing process. However, before doing this, the daisy chain topology was simulated to establish whether the VTT end-of-line pull-up is required, and if a series terminator is also necessary.

Figure 10 highlights the routed MA0 address signal starting at the processor (U1)—through a series terminator, then on to U5, U4, U3 and U2—finally being pulled up by R18 to VTT. Fortunately, source synchronous busses have a unique immunity to crosstalk, provided that the ringing has settled by the sample and hold times.

The post-layout simulation of the address signals (Figure 11), confirms that the correct selection of topology and termination strategies was made. The fact that the prototype board worked the first time, when tested, is also a very good indication.

The DDR2 differential clock(s) should also be routed to the exact same length, and daisy chained, just as the address bus should be. The time or skew between these should fall within specs. This brings us to the next point in pre-layout simulation: floor planning. Obviously, once you have established the individual lengths of the interconnects—with or without

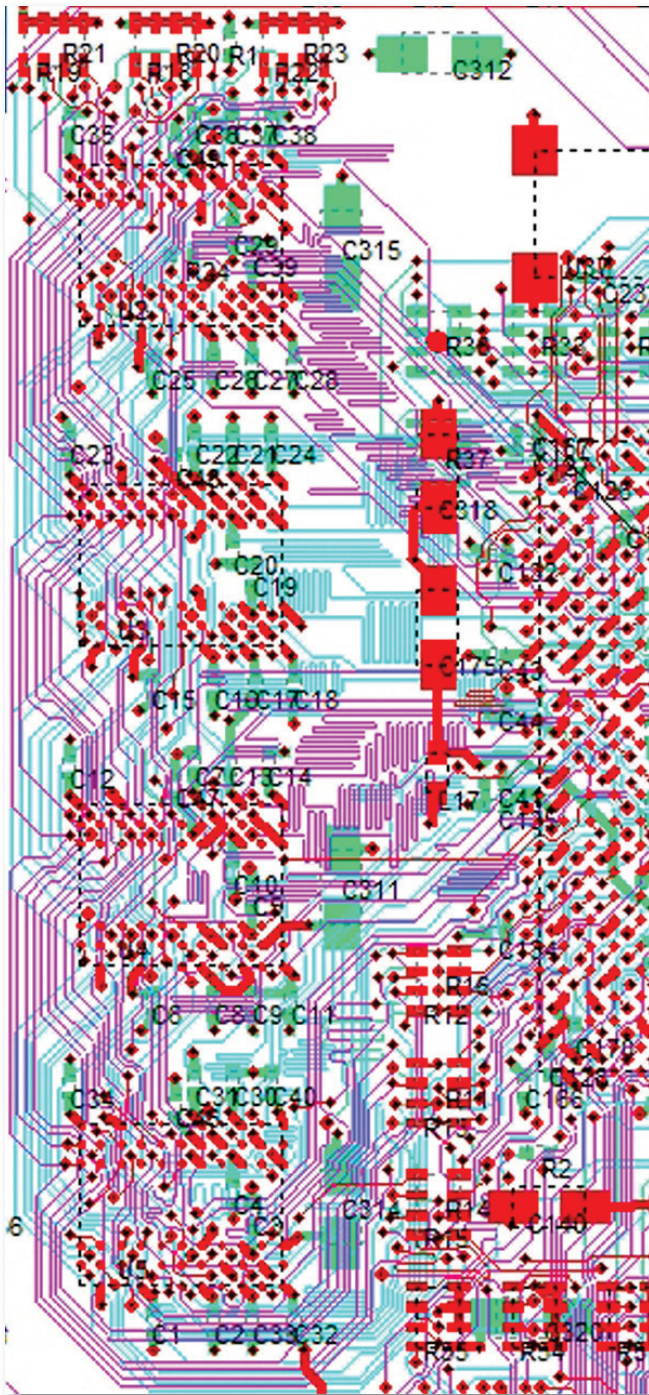


Figure 9: Routing results.

termination—you have the distance required to place the memory chips relative to the processor. The processor should be placed in the center of the board, whenever possible, to aid fanout and routing to peripheral devices.

Figure 12 shows the address signals, routed in a T section. The signals start at the processor

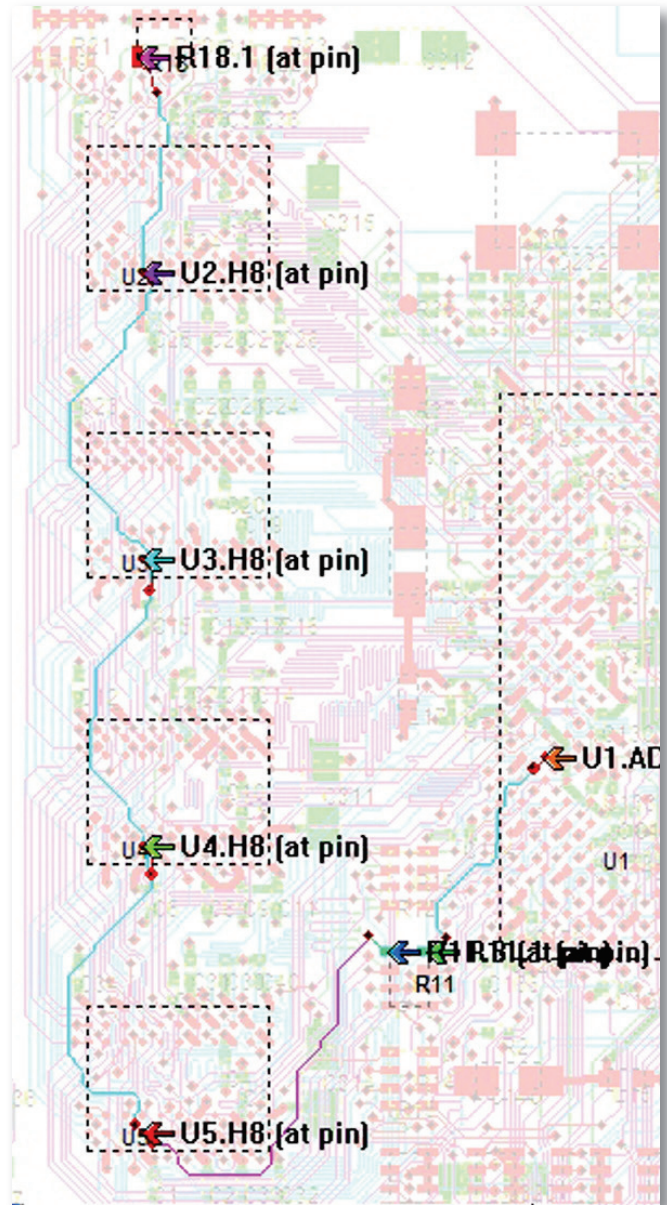


Figure 10: Multi-drop address line, MA0.

on the right, and route down at 45 degrees before splitting off to the memory chips above and below. In this case, the delay of the 45-degree sections should be identical, and the delay on each of the branches should be identical—quite a challenge for the novice PCB designer to tackle!

In a star topology, all signals emanate from a central node. The electrical delay for each leg of the star should be identical, and the loads should be the same—otherwise a series terminator can be used at the start of each leg to balance the delay and loading.

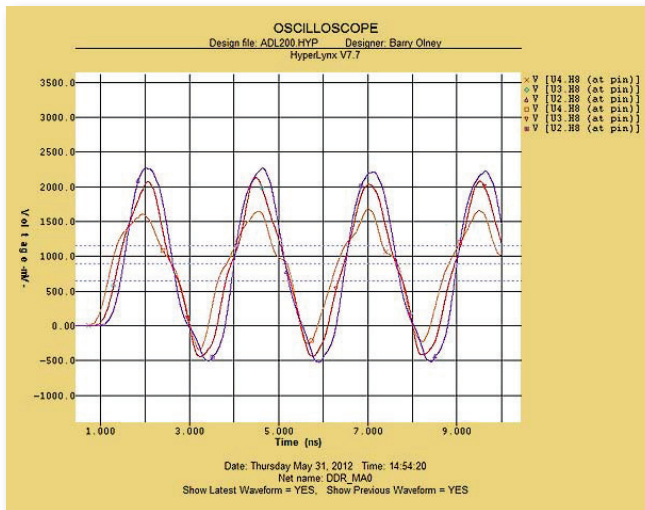


Figure 11: Post-layout address simulation results (MAO).

By utilizing a PCB board-level simulation service, you can be assured that your PCB will be reliable and manufacturable, will conform to specifications, as well as passing the relevant compliance tests. Saving one board spin or prototype can easily cover the cost of such a service, and the peace of mind—in terms of reliability—is priceless.

Points to remember

- Problems can be identified and prevented using pre-layout simulation
- Select the optimal topology style for signal integrity, timing, crosstalk, and EMC
- Unterminated high-speed traces should be less than 1/10 the driver rise time
- Closely match the data signals and data mask to the associated strobes, and the address, command and control signals to the clocks
- Pre-layout simulation allows you to experiment with termination strategies
- The processor should be placed in the center of the board to aid fanout and routing to peripheral devices
- Establish routing constraints based on the pre-layout simulation
- Return paths should be checked to ensure there are no split planes or obstacles to impede the return current

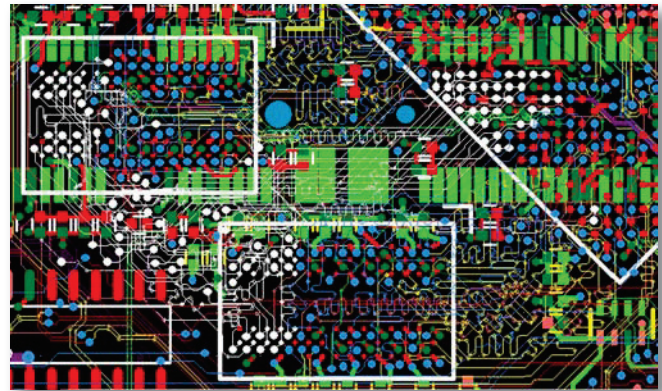


Figure 12: T-section routing of DDR2 address signals.

References

The ICD Stackup Planner with Field Solver Technology can be downloaded from www.icd.com.au. **PCB**

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