

# BOARD LEVEL SIMULATION SPECIALISTS

ICD Stackup Planner - offers engineers/PCB designers unprecedented simulation speed, ease of use and accuracy at an affordable price

- 2D (BEM) field solver precision
- Characteristic impedance, edge-coupled & broadside-coupled differential impedance
- Unique field solver computation of multiple differential technologies per stackup
- Heads-up impedance plots of signal and dielectric layers
- User defined dielectric materials library - over 16,250 materials up to 100GHz

ICD PDN Planner - analyze multiple power supplies to maintain low impedance over entire frequency range dramatically improving product performance

- Fast AC impedance analysis with plane resonance
- Definition of plane size/shape, dielectric constant & plane separation for each on-board power supply
- Extraction of plane data from the integrated Stackup Planner
- Definition of voltage regulator, bypass/decoupling capacitors, mounting loop inductance
- Frequency range up to 100GHz
- Extensive Capacitor Library – over 5,250 capacitors derived from SPICE models

# Postmortem Simulation

by **Barry Olney**

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**SUMMARY:** *Developing the practice of performing a postmortem analysis on every project facilitates a culture of continuous improvement. This embedded culture of ongoing, positive change is the best way to ensure long-term success.*

Often we find that PCB simulation is engaged too late in the design cycle. This results in the simulation process becoming more a post-mortem to uncover what has gone wrong with the design and how it can be resurrected to work as intended.

In my work as a high-speed analyst, I sometimes get called on to fix problems that could have been prevented. However, a total disaster can usually be avoided and final success achieved (providing the conceptual design has been validated).

Ideally, every high-speed design should be exposed to the preventative medicine of pre-layout simulation and proactive stackup and power-delivery optimization.

As with any forensic postmortem, a thorough external examination is undertaken to see if there are any visible signs of impairment that may identify the cause of the problem. This is what I refer to as “eyeballing” the design. It is actually amazing what can be picked up just by looking closely at the PCB database. I think we have all experienced the case where we simply cannot see the obvious because we are intimate-

ly involved in the design – that is, our subconscious does not warrant rechecking the obvious. That is why I always advocate having a second, equally qualified person thoroughly check a PCB before handover to manufacturing.

The following is a short list of issues to regularly check in a design:

- Minimum edge/tooling hole clearances and component to edge of board clearance.
- Thermal reliefs are not compromised.
- Split planes (if present) are correctly placed.
- No critical nets cross split planes.
- No critical (high-speed) nets in the analog areas.
- Critical nets must not change reference planes unless accompanied by a stitching via or bypass capacitor.
- Matched length signals – memory data, strobe, clock, address, control and command signals are routed to specs.
- All critical nets are buried between solid planes. The allowable length of the exposed portion of a critical net is limited.
- All critical nets must be routed with adequate clearance to avoid crosstalk.
- All power and ground traces longer than 500 mils must be wide enough to carry the specified current.

## POSTMORTEM SIMULATION *continues*

- All oscillators must be placed within 500 mils from the clock driver.
- Critical nets are not within 3x trace width of the edge of their reference plane.
- Decoupling capacitors are placed within 500 mils from each IC power pin.
- The trace connecting between a decoupling capacitor to the associated via to the power/ground reference plane must be no longer than 200 mils and be 20 mils wide.

Of course, there are many more rules embedded in the experienced designer's head. A digital simulator may also pick up some of these rule violations, but software automation is not a surrogate for good design judgment, and doing forensics on your own designs.

Next, the examiner takes a look inside at the major organs – the PCB stackup and power distribution networks (PDN) in this case.

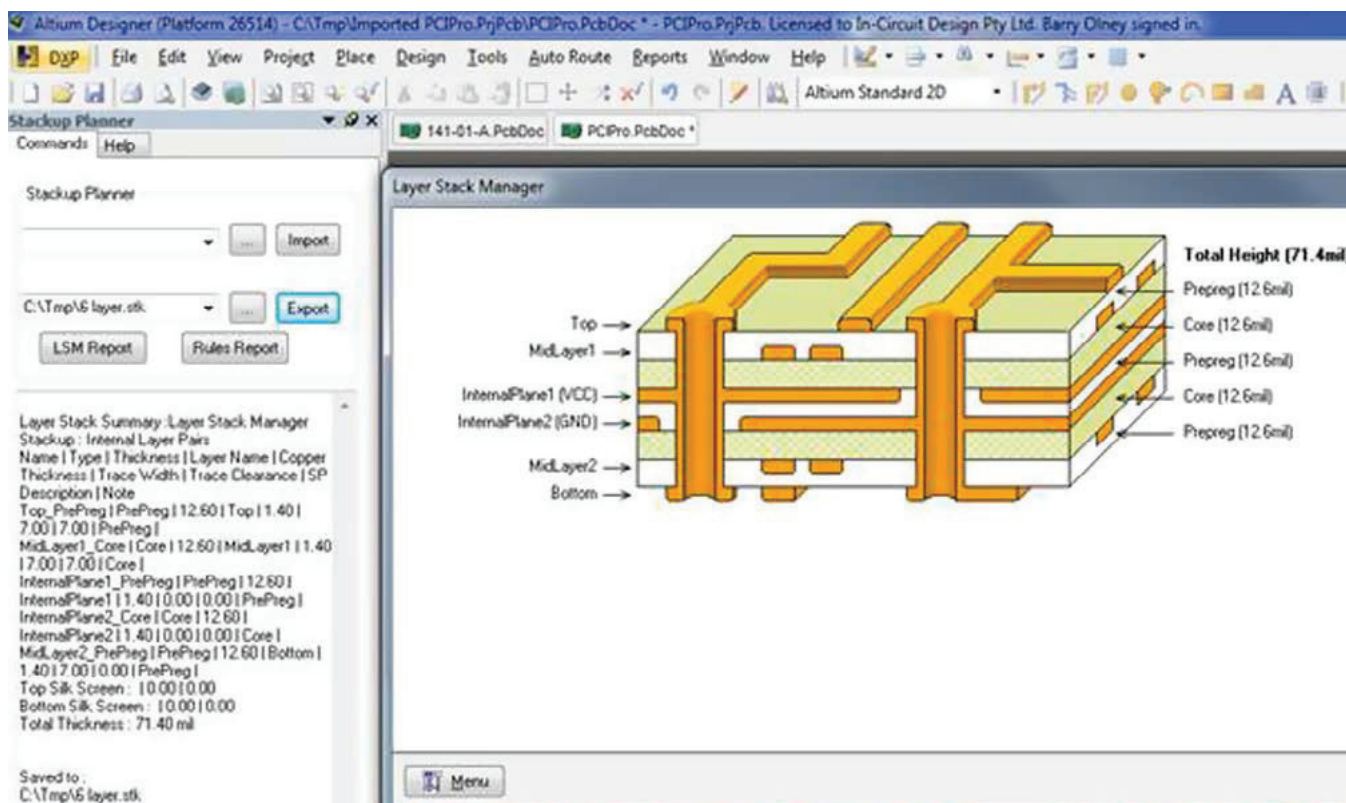
A poorly designed substrate, with inappropriately selected materials, can degrade the electrical performance of signal transmission,

increasing emissions and crosstalk, and it can also make the product more susceptible to external noise. These issues can cause intermittent operation, due to timing glitches, and interference dramatically reducing the product's performance and long term reliability.

The less than desirable stackup in Figure 2 can be exported from Altium Designer (S09 to R13) into the ICD Stackup Planner to incorporate dielectric materials and adjust the stackup for optimal performance. The stackup is then modified to give 50 ohms single-ended and 100 ohms differential impedance by moving the plane layers and adding dielectric materials from the Stackup Planner's dielectric materials library.

Once modified, the stackup in Figure 3 can then be exported back to Altium Designer to also include impedance-controlled routing and differential rules. Plus, the stackup can also be exported to HyperLynx LineSim for pre-layout analysis, BoardSim for post-layout analysis, PADS and Allegro.

To promote communication with PCB fabricators, an Excel spreadsheet output (Figure 4)



**Figure 2:** Exporting the stackup from Altium Designer's layer stack manager.

is also available from the [ICD Stackup Planner](#). It is for this reason that the ICD (.stk) format is fast becoming the industry standard for impedance controlled data collaboration between

engineers, designers and fabricators.

If the product is showing “flakiness” in functional tests, or even in production, the cause may involve inadequate PDN design. Ideally,

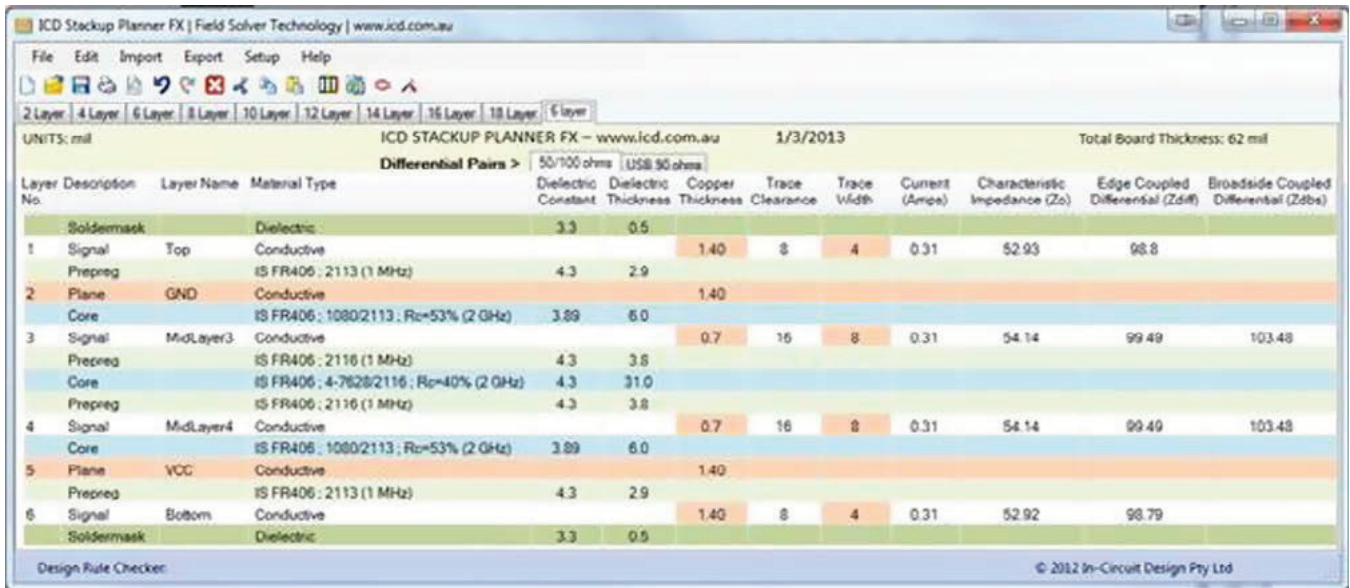


Figure 3: The modified stackup can be exported from the ICD Stackup Planner back to Altium Designer.

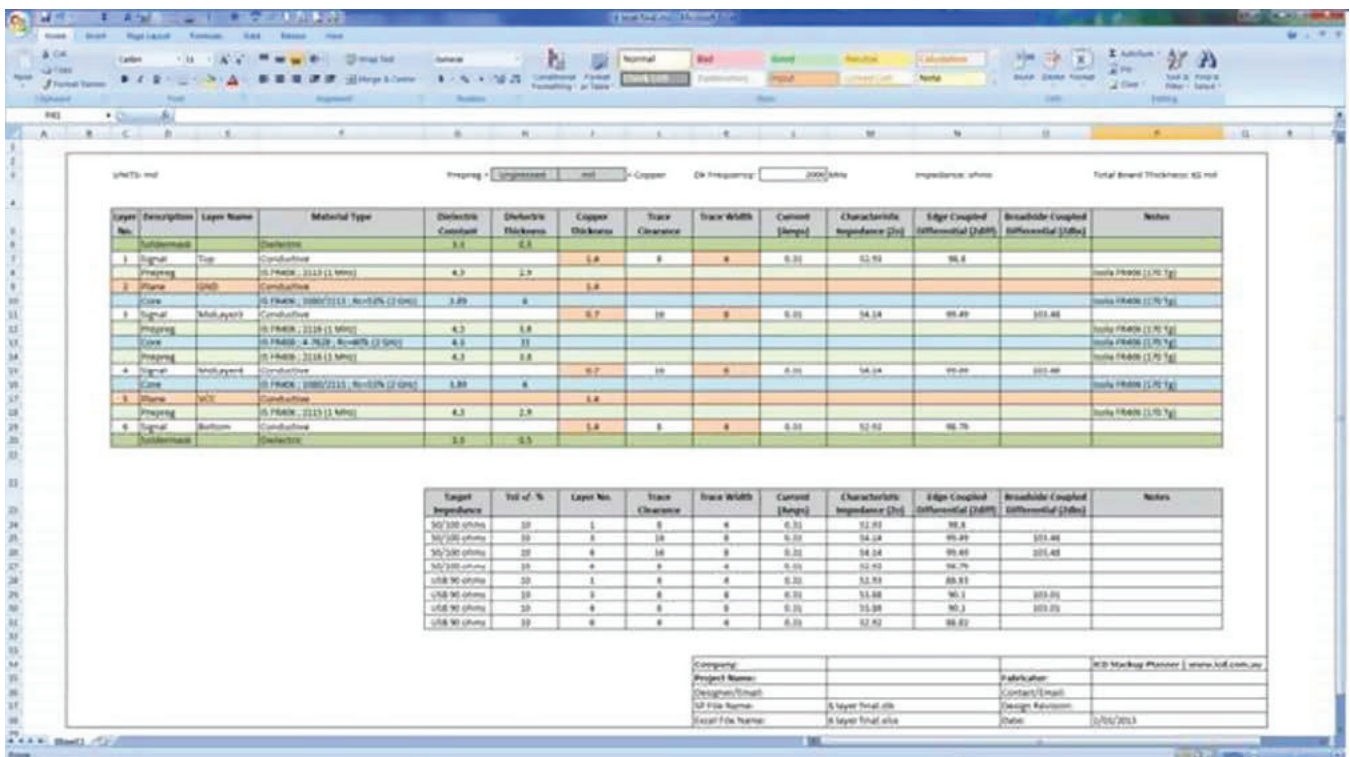


Figure 4: The stackup, exported to Excel, allows engineers and PCB designers to communicate more effectively with fabricators.

**POSTMORTEM SIMULATION** *continues*

issues like this should be resolved before a single chip has been placed on the board.

Decoupling capacitors supply instantaneous current (at different frequencies) to the drivers until the power supply can respond. In other words, it takes a finite time for current to flow from the power supply circuit (whether on-board or remote), due to the inductance of the trace, and/or leads to the drivers. Every decoupling capacitor has an equivalent series inductance (ESL), causing its impedance to increase at high frequencies. In order to reduce this inductance, a number of small-value decaps can be placed in parallel, as close as possible to each power pin using a thick, short trace or – even better – directly to the low-inductance plane.

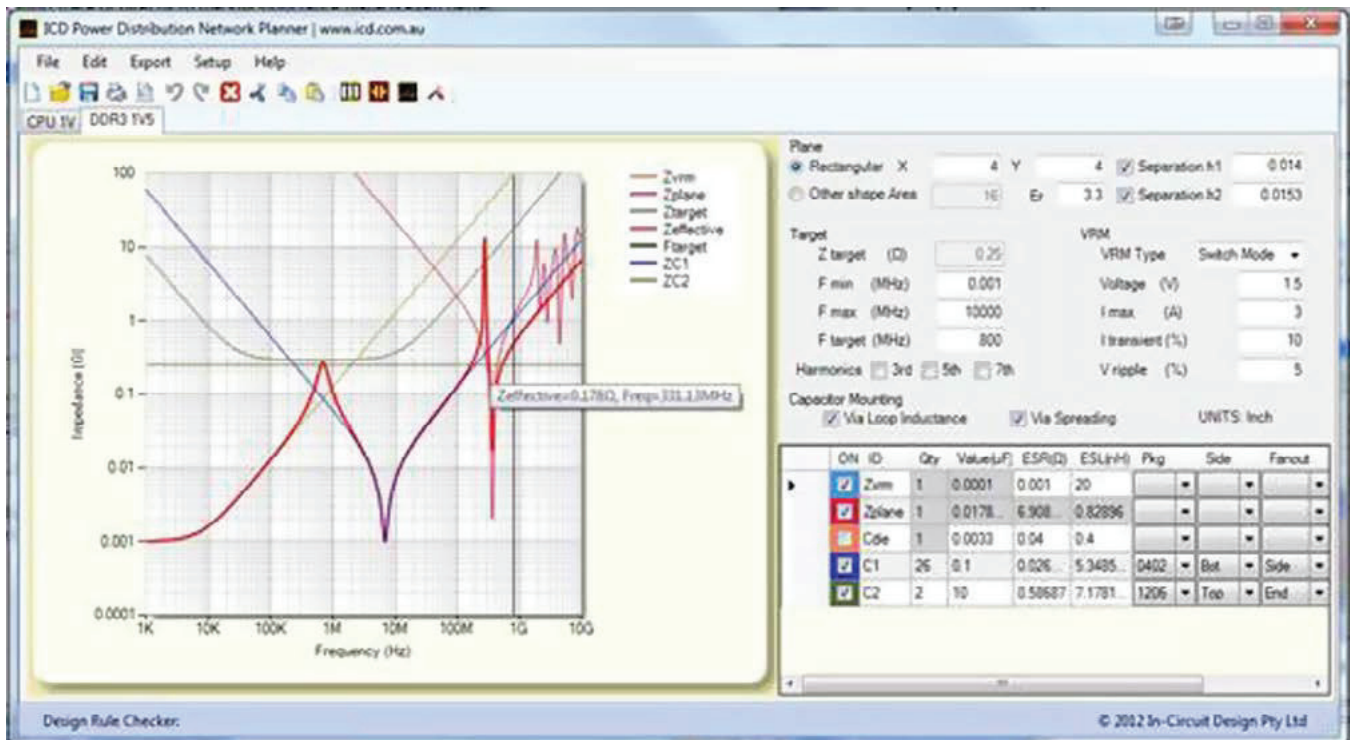
The selection of capacitors, with the correct attributes, is a trial and error process and needs to be done with the assistance of an analysis tool. The ICD PDN Planner (available for download from [www.icd.com.au](http://www.icd.com.au)) illustrates a typical decoupling scheme in Figure 5.

In a postmortem, blood tests are also sent to pathology to be analyzed. This gives the pathologist a few clues regarding systemic issues that

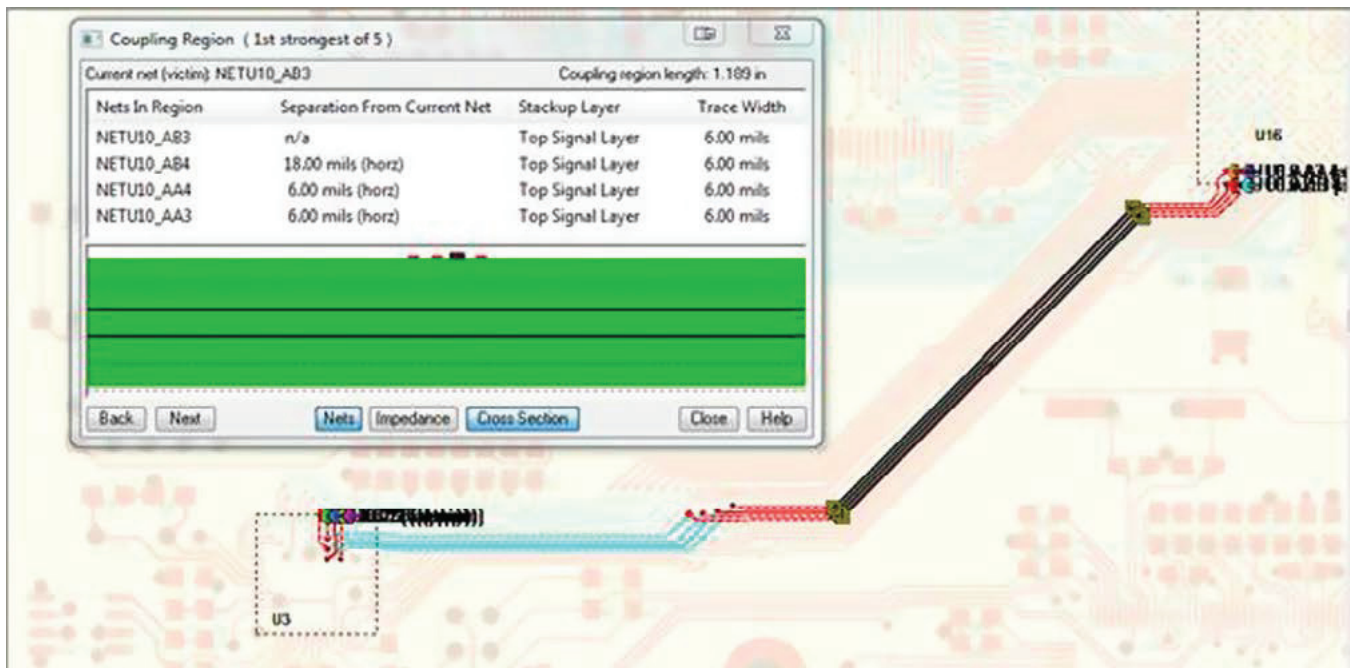
might escape initial observation. In my mind, this is analogous to whole-board analysis, with a simulator like Mentor Graphics HyperLynx. Batch simulation flags signal integrity, crosstalk, timing, and EMC hot spots across the entire design. Default IC characteristics, crosstalk of 150mV maximum and EMC to FCC, CISPR Class A and B are setup in the simulator.

The post-layout simulation analysis is an extensive interactive board level simulation that takes the analysis to the next level, simulating trouble spots identified by the batch analysis in order to further resolve the issues with greater accuracy. The virtual oscilloscope and spectrum analyser give the examiner another view, similar to the images of an MRI and X-ray films which allow the examiner to visualize internal trauma and minute fractures. The simulations allow in-depth analysis of signal integrity and crosstalk within the substrate.

Crosstalk is typically picked up on long parallel trace segments. These can be on the same layer but may also be broadside-coupled from the adjacent layer. It is for this reason that orthogonal routing is recommended on adja-



**Figure 5:** The ICD PDN Planner illustrates a typical decoupling scheme for 1.5V DDR3 supply.



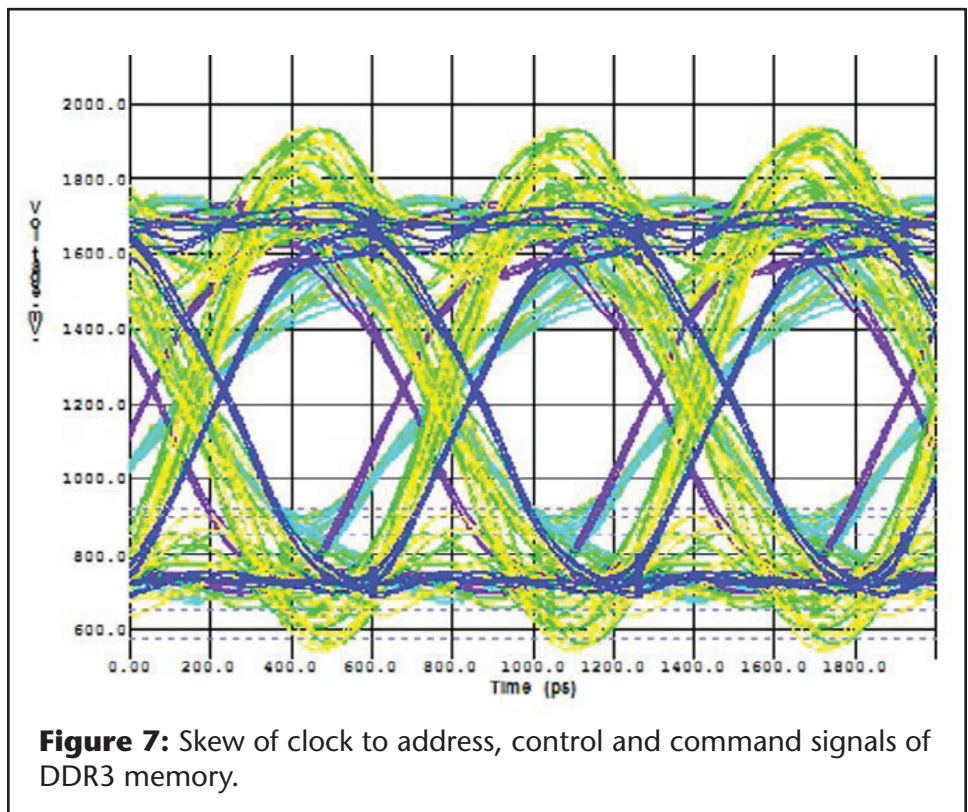
**Figure 6:** HyperLynx shows crosstalk on manually routed parallel traces segments.

cent layers (between planes) to minimize the coupling area. Figure 6 shows this crosstalk on the 45-degree routes. It is recommend that segments are only routed to a maximum of 500 mils in parallel or that the clearance is increased to at least 3x trace width to avoid coupling.

The next step in the analysis is to examine timing: This is the heartbeat of the design. Irregular heartbeat can have catastrophic affects just as irregular timing can cause intermittent faults in a digital system. In the classic high-speed design flow, timing specifications and simulation results are compared to check skew and set and hold times to ensure everything is operating like clockwork.

Figure 7 illustrates the

timing of the clock compared to the address, control and command signals of a DDR3 memory design. The skew can be up to 200ps for



**Figure 7:** Skew of clock to address, control and command signals of DDR3 memory.

**POSTMORTEM SIMULATION** *continues*

DDR3-800. Also, the skew between data lanes and data strobes should be kept to less than 125ps and the eyes should be wide open. DDR3 is much easier to route, in fact, than DDR2 as leveling can be used to synchronize the delay of groups of signals. All critical signals are checked with the physical information that is obtained from the PCB data base (e.g., trace lengths, clearances, vias, etc.) to ensure that the design complies to specification.

**Conclusion**

Developing the practice of performing a postmortem analysis on every project – identifying both the good and the bad – facilitates a culture of continuous improvement. Embedding a culture of ongoing, positive change inside a project delivery organization is the best way to ensure long-term success. Postmortems are an important link in this chain of positive improvement.

**Points to remember:**

1. Ideally, the simulation should be done during the design process to ensure design integrity.
2. A postmortem should be performed on every project, creating a culture of continuous improvement.
3. For a project that suffers from intermittent flakiness, the postmortem can begin with a thorough external examination – a second set of eyeballs – looking for the obvious.
4. The PCB stackup can be the source of problems that include impedance mismatches, signal integrity problems, crosstalk, or emissions. As part of the stackup optimization process, a PCB stackup can be exported from several PCB environments to the ICD Stackup Planner to incorporate dielectric materials and adjust the stackup for optimal performance.
5. Once modified, the stackup can then be exported back to the PCB environment or to HyperLynx for signal integrity, crosstalk, and EMC analysis. With Altium Designer, impedance and differential routing rules can also be incorporated into the export.

6. To improve communications with PCB Fabricators, an Excel spreadsheet output is also available.

7. The design of the PDN is another important part of the conceptual design process, and should be analyzed as part of a comprehensive postmortem, as well.

8. Post-layout (board-level) analysis can find systemic trouble spots in a design.

9. Crosstalk is typically picked up on long parallel trace segments.

10. Interactive simulation takes the investigation process deeper, including detailed signal integrity analysis, as well as crosstalk and timing.

11. Timing is the heartbeat of the design. Irregular timing can cause intermittent faults in a digital system. **PCBDESIGN**

**References**

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3. Beyond Design: [Intro to Board-Level Simulation and the PCB Design Process](#) – Barry Olney
4. Beyond Design: [Mixed Digital-Analog Technologies](#) – Barry Olney
5. [PCB Design Techniques for DDR, DDR2 & DDR3, Part 2](#) – Barry Olney
6. [PCB Design Techniques for DDR, DDR2 & DDR3, Part 1](#) – Barry Olney
7. The ICD Stackup and PDN Planner can be downloaded from [www.icd.com.au](http://www.icd.com.au)

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Barry Olney is the managing director of In-Circuit Design Pty Ltd (ICD), Australia. The company developed the ICD Stackup Planner and ICD PDN Planner software, and is a PCB design service bureau that specializes in board-level simulation.