Beyond Design: Plane Jumpers

by Barry Olney | In-Circuit Design Pty Ltd | Australia

The key to building the optimum board stackup is to determine how and where the return currents flow. But it is also just as important, to have the board constructed to your specifications – having *Engineering* drive fabrication – rather than delegating impedance control and material selection to the *Fab Shop*.

Moats, islands, cut-outs in the ground plane, isolated power planes, floating ground regions, and a host of other intricate layout techniques are often used by PCB Designers to reduce crosstalk, EMI, and to otherwise improve overall system performance.

But, a high-speed signal crossing a split in the plane causes problems along at least three dimensions, including signal quality, crosstalk, and EMI. The problem is the impedance discontinuity in the signal path crossing the split. The discontinuity reflects energy back toward the source – particularly the higher-frequency components of the signal. At high frequencies, the return current follows the path of least inductance – which is directly below the signal trace – but that path is broken by the split. The reason for this discontinuity is the fact that the return current has to find an alternate path back to the source, creating a large loop area, and a nice little antenna for differential-mode radiation.

It is important to keep in mind that both ground and power planes (any plane) can be used as the reference plane and return current path for a signal.

The key to a successful mixed digital/analog design is functional partitioning, understanding the current return path, and routing control and management … not carving up ground planes. It is always better to have just one single reference (ground) plane for a system.

I mentioned 'Plane Jumpers' briefly in a recent column '[Mixed Digital Analog Technologies]' where I said: **"**If a digital signal(s) must cross a split in the power reference plane a 'Plane Jumper' decoupling capacitor (100nF) can be placed close to the offending signal(s) to provide a path for the return current between the two supplies (e.g. 3.3V —||— 1.5V)."

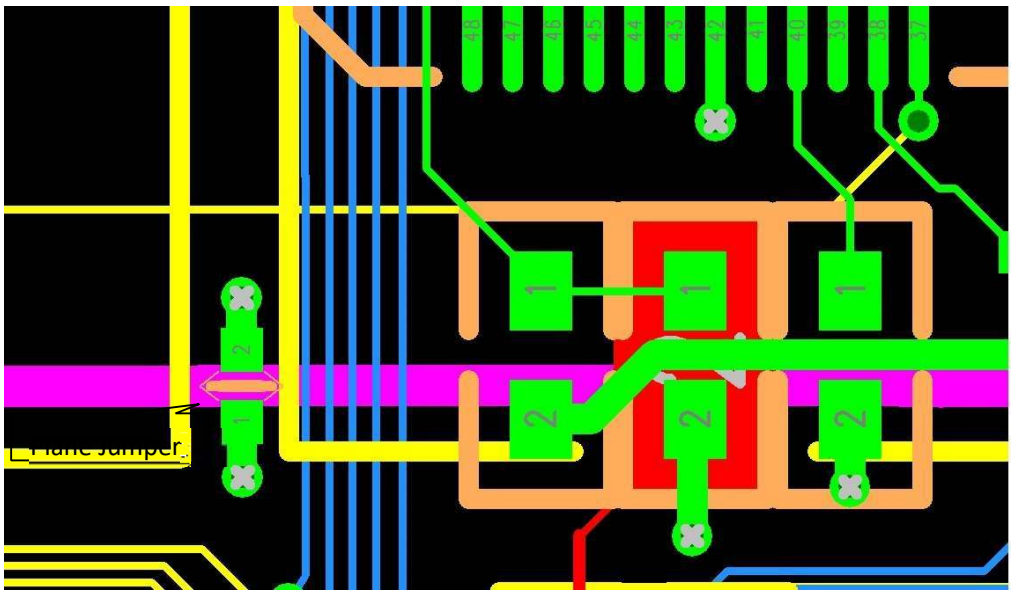


Figure 1. The return current path uses the capacitor to bridge power reference planes

In Figure 1, the gap totally isolates the power reference planes, so a 'Plane Jumper' capacitor is used to allow the return current to bridge the gap in the planes from 3.3V to 1.5V. This is quite effective, but should be only used as a last resort, if you cannot avoid routing such a signal across the gap. I must say that it does look weird– having a decap on the schematic between 3.3V and 1.5V, where decaps are normally placed between power and ground.

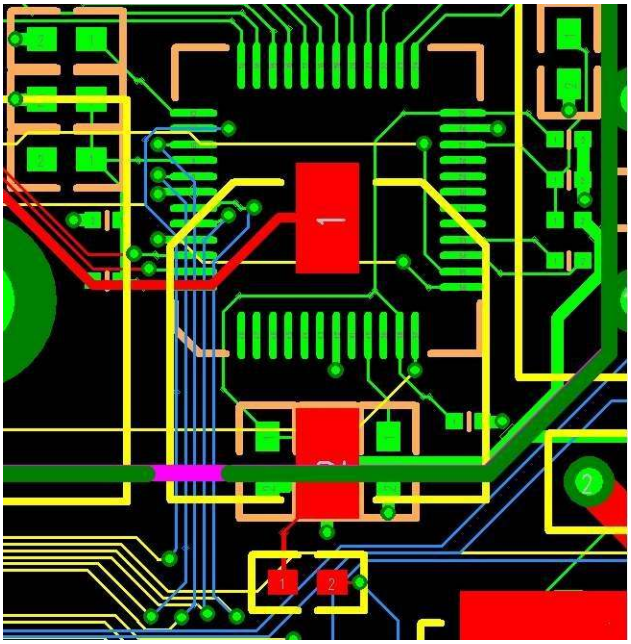


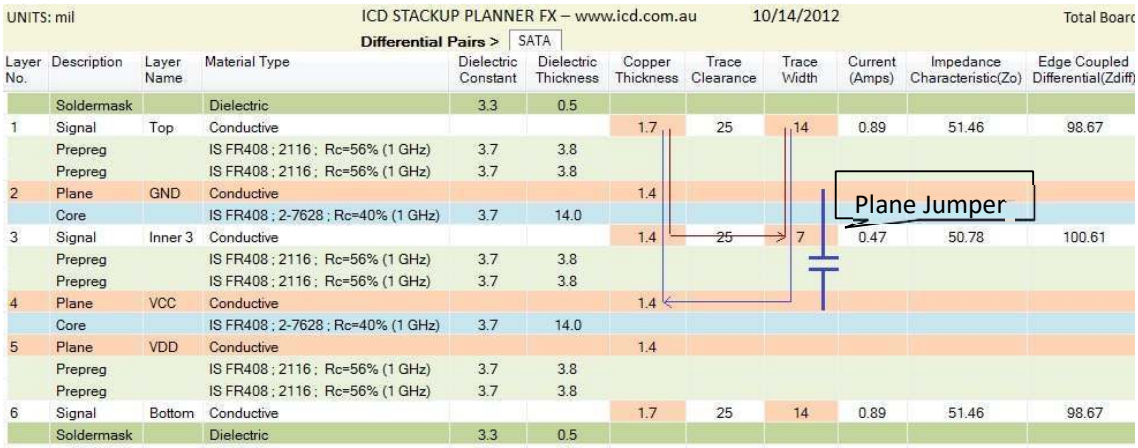
Figure 2. Control signals cross over the 'Bridge' of a split GND plane

Figure 2 illustrates the correct way to tackle this situation – control signals crossing over a 'Bridge' of a split plane. The (blue) traces are grouped together, with a continuous ground plane beneath, providing a reliable return path for these signals. The trick is to always reference a signal to a solid plane – not to split the reference plane. The power plane can be split providing it is not used as a reference plane.

But that is the most basic use of a 'Plane Jumper'. Let's look at where else in the design these magic jumpers can be employed.

ICD recently simulated a board where designers intended to route high-speed signals from a chip to a connector on top of the board. The routing fanned out from the BGA, went directly to layer 3, then popping back up through a via to a connector on the top layer. This seems perfectly reasonable. But, looking at the stackup in more detail, the signal was first referenced to the GND plane on layer 2; then, as it transitioned to layer 3, its reference plane changed to VCC (layer 4) due to proximity. There is, in this case, only one way for the return current to "jump" planes, and that is by finding the nearest VCC to GND decoupling capacitor – which may be a long distance (relatively) from the signal transient, creating a large loop area and undesirable common-mode currents. This can all be avoided by placing a "Plane Jumper" (decap), close to the signal-via transition, between VCC and GND.

In the case, where there are multiple ground planes on a PCB, we cannot simply assume that "ground is ground" and be sure that the return current will find its way back to the source. GND stitching vias should be placed next to each signal-via transition to stitch the GND planes together, providing a clear return path.



Layer No.	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Impedance Characteristic(Zo)	Edge Coupled Differential(Zdiff)
	Soldermask		Dielectric	3.3	0.5						
1	Signal	Top	Conductive			1.7	25	14	0.89	51.46	98.67
	Prepreg		IS FR408 ; 2116 ; Rc=56% (1 GHz)	3.7	3.8						
	Prepreg		IS FR408 ; 2116 ; Rc=56% (1 GHz)	3.7	3.8						
2	Plane	GND	Conductive			1.4					
	Core		IS FR408 ; 2-7628 ; Rc=40% (1 GHz)	3.7	14.0						
3	Signal	Inner 3	Conductive			1.4	25	7	0.47	50.78	100.61
	Prepreg		IS FR408 ; 2116 ; Rc=56% (1 GHz)	3.7	3.8						
	Prepreg		IS FR408 ; 2116 ; Rc=56% (1 GHz)	3.7	3.8						
4	Plane	VCC	Conductive			1.4					
	Core		IS FR408 ; 2-7628 ; Rc=40% (1 GHz)	3.7	14.0						
5	Plane	VDD	Conductive			1.4					
	Prepreg		IS FR408 ; 2116 ; Rc=56% (1 GHz)	3.7	3.8						
	Prepreg		IS FR408 ; 2116 ; Rc=56% (1 GHz)	3.7	3.8						
6	Signal	Bottom	Conductive			1.7	25	14	0.89	51.46	98.67
	Soldermask		Dielectric	3.3	0.5						

Figure 3. Signal current flow (red) and return current flow (blue)

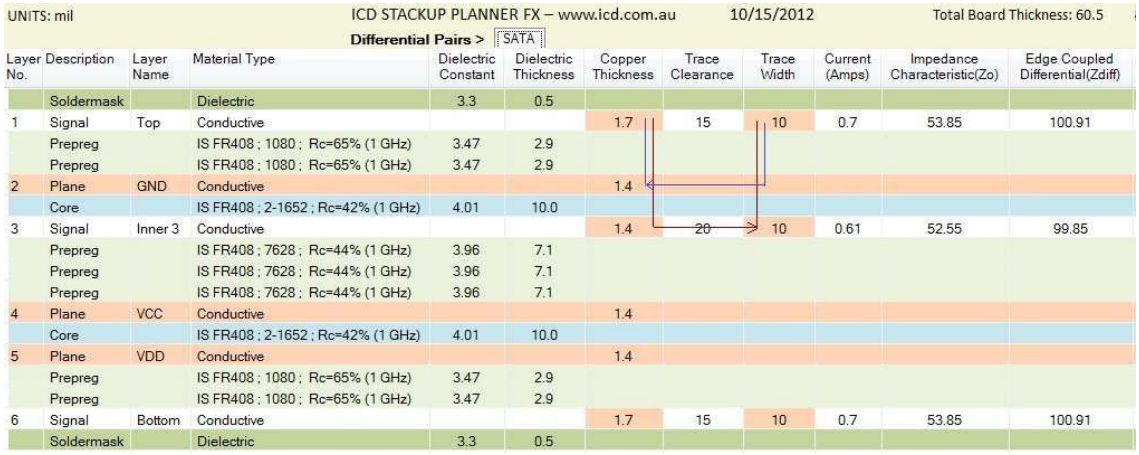
Now, the Designer had good intentions: using the GND plane on layer 2 as the common reference plane. Everything would be fine, until a lack of communication (and understanding of the design parameters) led the Computer Aided Manufacturing (CAM) Engineer, at the fabricator, to change the thickness of the core and prepreg materials to suit the dielectric materials they had in stock.

This is a classic case that we see all the time. It is the point where our design crosses over into the real world – *manufacturing*. It represents a point beyond which many designers rarely dare to venture – due to their lack of understanding of PCB fabrication processes. But, it is a fact that the more awareness we have surrounding the fabrication processes, the better our *designs* become, and the better *Designers* we become.

The CAM professional looks at your board in *purely physical* terms. He, most likely, has no understanding of which signals are critical, and your current return paths. His window to your world consists of layers of dielectric materials, copper foils, PTH vias, and soldermasks. The standard Gerber file format—transferred from layout to fab—is a rather primitive (based on the old X,Y Plotters), but highly-effective format for describing two-dimensional graphical information. It is well suited for representing the two major components of a PCB image: lines and dots. But this is all they are to the CAM Engineer.

The proverbial "Left Shift" in the design process is to put control of the stackup build back into the hands of Engineers and PCB Designers—enabling them to collaborate with, if not control the outcome of the fabrication. To do this, Designers need a comprehensive list of standard dielectric materials from popular manufacturers like Isola, Nelco, Rogers, etc., and the ability to insert these into a prototype stackup, determining the single-ended and differential impedances of these materials combined with PCB layout design rules. The ICD Stackup Planner, shown in Figures 3 and 4, (available for download at www.icd.com.au) handles these tasks quite well, in fact—providing an interface between CAM, signalintegrity simulation, and PCB layout.

Since layer 3 is now closer to the GND plane on layer 2 in Figure 4, it will be used for the current return path, rather than VCC, as before. And, there is no need for ”Plane Jumpers” in this case. This is by far the best scenario. The PCB Designer can pass this information on to fabrication with confidence that his intended stackup build will be manufactured to suit the design’s *electrical* needs.



UNITS: mil — ICD STACKUP PLANNER FX – www.icd.com.au — 10/15/2012 — Total Board Thickness: 60.5

Differential Pairs > SATA

Layer No.	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Impedance Characteristic(Zo)	Edge Coupled Differential(Zdiff)
	Soldermask		Dielectric	3.3	0.5						
1	Signal	Top	Conductive			1.7	15	10	0.7	53.85	100.91
	Prepreg		IS FR408 ; 1080 ; Rc=65% (1 GHz)	3.47	2.9						
	Prepreg		IS FR408 ; 1080 ; Rc=65% (1 GHz)	3.47	2.9						
2	Plane	GND	Conductive			1.4					
	Core		IS FR408 ; 2-1652 ; Rc=42% (1 GHz)	4.01	10.0						
3	Signal	Inner 3	Conductive			1.4	20	10	0.61	52.55	99.85
	Prepreg		IS FR408 ; 7628 ; Rc=44% (1 GHz)	3.96	7.1						
	Prepreg		IS FR408 ; 7628 ; Rc=44% (1 GHz)	3.96	7.1						
	Prepreg		IS FR408 ; 7628 ; Rc=44% (1 GHz)	3.96	7.1						
4	Plane	VCC	Conductive			1.4					
	Core		IS FR408 ; 2-1652 ; Rc=42% (1 GHz)	4.01	10.0						
5	Plane	VDD	Conductive			1.4					
	Prepreg		IS FR408 ; 1080 ; Rc=65% (1 GHz)	3.47	2.9						
	Prepreg		IS FR408 ; 1080 ; Rc=65% (1 GHz)	3.47	2.9						
6	Signal	Bottom	Conductive			1.7	15	10	0.7	53.85	100.91
	Soldermask		Dielectric	3.3	0.5						

Figure 4. The return current path now uses a common GND plane (layer 2)

”Plane Jumpers” can be used to easily resolve a return-current issue, but they are best avoided by taking control of the stackup back into the hands of the Hardware Engineer and PCB Designer, while streamlining communication between the hardware-engineering team and fabrication.

Points to Remember:

- A split in a plane causes an impedance discontinuity in the signal path crossing the split, creating signal reflections, crosstalk, and unwanted common-mode currents that can lead to EMI problems.
- Both ground and power planes (any plane) can be used as a reference plane and return current-return path for a signal.
- It is always better to have only one single reference (ground) plane for a system.
- ”Plane Jumpers” (ceramic decaps) can provide a path for the return current between the two supply planes.
- A “bridge”—provided by an adjacent plane—is best used for control signals to cross a split plane.
- ”Plane Jumpers” (decaps) can be placed close to a via to allow the flow of return current from plane to plane.
- Where there are multiple ground planes, ground-stitching vias should be placed next to each signal-via transition.
- The more knowledge PCB Designers have of the fabrication processes – the better the outcome of our design, and the better Designers we become.
- The ”Left Shift” in the design process is to put control of the stackup back into the hands of Hardware Designer so that electrical design parameters don’t get pushed to the side.

References:

Advanced Design for SMT (two day course) – Barry Olney
Beyond Design: The Dumping Ground – Barry Olney
Intro to Board-Level Simulation and the PCB Design Process– Barry Olney
PCB Design Techniques for DDR, DDR2 & DDR3, Part 1 – Barry Olney
PCB Design Techniques for DDR, DDR2 & DDR3, Part 2 – Barry Olney
Electromagnetic Compatibility Engineering – Henry Ott
High Speed Digital Design – Howard Johnson
The ICD Stackup Planner and PDN Planner can be downloaded from www.icd.com.au

Bio :

Barry Olney is Managing Director of In-Circuit Design Pty Ltd (ICD), Australia. The company developed the ICD Stackup Planner and ICD PDN Planner software, is a PCB Design Service Bureau, and specializes in signal integrity, crosstalk, and timing simulation, as well as EMC analysis.