

BOARD LEVEL SIMULATION SPECIALISTS

ICD Stackup Planner - offers engineers/PCB designers unprecedented simulation speed, ease of use and accuracy at an affordable price

- 2D (BEM) field solver precision
- Characteristic impedance, edge-coupled & broadside-coupled differential impedance
- Unique field solver computation of multiple differential technologies per stackup
- Heads-up impedance plots of signal and dielectric layers
- User defined dielectric materials library - over 16,250 materials up to 100GHz

ICD PDN Planner - analyze multiple power supplies to maintain low impedance over entire frequency range dramatically improving product performance

- Fast AC impedance analysis with plane resonance
- Definition of plane size/shape, dielectric constant & plane separation for each on-board power supply
- Extraction of plane data from the integrated Stackup Planner
- Definition of voltage regulator, bypass/decoupling capacitors, mounting loop inductance
- Frequency range up to 100GHz
- Extensive Capacitor Library – over 5,250 capacitors derived from SPICE models

Plane Crazy, Part 2

by Barry Olney

IN-CIRCUIT DESIGN PTY LTD AUSTRALIA

In my [recent four-part series](#) on stackup planning, I described the best configurations for various stackup requirements. But I did not have the opportunity to delve into the use of planar capacitance to reduce the AC impedance at frequencies above 1GHz, which is the region wherein bypass and decoupling capacitors dramatically lose their impact. In this column, I will flesh out this topic, and consider the effects of plane resonance on the power distribution network (PDN).

Figure 1 illustrates a 12-layer DDR3 board with six routing layers and six plane layers utilizing multiple technologies. This board must accommodate 40/80-ohm single-ended/differential impedance for DDR3, 90-ohm differential USB, and the standard 50/100-ohm digital impedances all on the same substrate. In order to reduce the layer count, it is important that

these different technologies share the same layers. Plus, one needs to manage the return current paths and broadside coupling of the stripline configurations—quite a challenge!

The DDR3 matched delay signals are routed on the internal layers 3 & 4 and 9 & 10, which all use ground (GND) as the reference plane. To eliminate broadside coupling, the data lanes (eight in this case), differential strobes, and masks are routed on layers 3 & 4. And the adjacent traces are routed skewed or orthogonally. The address, control and command signals are routed together with the differential clock on layers 9 & 10. This separates the data lanes and address signals. Since DDR technology utilizes synchronous buses, the signals within the data lanes and within the address bus can be routed closely together, but the eight data lanes should be separated to avoid crosstalk.

UNITS: mil		10/22/2015										Total Board Thickness: 78.2 mil		
Layer No.	Via	Description	Layer Name	Material Type	Differential Pairs >				Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)
					40 DDR3 SE	50 SE	80 DDR3 DIFF	90 USB DIFF						
1	8	Soldermask		PSR-4000 MH LPI (1GHz)	3.6	0.5								
		Signal	Top Layer	Conductive			2.1	4	6	0.56	52.66	80.64		
		Prepreg		370HR; 106; Rc= 73% (2GHz)	3.74	2								
		Prepreg		370HR; 106; Rc= 73% (2GHz)	3.74	2								
2		Plane	GND Plane 1	Conductive			1.4							
		Core		370HR; 1-2116; Rc=47% (2GHz)	4.2	4								
3		Signal	Signal Layer 1	Conductive			1.4	4	4	0.31	53.08	79.65	95.64	
		Prepreg		370HR; 7628; Rc= 50% (2GHz)	4.16	8								
		Prepreg		370HR; 7628; Rc= 50% (2GHz)	4.16	8								
4		Signal	Signal Layer 2	Conductive			1.4	4	4	0.31	53.08	79.65	95.64	
		Core		370HR; 1-2116; Rc=47% (2GHz)	4.2	4								
5		Plane	GND Plane 2	Conductive			1.4							
		Prepreg		370HR; 1080; Rc= 64% (2GHz)	3.89	2.8								
6		Plane	Internal Plane 3	Conductive			1.4							
		Core		370HR; 1-2116; Rc=47% (2GHz)	4.2	4								
7		Plane	Internal Plane 4	Conductive			1.4							
		Prepreg		370HR; 1080; Rc= 64% (2GHz)	3.89	2.8								
8		Plane	GND Plane 5	Conductive			1.4							
		Core		370HR; 1-2116; Rc=47% (2GHz)	4.2	4								
9		Signal	Signal Layer 3	Conductive			1.4	4	4	0.31	53.08	79.65	95.64	
		Prepreg		370HR; 7628; Rc= 50% (2GHz)	4.16	8								
		Prepreg		370HR; 7628; Rc= 50% (2GHz)	4.16	8								
10		Signal	Signal Layer 4	Conductive			1.4	4	4	0.31	53.08	79.65	95.64	
		Core		370HR; 1-2116; Rc=47% (2GHz)	4.2	4								
11		Plane	GND Plane 6	Conductive			1.4							
		Prepreg		370HR; 106; Rc= 73% (2GHz)	3.74	2								
		Prepreg		370HR; 106; Rc= 73% (2GHz)	3.74	2								
12		Signal	Bottom Layer	Conductive			2.1	4	6	0.56	52.66	80.64		
		Soldermask		PSR-4000 MH LPI (1GHz)	3.6	0.5								

Figure 1: A 12-layer DDR3 stackup using Isola 370HR 2GHz material.

PLANE CRAZY, PART 2

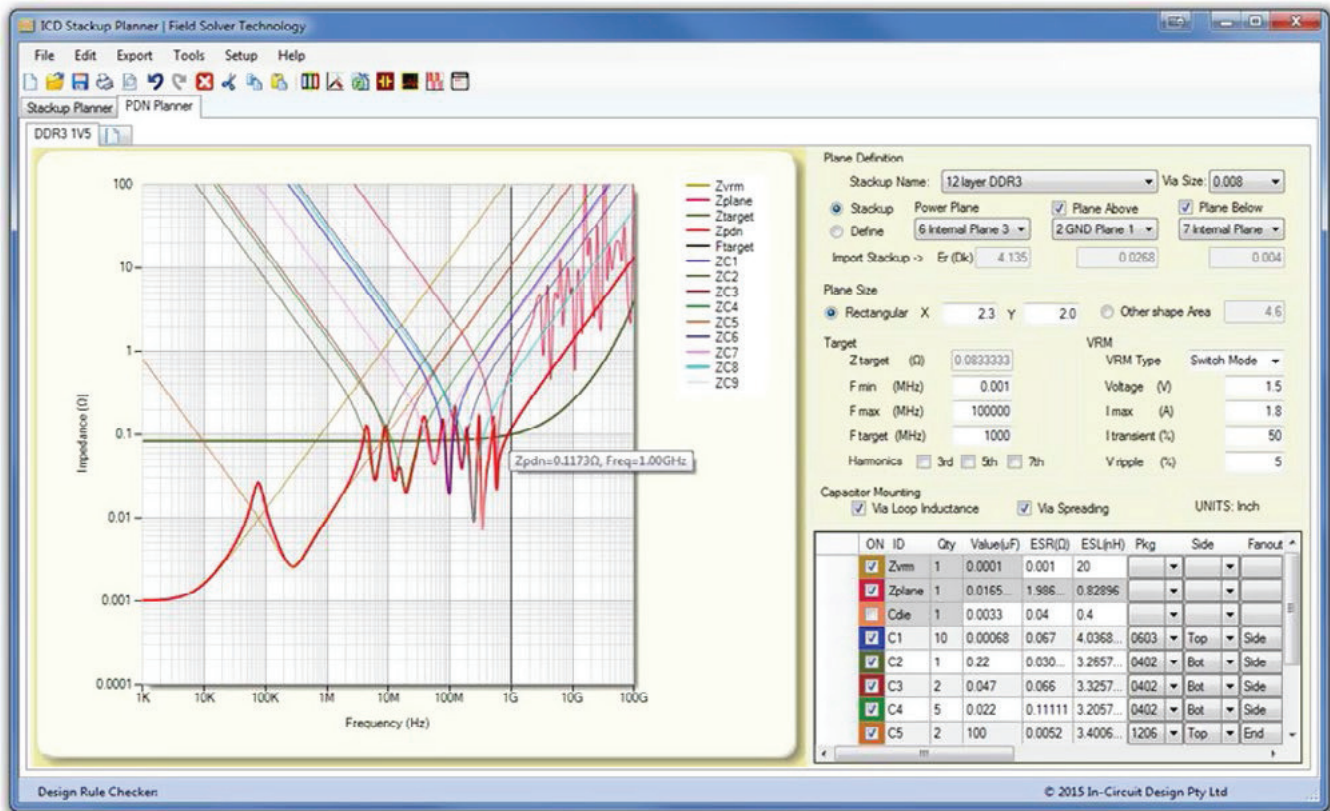


Figure 2: DDR3 PDN with low impedance up to 1GHz.

As you can see, there are four planes in the center of the board, two power and two ground. This is where tight coupling, between adjacent planes, can be utilized to add planar capacitance at low cost and dramatically reduce the AC impedance at the high end. There are thin sheets of Isola 370HR 1080 prepreg (2.8 mils thick) between both planes pairs.

Given the effects of the capacitors equivalent series inductance (ESL) and mounting inductance, the added planar capacitance still reduces the overall impedance to approximately the target impedance up to 1GHz as in Figure 2. Now, this is not easy to do using standard stackups.

With the continuous trend to smaller feature sizes and faster signal rise times, planar capacitor laminate (PCL), also known as embedded capacitor material (ECM), is becoming a cost-effective solution to further improved power integrity. This technology provides an effective approach for decoupling high-performance ICs whilst also reducing electromagnetic interference.

Plane pair cavity resonances contribute to emissions. Smaller plane separation implies less area of equivalent magnetic current at the plane pair edge, or equivalently less local fringing field volume, and therefore lower emissions for a given field strength. However, the smaller the plane separation, the higher the Q of the cavity can be, implying a higher field strength at the plane pair edges.

Embedded capacitance technology allows for a very thin dielectric layer (0.24–2.0 mil) that provides distributive decoupling capacitance and takes the place of conventional discrete decoupling capacitors over 1GHz. Unfortunately, standard decoupling capacitors have little effect over 1GHz and the only way to reduce the AC impedance of the PDN above this frequency is to use ECM or alternatively die capacitance. These ultra-thin laminates replace the conventional power and ground planes and have excellent stability of dielectric constant and dielectric loss up to 15GHz. The thinner layers of ECM, also significantly reduces the ca-

capacitor mounting inductance.

The ZBC-2000™ laminate is constructed using a single ply of either 106 or 6060 style prepreg, yielding a dielectric thickness after lamination of 2 mils when measured by cross sectioning. The ZBC-1000 technology results in a 1 mil dielectric distributed capacitance material. FaradFlex™ and Interra™ buried capacitance products utilize a durable resin system for non-reinforced dielectrics for 1mil thickness and below. This also eliminates the skew associated with the fiber weave effect in standard materials. Also, with a product range up to 20nF per square inch in capacitance density, 3M ECM is the highest capacitance density embedded capacitance material on the market.

These ultra-thin laminates allow a significant layer count reduction in PCBs with better signal performance. Having a low dielectric constant, combined with very high withstanding voltage, these glass-free films change the design rules for via diameter and trace width, while still conforming to the manufacturing needs of the Fab shop. Three traces between vias, at a 0.4 mm pitch, are not only possible but very manufacturable according to Integral Technology.

It is a common belief that solid power and ground planes act as a large, perfect, lumped element capacitor. However, they actually encompass a distributed system of surprising complexity. The distinction between a lumped element and a distributed system involves the relationship between the time delay of the system and the rise-time of the signals.

For instance, for a PCB of six square inches, the signals entrapped between the VCC and

GND planes create a standing wave, resonating as they reflect from side to side, and have a delay time of about 1ns. If the rise time of the signal is 5ns, the lumped condition is satisfied. However, with a much faster rise time or if the DDR3 plane is very small (typically one inch square), then the driver perceives the VCC and GND structure as a distributed object with significant delay.

This delay causes a couple of issues:

1. During the rising and falling edge, only the portion of the planes and decoupling capacitors located within the close vicinity of the driver can react before the edge has vanished. This frequently results in the noise spike being larger than anticipated.

2. The residual PDN noise from the first event reflects like an unterminated transmission line a couple of ns later, back to the driver. If at that precise moment, the driver switches a second time, both pulses (first and second) are superimposed. If the phases add and the driver has a repetitive pulse (as clocks do), the reflected pulse may build significantly.

One could possibly avoid this potential failure by comparing the round-trip delay across the plane, in question, to the clock period. If it is close, then an adjustment in plane size may be an appropriate solution. This may not eliminate all plane resonances but can serve to shift the resonances to other frequencies. Also, adding stitching vias, in appropriate locations, can reduce the extent that signal energy spreads through the plane cavity, and raises the frequency of structural resonances.

Manufacturer	Material	Description	Thickness (mil)
3M	ECM	Embedded Capacitance Material (ECM)	0.24, 0.47, 0.55
DuPont	Interra HK04	Ultra-thin laminate	0.5, 1.0
Integral Technology	Zeta Bond	High Tg Epoxy-Based adhesive film	1.0, 1.5, 2.0
Integral Technology	Zeta Lam SE	Low CTE C-stage dielectric with a Hi Tg	1.0
Integral Technology	Zeta Cap	Hi performance polymer coated copper	1.0
Oak-Matsui Technology	FaradFlex	Planar capacitor	0.31,0.47,0.63,0.94
Sanmina	ZBC1000	Buried Cap, hi-performance decoupling	1.0
Sanmina	ZBC2000	Buried Cap, hi-performance decoupling	2.0

Table 1: Embedded capacitor materials available in the ICD Dielectric Materials library.

PLANE CRAZY, PART 2

The worst-case noise response of a PDN is formed when a long, slow oscillation is followed by a short, fast oscillation. This phenomenon is referred to as a 'rough wave' and in extreme cases can cause total system failure. The long and slow oscillation is the clock and its odd harmonics, while the short and fast oscillation is due to the high-frequency plane resonance peaks. This is similar to an oceanographic 'rogue wave' phenomenon that is formed when a sudden quick wave hits a long, slow wave.

The ICD PDN Planner displays this plane resonance effect in Figure 2 and the projected EMI in Figure 3 (the red line represents the FCC Class B limit). Although the current EMC limits are only defined to 1GHz, one could assume that these will one day be increased to cover the entire bandwidth. The EMI plot represents the projected maximum radiated noise if a high-speed signal excites the plane resonance at a particular frequency.

If the plane size is increased, then the plane

resonance is typically reduced. A combination of modifications to dielectric thickness and dielectric constant of the material in the ICD Stackup Planner, together with an adjustment of plane size, can usually establish the minimum resonance for the configuration. One should also ensure that the resonance peaks do not occur at the odd harmonics (red dotted vertical line), which tend to further radiate.

In conclusion, multiple planes are essential for high-speed design. But, one needs to select the right configuration to manage all of the diverse technologies, return current paths, broadside coupling and multiple power supplies requirements in order to achieve a high-performance, reliable product. Ensuring planes do not resonate, with the clock period, and that slow and fast frequency resonances do not combine will help avoid that dreaded 'rough wave' phenomenon. Power integrity issues generally manifest themselves as intermittent problems, which are otherwise difficult to nail.

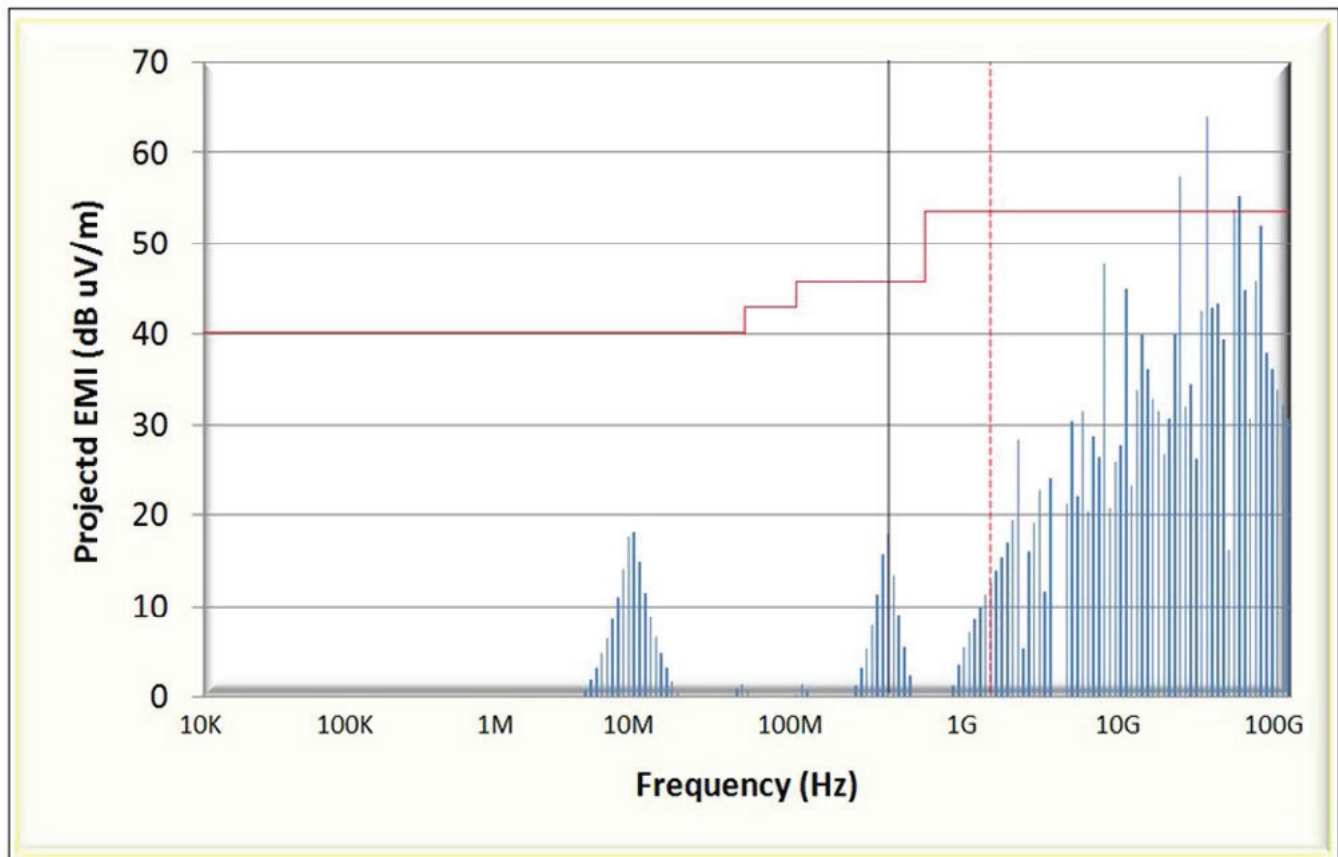


Figure 3: Projected PDN EMI.

PLANE CRAZY, PART 2

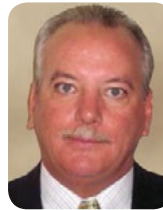
Points to Remember:

- Tight coupling between adjacent planes can be utilized to add planar capacitance and dramatically reduce the AC impedance at the high end.
- Planar capacitor laminate, also known as embedded capacitor material, is becoming a cost-effective solution to further improved power integrity.
- Solid power and ground planes encompass a distributed system of surprising complexity.
- A distributed system involves the relationship between the time delay of the system and the rise-time of the signals.
- During the rising and falling edge, the local planes and decaps cannot react before the edge has vanished. This frequently results in a large noise spike.
- Repetitive pulse clocks tend to superimpose and build significant peaks.
- Avoid potential failure by comparing the round-trip delay across the plane, to the clock period.
- A “rough wave” is formed when a long, slow oscillation is followed by a short and fast oscillation.
- A combination of modifications to dielectric thickness and dielectric constant of

the material in the ICD Stackup Planner, together with an adjustment of plane size, can usually establish the minimum resonance for the configuration. **PCBDESIGN**

References

1. Barry Olney's Beyond Design columns: [No One-Way Trips](#), [The Dumping Ground](#), [Losing a Bit of Memory](#), [Stackup Planning Parts 1-4](#), [Material Selection for SERDES Design](#).
2. Henry Ott: [Electromagnetic Compatibility Engineering](#)
3. Howard Johnson: [High-speed Signal Propagation](#)
4. Masanori Hashimoto and Raj Nair: [Power Integrity for Nanoscale Integrated Systems](#)
5. The ICD Stackup and PDN Planner: www.icd.com.au



Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. This PCB design service bureau specializes in board-level simulation, and has developed the ICD Stackup Planner and ICD PDN Planner software. To read past columns, or to contact Olney, [click here](#).

Spooky Interference at a Distance

Nanotechnologists at the University of Twente research institute MESA+ have discovered a new fundamental property of electrical currents in very small metal circuits. They show how electrons can spread out over the circuit like waves and cause interference effects at places where no electrical current is driven. The geometry of the circuit plays a key role in this so called nonlocal effect. For designers of quantum computers it is an effect to take account of.

Interference is a common phenomenon in nature and occurs when one or more propa-

gating waves interact coherently. Interference of sound, light or water waves is well known, but also the carriers of electrical current—electrons—can interfere. It shows that electrons need to be considered as waves as well, at least in nanoscale circuits at extremely low temperatures.

The researchers have demonstrated electron interference in a gold ring with a diameter of only 500 nanometers. One side of the ring was connected to a miniature wire through which an electrical current can be driven. On the other side, the ring was connected to a wire with a voltmeter attached to it.

Now the researchers have discovered a new way to affect the dynamical nonlocality. Understanding this fundamental effect is important for future quantum information processing.

