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Plane Crazy, Part 1

by Barry Olney

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A high-speed digital power distribution network (PDN) must provide a low inductance, low impedance path between all ICs on the PCB that need to communicate. In order to reduce the inductance, we must also minimize the loop area enclosed by the current flow. Obviously, the most practical way to achieve this is to use power and ground planes in a multilayer stackup. In this two-part column, I will look at the alternatives to planes, why planes are used for high-speed design and the best combination for your application.

Back in the mid-eighties, when I worked at the University of Western Australia, one of my duties was to fix the departmental mainframe: the dreaded DEC PDP-11/40. When it broke down, it was a two-week sentence to solitary

confinement in the frigid computer room. This monster machine had card after card with rows of TTL logic chips. Figure 1 illustrates a typical Unibus board. It had 8K, 16-bit word core memory, which I believe could be expanded to 80K if the need ever arose. The core had a 400ns access time, which means the system clock would have been a blazing 2.5MHz.

I always used the “divide and conquer” methodology. First, eliminate the power supplies then start dividing the system in half, then half again until the fault was localized within a small circuit. But, as it took about half an hour to reboot, with a specific sequence of octal latches, it was a very time consuming process. Plus, there were always numerous engineering students banging on the window, to the terminal room, enquiring when the “mother” might be fixed so they could complete their assignments.

The boards were double-sided and used a power finger, type A or B layout configuration on the top side of the board, as shown in Figure 2. The bottom side could then be used entirely

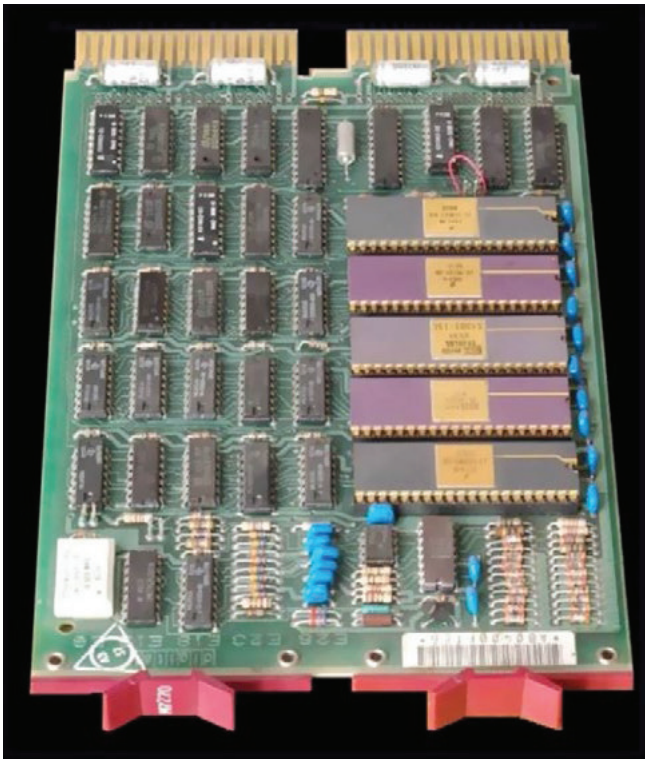


Figure 1: Unibus board (courtesy of DEC).

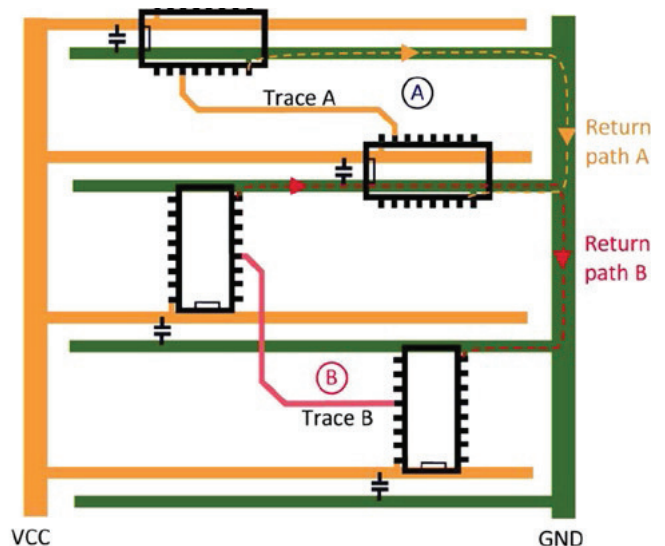


Figure 2: Power finger configuration.

PLANE CRAZY, PART 1

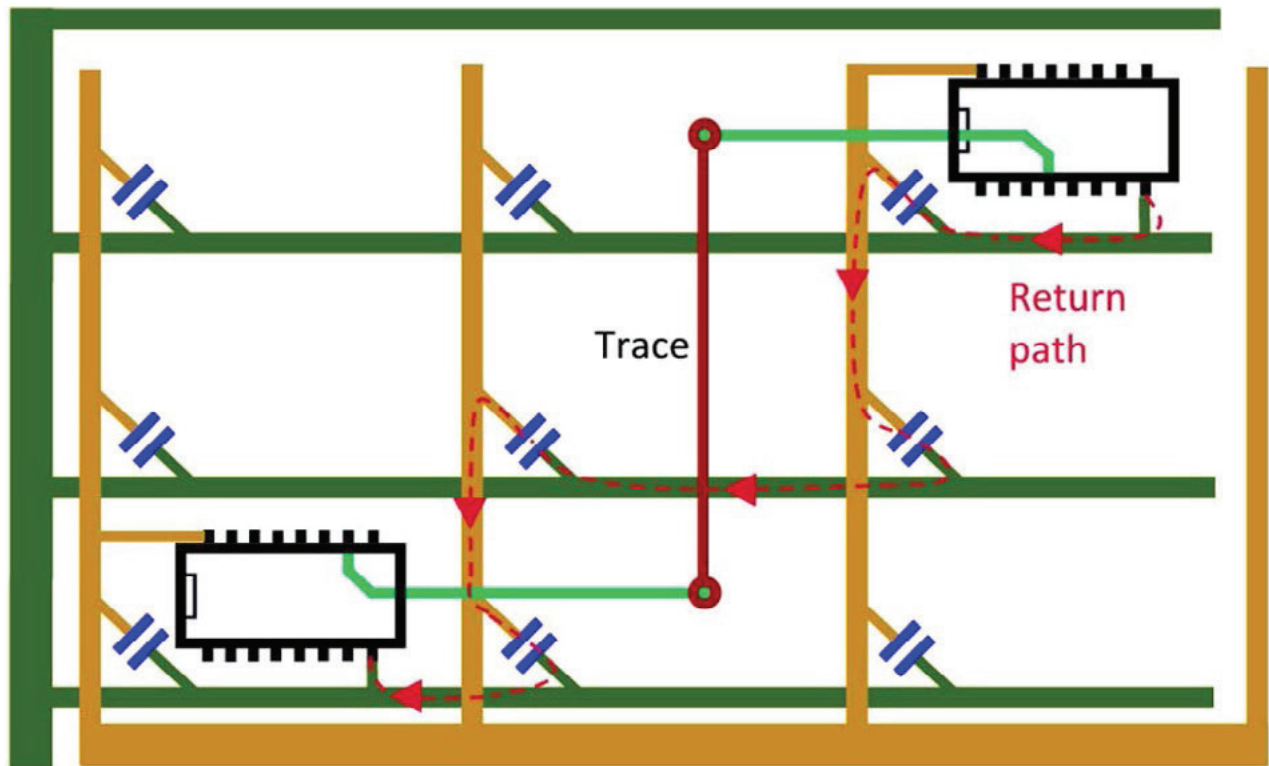
for routing. This provided some mutual inductive coupling between the wide power and ground traces and saved on board area. However, it meant that the return current had to flow all the way around the board perimeter, creating a large loop area. Fortunately, the PDP-11/40 was manufactured way before the era of FCC-mandated radiation guidelines. Needless to say, this is not a good supply configuration for high-speed design. Don't try this at home!

The power and ground grid configuration of Figure 3 also saves on board area, but at the expense of increased mutual inductance. In this case, the ground (GND) traces are horizontal on the bottom of the board, while the power (VCC) traces are vertical on the top side. Connecting the two supplies, at every intersection, with a decoupling capacitor forms a cross-hatch pattern. Current returns equally well, to its source, along either the ground or power traces. The down-side here is that the capacitors used should be of particularly good quality (low ESL)

as the return current must traverse several capacitors to return to the source. If you are limited to a double sided board, then this is the best approach for providing power to the network of chips. But, solid copper planes, in a multilayer configuration, are of course a much, much better solution for high-speed design.

Although it is true that a plane has significantly less inductance than a trace, plane inductance is not negligible. The mechanism by which a plane reduces the inductance is by allowing the current to spread out, effectively creating numerous parallel paths. But at high speeds, return currents flow the path of least inductance which tends to direct the current directly below the signal trace.

Also, due to skin effect, high-frequency currents cannot penetrate a plane, and therefore, all currents in conductors are surface currents. This effect will begin to occur at frequencies above 30 MHz for 1 oz. copper layers in a PCB. Therefore, at high frequencies, a plane in a PCB is really



GND VCC

Figure 3: Power and ground grid configuration.

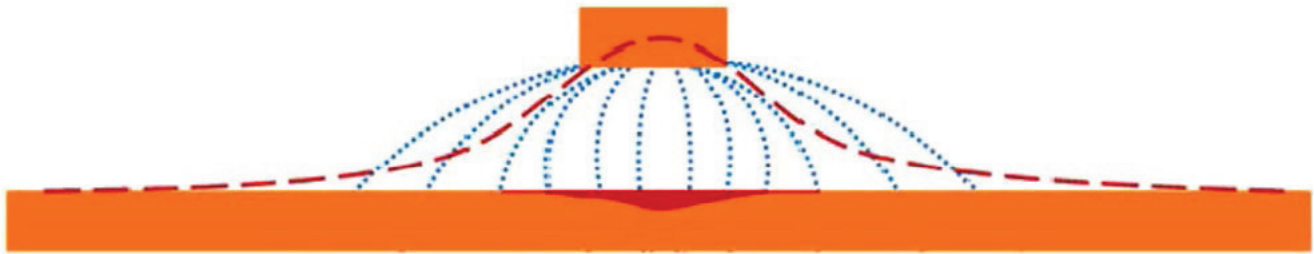


Figure 4: Microstrip plane return current distribution.

two conductors—not one conductor. There will be a current on the top surface of the plane, and there can be a different current or no current at all on the bottom surface of the plane.

Figure 4 illustrates the cross-section on a microstrip (outer layer) trace and its associated plane return current distribution (red). Where the electric fields (blue) are more tightly coupled to the plane—directly below the trace—the return current also exhibits tighter coupling. But where the field spreads out from the trace, the larger loop area, between the signal and the return current path, increases the inductance. Return current tends to couple to the signal conductor and on the same side, of the plane nearest the signal, falling off in intensity, with the square of increased distance. A stripline (inner layer) return current distribution is narrower with the fields more intense above and below the trace.

Any voltage drop across a ground plane will excite cables terminating on the board, which causes them to radiate as dipole or monopole antennae. The amount of current needed to cause the radiation to exceed the FCC Class B emission requirements, in a one meter long antenna, is extremely small—in the vicinity of just a few μA . Therefore, even the smallest ground noise voltage is significant, since it only takes a few mV of potential to produce currents of this magnitude. Power and ground planes reduce the loop area and hence the inductance and the impedance, which in turn reduces the noise.

Although single-sided and double-sided boards have been used successfully in unshielded enclosures at frequencies of 20–25MHz, these cases are the exception rather than the rule. A design of this type, also requires a high level of EMC expertise and thus is time consuming and risky to produce. Above 10MHz, multilayer

PCBs with at least two plane layers should be seriously considered.

Multilayer boards reduce radiated emissions by more than 10 db compared to a double-sided board—all other factors being equal. Embedding signals between the planes also reduces susceptibility to radiation, as well as providing ESD protection. So not only do we prevent noise from being radiated, but we also reduce the possibility of being affected by an external source.

The planes in a high-speed, digital board perform five crucial functions:

1. Allow the routing of controlled impedance transmission lines in both microstrip and stripline configurations.
2. Provide a reference voltage for the exchange of digital signals.
3. Distribute stable power to all logic devices.
4. Control crosstalk between switching signals.
5. Provide a shield for electromagnetic radiation on internal layers.

Next month, I will look at why solid power and ground planes encompass a distributed system of surprising complexity and how we can best use planar capacitance to reduce AC impedance of the PDN.

Points to Remember:

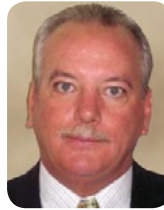
- Inductance may be reduced by minimizing the loop area enclosed by the current flow.
- Double-sided boards, using a power finger layout configuration, should be avoided as they create a large loop area for the return current.

PLANE CRAZY, PART 1

- The power and ground grid configuration is the best approach for providing power delivery on double sided boards.
- Solid copper planes are a much better solution for high-speed design.
- At high speeds, return currents flow the path of least inductance which tends to direct the current directly below the signal trace.
- At high frequencies, a plane in a PCB is really two conductors, not one conductor, due to the skin effect.
- Any voltage drop across a ground plane will excite cables terminating on the board, which causes them to radiate as dipole or monopole antennae.
- Above 10MHz, multilayer PCBs with at least two plane layers should be seriously considered.
- Multilayer boards reduce radiated emission by more than 10 db compared to a double-sided board. **PCBDESIGN**

References

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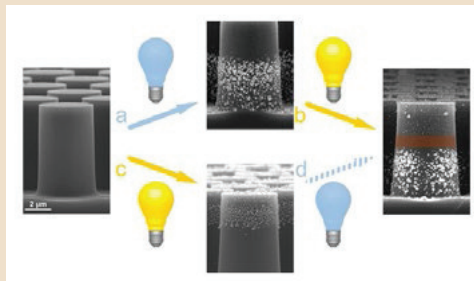


Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. This PCB design service bureau specializes in board-level simulation, and has developed the ICD Stackup Planner and ICD PDN Planner software. To read past columns, or to contact Olney, [click here](#).

University of Twente Develops Versatile Method for Developing New Materials

Researchers at the University of Twente research institute MESA+ have devised an elegant method for fitting various functional coatings to silicon microwires. The research has been published today in the prestigious scientific journal *Advanced Materials*.

Microwires made of the semi-conductor silicon are used in numerous fields. It is generally necessary to 'functionalize' them, by adding a layer of metal or a layer of a catalyst. In most cases, the wires are given a single layer, but in specific instances it is useful to put a different material on the bottom and on the top of the wires. However, creating these wires proved very dif-



ficult and the process of making them involved many steps. Researchers from the University of Twente have now developed a new method that makes creating wires of this kind easy. According to University of Twente Professor Jurriaan Huskens, this has provided chemists with a versatile method for creating new materials.

In their experiments, the University of Twente researchers first made microwires with a PN junction halfway along the wires. In the experiment, the wires were submerged into a solution containing platinum in the dark, causing the 'P side' of the wire to be covered in platinum. In the next stage, silver was added to the other side in the light. The result was a microwire with silver on the top and platinum on the bottom. The wires can be very valuable for the purpose of generating energy from sunlight or purifying water with the help of sunlight.