

# BOARD LEVEL SIMULATION SPECIALISTS

ICD Stackup Planner - offers engineers/PCB designers unprecedented simulation speed, ease of use and accuracy at an affordable price

- 2D (BEM) field solver precision
- Characteristic impedance, edge-coupled & broadside-coupled differential impedance
- Unique field solver computation of multiple differential technologies per stackup
- Heads-up impedance plots of signal and dielectric layers
- User defined dielectric materials library - over 16,250 materials up to 100GHz

ICD PDN Planner - analyze multiple power supplies to maintain low impedance over entire frequency range dramatically improving product performance

- Fast AC impedance analysis with plane resonance
- Definition of plane size/shape, dielectric constant & plane separation for each on-board power supply
- Extraction of plane data from the integrated Stackup Planner
- Definition of voltage regulator, bypass/decoupling capacitors, mounting loop inductance
- Frequency range up to 100GHz
- Extensive Capacitor Library – over 5,250 capacitors derived from SPICE models

# Board-Level Simulation and the Design Process: Plan B — Post Layout Simulation



by **Barry Olney**  
IN-CIRCUIT DESIGN PTY LTD | AUSTRALIA

*Summary — Post-layout simulation covers batch mode simulation, which automatically scans nets on an entire PCB, flagging signal integrity, crosstalk and EMC hot spots. While post-layout simulation can be used for disaster recovery, ideally this process is completed during the design process.*

As with the film *Star Wars*, we are going to start this saga toward the end to see how the Imperial Empire has destroyed our system and then go back to the beginning to step through a methodology that will hopefully save us from this final painful and time-consuming step.

Unfortunately, board-level simulation is engaged too often towards the end of the design cycle. Ideally the simulation should be done during the design process to ensure design integrity. By following this year's series of columns on *Board-Level Simulation and the Design Process*, designers can be up-to-date on the best methodology to follow.

Plan B is basically disaster recovery. If, for instance, on the third iteration your product still does not meet specifications and management is pushing to have the project completed, then you need an alternative plan. However, if

the simulation is done during the design process, these re-spins can be avoided.

First, the post-layout board-level simulation requires the translation of the design files so that they can be read into the simulator. The simulation software interfaces to all major electronic design automation (EDA) PCB design packages. However, when there are issues with the translation of PCB databases, there is always another way via Spectra DSN or another PCB package.

The I/O Buffer Interface Specification (IBIS) models are required for all the major devices. Because IBIS models do not reveal the proprietary internal process or architecture information, semiconductor vendor's support of IBIS continues to grow and these days most models are available for download from the vendor's Web site. The IBIS format has proven to give reliable and accurate board-level simulation information.

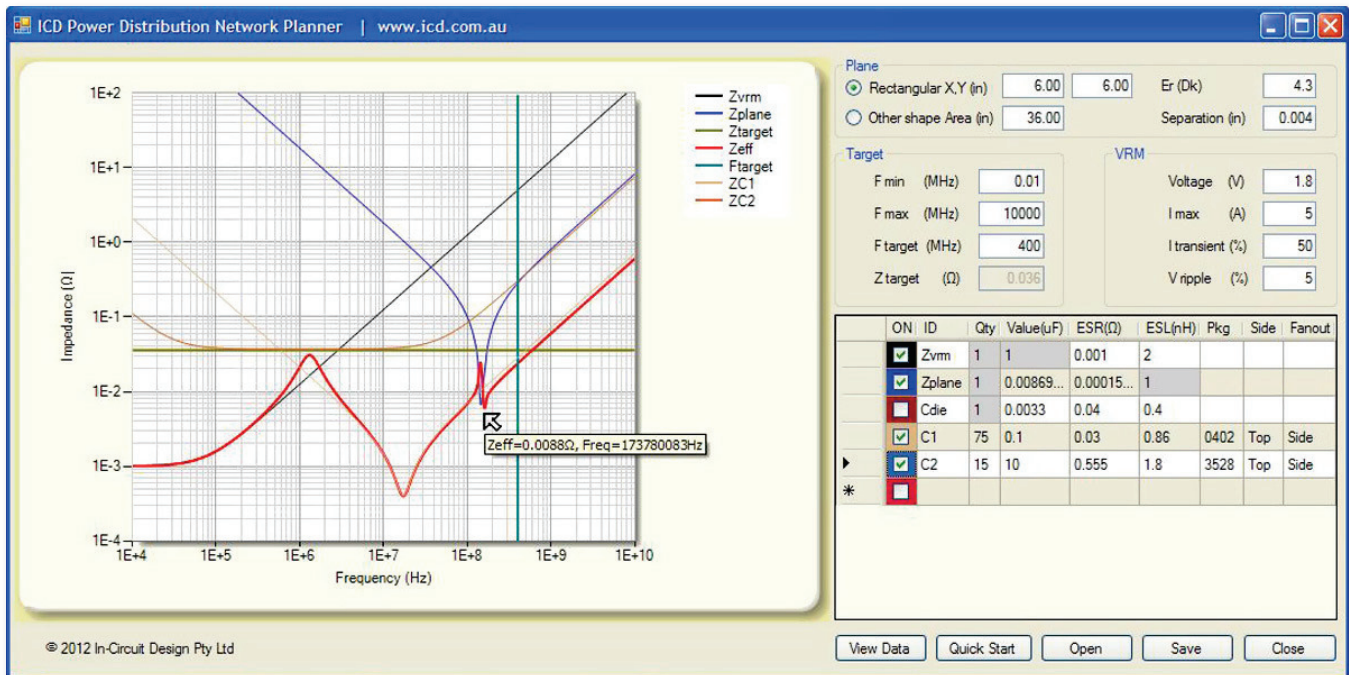
A preliminary batch mode simulation is initially completed on the design. Default IC characteristics, crosstalk of 150mV maximum and EMC to FCC, CISPR Class A and B are set up in the simulator. The batch mode simulation au-

UNITS: MIL ICD STACKUP PLANNER – www.icd.com.au 9/27/2011 Total Board Thickness: 61.2

Layer Number	Layer Name	Material Type	Dielectric		Copper Thickness	Trace		Current (Amps)	Impedance Characteristic(Zo)	Edge Coupled Differential(Zdiff)	Broadside Coupled Differential(Zdbs)	Description
			Constant	Thickness		Clearance	Width					
1	Top	Dielectric	3.3	0.5	1.4	8	4	0.31	53.53	99.99		Soldermask
		Conductive										Signal
2	GND	Dielectric	4.3	3	1.4							Prepreg
		Conductive										Plane
3	Inner 3	Dielectric	4.3	8	1.4							Core
		Conductive				8	4	0.31	62.39	99.59		Signal
		Dielectric		12								Prepreg
4	VCC	Conductive			1.4							Plane
		Dielectric	4.3	4								Core
5	GND	Conductive			1.4							Plane
		Dielectric	4.3	12								Prepreg
6	Inner 6	Conductive			1.4	12	6	0.42	54.11	91.56		Signal
		Dielectric	4.3	8								Core
7	GND	Conductive			1.4							Plane
		Dielectric	4.3	3								Prepreg
8	Bottom	Conductive			1.4	4	4	0.31	53.53	89.98		Signal
		Dielectric	3.3	0.5								Soldermask

**Figure 1:** The perfect stackup for high-speed design.

## PLAN-B — POST LAYOUT SIMULATION *continues*



**Figure 2:** The ICD power distribution network planner illustrates the decoupling scheme.

tomatically scans large numbers of nets on an entire PCB, flagging signal integrity, crosstalk and EMC hot spots.

The post-layout simulation analysis can then be prepared using supplied specifications. This is an extensive interactive board-level simulation which takes the analysis to the next level — simulating trouble spots identified by the batch analysis in order to further resolve the issues with greater accuracy.

As part of the design for manufacturability (DFM) check, the board stackup is analyzed to ensure that both single-ended and differential impedances conform to the technology requirements. For example, USB differential pairs must be 90 ohms and the DDR2 clocks have to be routed to 100 ohms differential impedance; thus, the variables need to be adjusted to achieve this. However, the basic structure of the substrate remains the same — the dielectric thickness, copper thickness, etc.

Figure 1 illustrates the perfect stackup for high-speed design. This is calculated by the ICD Stackup Planner (download from [www.icd.com.au](http://www.icd.com.au)). Good interplane capacitance can be achieved by using 4-MIL plane spacing, in the center, resulting in 241 pF/in<sup>2</sup> capacitance. This

reduces the power distribution network (PDN) impedance at high frequencies. Also, the stack-up should be symmetrical about the center to ensure that the board does not warp during the PCB fabrication or reflow process.

The stackup should be checked for split planes; analog and digital sections should be examined, keeping the current return paths in mind. I generally use route fences to direct routes rather than splitting the planes, which can be disastrous. High-speed signals should not cross over analog areas.

Stitching vias should be used to connect all ground planes to provide a direct return path for signal currents. If the return current needs to cross over from a ground plane to a power plane (which can also be used as a reference plane) then a 100-nF capacitor should be placed next to the signal via, between the planes to provide this path.

Decoupling capacitors (DCAPs) supply instantaneous current (at different frequencies) to the drivers until the power supply can respond. In other words, it takes a finite time for current to flow from the power supply circuit (whether on-board or remote) due to the inductance of the trace and/or leads to the drivers.

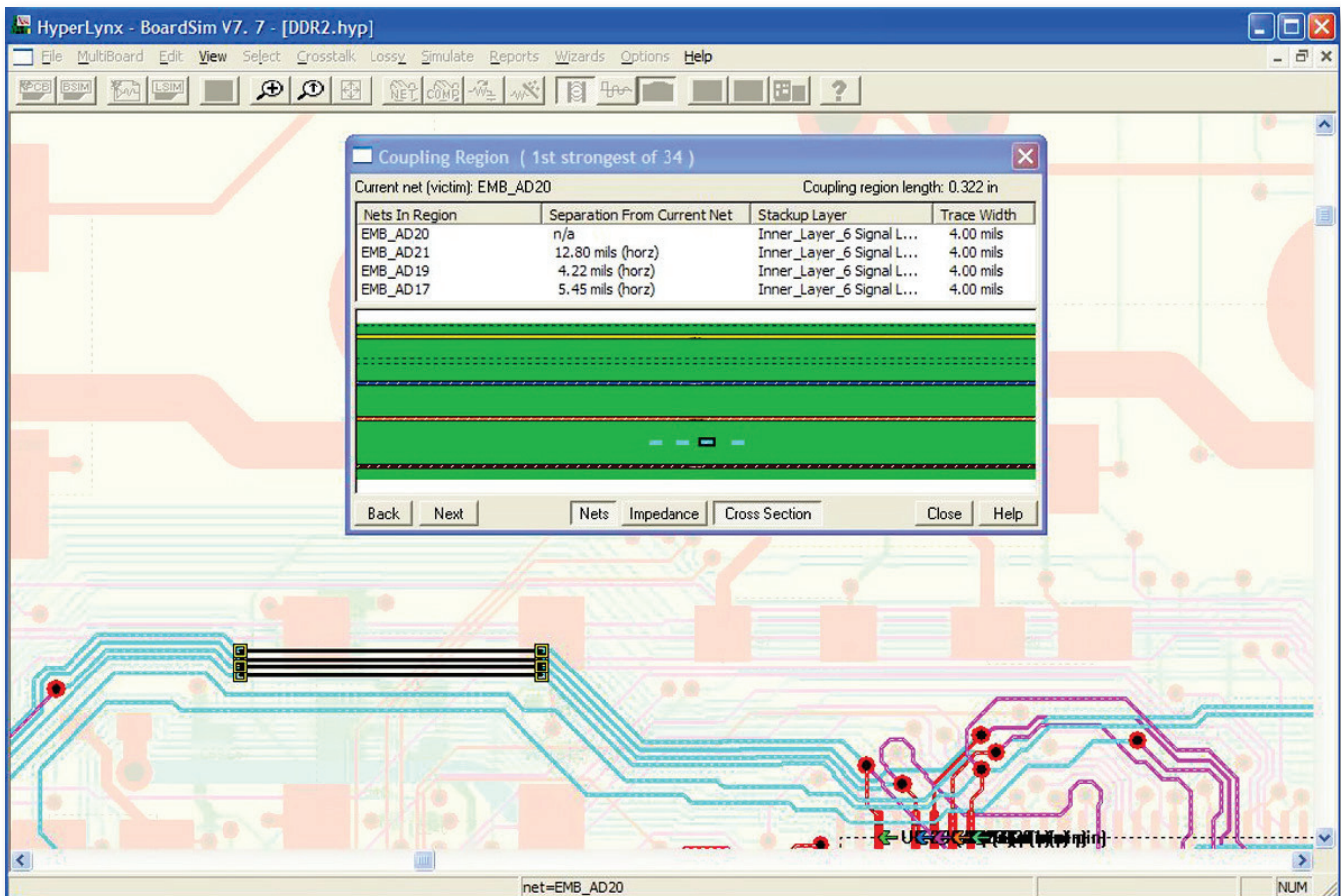
Every decoupling capacitor has a finite series inductance which causes its impedance to increase at high frequencies. In order to reduce this inductance, as much as possible, a number of DCAPs should be placed in parallel, as close as possible to each power pin, using a thick, short trace. For example, if the vias are 20/8 MIL (pad/hole) then a 20-MIL trace should be used on the DCAPs.

The specifications, number and placement of all DCAPs should be reviewed. Figure 2 illustrates how the ICD PDN Planner is used to calculate the value and number of 10uF tantalums and 100-nF ceramic X7R capacitors required to keep the PDN impedance below the target impedance up to 400 MHz. The target impedance is determined by the switch mode voltage regulator characteristics and the allowable voltage ripple. The red line represents the effective impedance.

In this example, there are two anti-resonance peaks. The first, at 1.4 MHz, is formed

by the switched mode voltage regulator module and the 100-nF capacitors suppressed slightly by the tantalums. The second peak is around 173 MHz, which in this case happens to be the resonant frequency of the plane reacting with the 100-nF capacitors. These peaks are associated with the circuit formed after one capacitor (or regulator plane) has gone inductive and another capacitor is still capacitive — the classic parallel LC tank circuit. The most effective way to reduce the height of the anti-resonance is to minimize inductance.

This is, however, a trial-and-error process and you should keep in mind that every different value capacitor added creates another anti-resonance peak. And, even small-value DCAPs do not have much affect above 1 GHz, so in order to minimize the impedance at higher frequencies you may have to reduce the plane-to-plane spacing or use embedded plane capacitance if using high-frequency, fast rise-time devices.



**Figure3:** Crosstalk on long parallel trace segments.

The inductance of the capacitor mounting has not been considered in this example. This inductance will increase the impedance and can be reduced by placing the power and ground planes closer to the capacitor mounting surface which reduces the loop area. The optimum mounting inductance of 0.5 nH is obtained when an 0402 capacitor is mounted using the via-on-side scheme with wide connecting traces to the vias. To further reduce the mounting inductance, two vias per capacitor land can be used in parallel.

As mentioned previously, the batch mode simulation produces a report of possible SI, crosstalk and EMC violations. Interactive simulation is then used to further analyze these potential issues.

**Example:**

Maximum allowed crosstalk: 150 mV pea  
NET = EMB\_AD20

AGGRESSOR NETS (Estimated peak crosstalk)

EMB\_AD17: 175 mV

EMB\_AD21: 65 mV

EMB\_AD19: 102 mV

Sum of the two strongest aggressors: 277mV

Crosstalk is typically picked up on long parallel trace segments. These can be on the same layer, as in Figure 3, but may also be broadside coupled from the adjacent layer. It is for this reason that orthogonal routing is recommended on adjacent layers (between planes) to minimize the coupling area. This will not occur with the stackup illustrated in Figure 1, because there is only one signal layer between the planes — so this is very safe as far as broadside crosstalk is concerned, plus it allows a clear return path for signal current.

When interactive routing, one tends to group signals for aesthetic reasons — this is the artistic side of the PCB designer showing through. But, although it looks nice and neat, it may not perform so well. It is recommended that, in the above case, trace segments should be spaced by three times the trace thickness where possible or alternatively the trace-to-plane height can be reduced in the stackup.

Synchronous buses, as typically used in

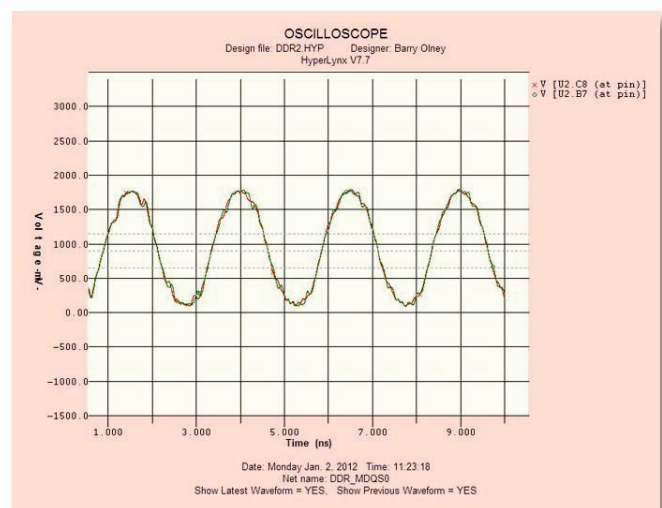
DDR designs, benefit from an extraordinary immunity to crosstalk. Crosstalk only occurs when the signals are being switched and this crosstalk only has an effect within a small window around the moment of the clocking. So, providing the receiver waits sufficiently long enough for the crosstalk to settle before sampling the bus, the crosstalk has no effect on the signal quality at the receiver.

Apart from the issues of EMC, signal integrity and crosstalk problems can cause intermittent operation due to timing glitches and interference dramatically reducing your product's reliability.

Series terminators are typically used in high-speed design to slow the rise time, prevent ringing and hence EMI. These need to be manually checked for correct value or they can be determined by the simulator:

$$\text{transmission line impedance} - \text{driver impedance} = \text{series terminator (ohms)}$$

Flight times of the critical signals are then examined. One could compare the matched lengths of each signal, but delay will vary depending on the meander pattern. Also, the trace either side of a series terminator needs to be added to obtain the total length. Instead, it is best to compare the skew between, for example in Figure 4, the DDR2 MDQ0 (data) and MDQS0 (strobe) to ensure the flight times are correct. In



**Figure 4:** Flight times of DDR2 MDQ0 compared to MDQS0.

## PLAN-B — POST LAYOUT SIMULATION *continues*

this case there is 10pS difference, well within the specification.

Also, firmware can be used to adjust the drive strength in most FPGAs. I typically use the mid-strength drive current (8 - 12 mA) unless there are multiple loads in which case a high drive current may be required. High drive strength normally distorts the waveforms. If this occurs, back it off a little and check the waveforms again.

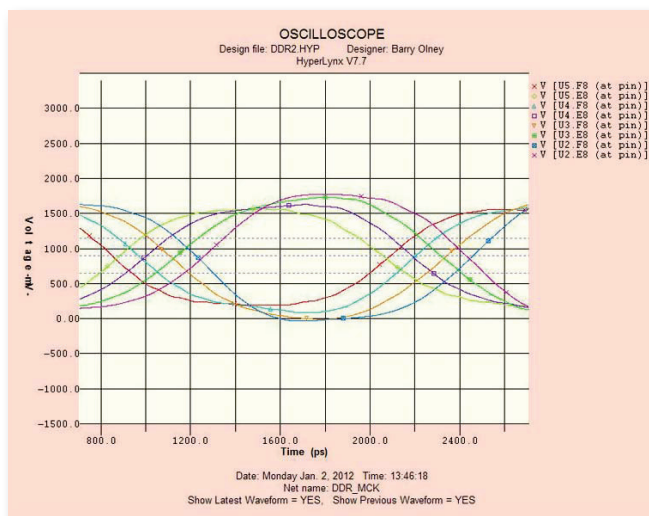
The signal groups to compare for DDR2 devices are:

Data: MDQ, MDQS & MDM  
Address: MA, MBA, MRAS, MCAS, MWE  
Control: MCS, MCLKE, MODT  
Clock: MCLK, MCLK#

The DDR2 signals should be referenced to the VDD (1.8V) power plane or ground plane. The clock is used to capture the address and command data whilst the data is captured by the strobes rather than the clock. Therefore, the signals in the groups above should be compared to each other. For example: MDQ0 compared to MDQS0 and MDM.

The timing of the differential clocks should also be checked and the eye needs to be wide open. Figure 5 shows the DDR2 clock signal at the pins of each memory chip.

Since all products must comply with strict electromagnetic compliancy regulations, all



**Figure 5:** The differential clock at each of the DDR2 chips and the 100-ohm end terminator.

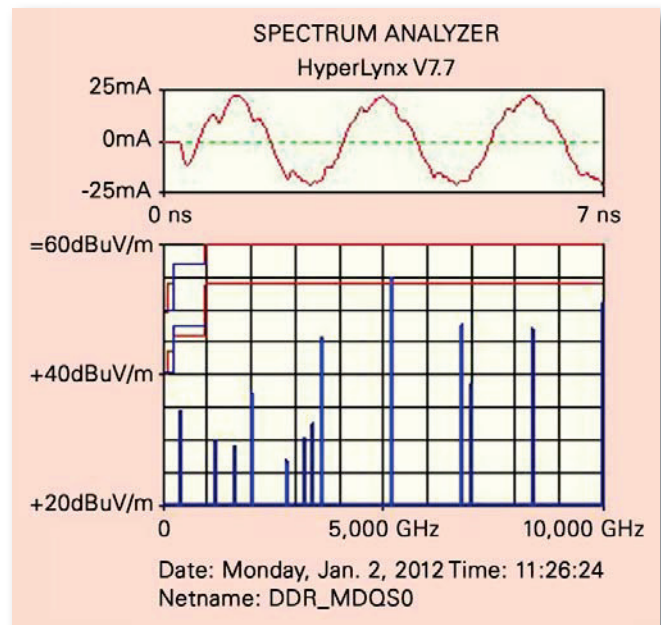
critical high-speed signals should be simulated to determine the amount of expected radiation. The EMC standards, for Class B, limit the radiation to 54 dB average with a peak of 74 dB (at a 3 m distance) above 1 GHz. However, harmonics can still cause unforeseeable problems. Generally these issues are caused by routing traces on the outer (microstrip) layers where radiation is much higher than that of the inner (stripline) layers. Routing these signals between the planes can reduce the EMI by more than 10 dB.

The FCC (US Standard) is the blue horizontal lines  
The CISPR (Euro standard) is the red horizontal lines  
The Class B limit is the lowest pair of lines.

In this case, the radiation for a DDR2 clock of 400MHz is:

34.54 dB @ 380.95 MHz (fundamental)  
29.9 dB @ 1.19 GHz (3<sup>rd</sup> harmonic)  
37.29 dB @ 2 GHz (5<sup>th</sup> harmonic)  
54.95 dB @ 5.19 GHz  
51.23 dB @ 10 GHz

If the maximum clock frequency is 108 – 500 MHz, then emissions have to be measured between 30 MHz – 2 GHz. For a 500 MHz – 1 GHz clock, the measurement is between 30



**Figure 6:** Electromagnetic radiation from MDQS0 strobe.

MHz – 5 GHz. The radiation in Figure 6, up to 2 GHz, is well below the Class B limit; however, we need to ensure that the anti-resonance peaks of the PDN are not at the frequencies of the odd harmonics. A large noise voltage spike can result on the power rail if there is a high transient current at these peaks.

On completion of the interactive simulation, an extensive post-layout simulation report is then compiled highlighting all the issues that need to be addressed by the engineer and/or designer. Once modified, the board is then re-simulated to ensure integrity.

We all know that simulation tools are expensive. Then there is the learning curve associated with complex software, not to mention the fact that the engineer needs to have years of experience analyzing high-speed designs.

By utilizing a PCB board-level simulation service, you can be assured that your PCB will be reliable and manufacturable, will conform to specifications and pass the relevant compliancy tests, which will save you time, money and frustration for a fraction of the cost of board iterations and multiple compliancy testing. Plus, the simulation can be done before the design is finalized (before Gerber output or even earlier in the design process, as recommended) to further reduce production time and costs.

**Points to Remember:**

1. Ensure that both single-ended and differential impedances conform to the technology requirements. Adjust the stackup if required.
2. The stackup should be symmetrical about the center.
3. Stitching vias should be used to connect ground planes or DCAPs between power and ground planes to provide return current paths.
4. DCAPs should be placed in parallel, as close as possible to each power pin using a thick, short trace.
5. The impedance of the PDN should be kept to a minimum (target impedance) up to the target frequency.
6. The inductance of the capacitor mounting can be reduced by taking the via fanout to the side of the land pattern.
7. Crosstalk is typically picked up on long parallel trace segments. Traces should be spaced

by three times the trace thickness where possible.

8. Series terminators should be used on critical signals and need to be checked for correct value.

9. Flight times of the critical signals should be within specification. This may be different for matched lengths. Check data to strobes and address/command to clocks.

10. Make sure that the anti-resonance peaks of the PDN are not at the odd harmonic frequencies of the clock.

11. Ideally, the board-level simulation should be done during the design process to ensure design integrity.

12. The post-layout board-level simulation can be used for disaster recovery: Plan B.

Stay tuned for Part 1 of the new series, Board-Level Simulation and the Design Process. Now that we have seen what happens when you don't follow a proven design process, I will walk you through the entire methodology to get it right the first time. **PCB**

**References:**

1. Advanced Design for SMT — Barry Olney
2. PCB Design Techniques for DDR, DDR2 & DDR3 — Barry Olney
3. Design for EMC — Barry Olney
4. Embedded Signal Routing — Barry Olney
5. Differential Pair Routing — Barry Olney
6. The Perfect Stackup — Barry Olney
7. Controlling the Beast — Barry Olney
8. High-Speed Signal Propagation — H. Johnson

The ICD Stackup Planner and the new ICD PDN Planner can be downloaded from [www.icd.com.au](http://www.icd.com.au)



Barry Olney is Managing Director of In-Circuit Design Pty Ltd. (ICD), Australia, a PCB Design Service Bureau and Board Level Simulation Specialist. Among others through the years, ICD was awarded "Top 2005 Asian Distributor Marketing" and "Top 2005 Worldwide Distributor Marketing" by Mentor Graphics, Board System Division. For more information, contact Barry Olney at +61 4123 14441 or email at [b.olney@icd.com.au](mailto:b.olney@icd.com.au).