PDN Trends and Challenges

Beyond Design

by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

Power distribution network (PDN) planning is a relatively new technology that has become an essential, interrelated component of signal integrity analysis. However, mainstream PCB developers have yet to adopt PDN analysis as a common design process. But, now that the technology is proven and the uptake costs have decreased dramatically, there is no reason why all designers should not take advantage of the technology to improve the reliability and performance of their products. In this month's column, I will delve into the latest PDN trends and challenges.

Today's high-performance processors employ low DC voltages with high transient currents and high clock frequencies to minimize the power consumption and hence the amount of heat dissipated. Unfortunately, the lower core voltages, higher currents and faster edge rates all impact the PDN design as well as signal integrity. The goal of robust PDN planning is to design a stable power source, tak-

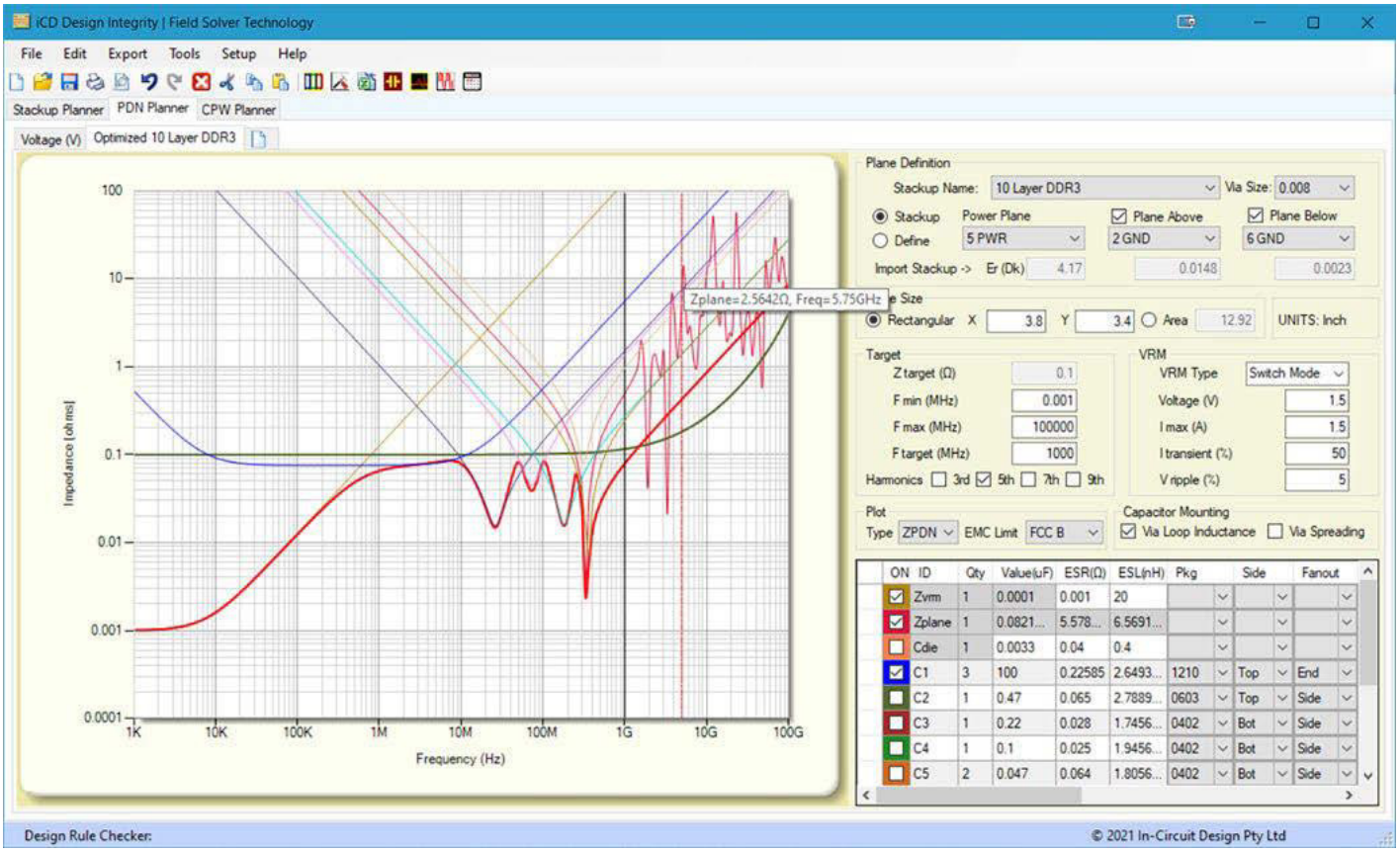

Figure 1: AC impedance profile of a DDR3 supply. (Source: iCD PDN Planner)

ing the above into account, for all the required onboard power supplies. And this all takes up valuable real estate—in some cases, up to 30% of the board surface area. One solution is to combine up to eight DC-to-DC converters in the same IC package. The resultant IC has one power input and outputs eight power rails. This approach reduces the overall PDN size by allowing the use of small 0201 capacitors combined with an integrated multi DC-to-DC converter.

Taking this strategy further creates a new challenge. As we move toward complete systems in a package (SiP) components with more functionality, even more power inputs are required. The SiP package itself may require up to 12 individual sources to power the increased functionality. Then, each supply requires discrete filtering components.

The trend in lower DC voltages also requires tighter voltage noise tolerances and higher currents. Market demands are forcing product designers to create PDNs with greater density, higher power efficiencies, and lower costs, making the process even more challenging.

The target impedance approach to analyzing the PDN is the combination of the worst-case transient current and the voltage noise specification, which act together to set the maximum allowable AC impedance with assured performance. But, as current demands increase and voltage noise fluctuation tolerances reduce, we must lower the AC impedance even further with higher density capacitance. This shift requires the use of more expensive, tighter-tolerance parts, such as capacitors capable of surviving higher currents—creating more heat in a reduced space.

In practice, accurately calculating the transient currents and the precise requirements for the target impedance can be difficult. Since we typically do not know the transient noise current excitation very accurately, it is customary instead to design the PDN to meet the required AC impedance profile. Also, it seems that the current portion of the target impedance equation varies from point-to-point, on the board, depending on a host of intricate relationships. One must always apply engineering judgment in translating the information available into the requirements for a cost-effective PDN design.

With the continuous trend to smaller feature sizes and faster signal rise times, planar capacitor laminate or embedded capacitor materials (ECMs) are becoming a cost-effective solution to further improve power integrity. This technology provides an effective approach for decoupling high-performance ICs whilst also reducing electromagnetic interference.

Plane pair cavity resonances contribute to emissions. Smaller plane separation implies less area of equivalent magnetic current at the plane pair edge, or equivalently less local fringing field volume, and therefore lower emissions for a given field strength.

Embedded capacitance technology comprises a very thin dielectric layer (0.24 – 2.0 mil) that provides distributive decoupling capacitance and takes the place of conventional discrete decoupling capacitors over 1 GHz. These ultra-thin laminates replace the conventional

Manufacturer	Material	Description	Thickness (mil)
3M	ECM	Embedded Capacitance Material (ECM)	0.24, 0.47, 0.55
DuPont	Interra HK04	Ultra-thin laminate	0.5, 1.0
Integral Technology	Zeta Bond	High Tg Epoxy Based adhesive film	1.0, 1.5, 2.0
Integral Technology	Zeta Lam SE	Low CTE C-stage dielectric with a Hi Tg	1.0
Integral Technology	Zeta Cap	Hi performance polymer coated copper	1.0
Oak-Matsui Technology	FaradFlex	Planar capacitor	0.31,0.47,0.63,0.94
Samina	ZBC1000	Buried Cap, hi-performance decoupling	1.0
Samina	ZBC2000	Buried Cap, hi-performance decoupling	2.0

Table 1: Embedded capacitor materials available in the ICD Dielectric Materials Library.

power and ground planes and have excellent stability of dielectric constant and dielectric loss up to 15 GHz. The thinner layers of ECM also significantly reduce the capacitor mounting inductance.

These ultra-thin laminates allow a significant layer count reduction in PCBs with better signal performance. Having a low dielectric constant, combined with very high withstanding voltage, these glass-free films change the design rules for a given via diameter and trace width, while still conforming to the manufacturing needs of the PCB fabricator.

Several technology trends are also enabling denser PDN design. For instance, increasing the converter switching frequency reduces the size of the PDN but is less efficient—producing more heat. Also, decoupling capacitors are tending to be smaller so they can be placed in closer proximity to the load and minimize the parasitic loop inductance. But, this means they need to be of higher quality to withstand the heat. These capacitors have low equivalent series resistance and inductance and take less mounting space which results in lower overall loop inductance.

When you cannot shrink the traditional PDN any further, it may be time to take a new approach involving switched tank converters. Traditionally, we use switched capacitor converters to step down the source voltage, however these require large banks of capacitors. Switched tank converters use resonant tanks which require much less space, so it is possible to put the power delivery devices much closer to the processor core. This enables faster power switching to accommodate changes in consumption of the core.

One of the best ways to lower design costs is to minimize respins of the board. Simulation is the key to resolving trade-offs. And, simulation allows the designer to perform what-if analysis of the PDN before the board assembly is produced. The AC impedance curve is a summation of all of the effects of the power source that you choose: bulk bypass capacitors, high-frequency decoupling capacitors, mounting inductance, the PCB substrate stackup, and the IC package. So it is imperative to be able to extract the plane data from the stackup and import the information into the PDN profile (Figure 2). This allows one

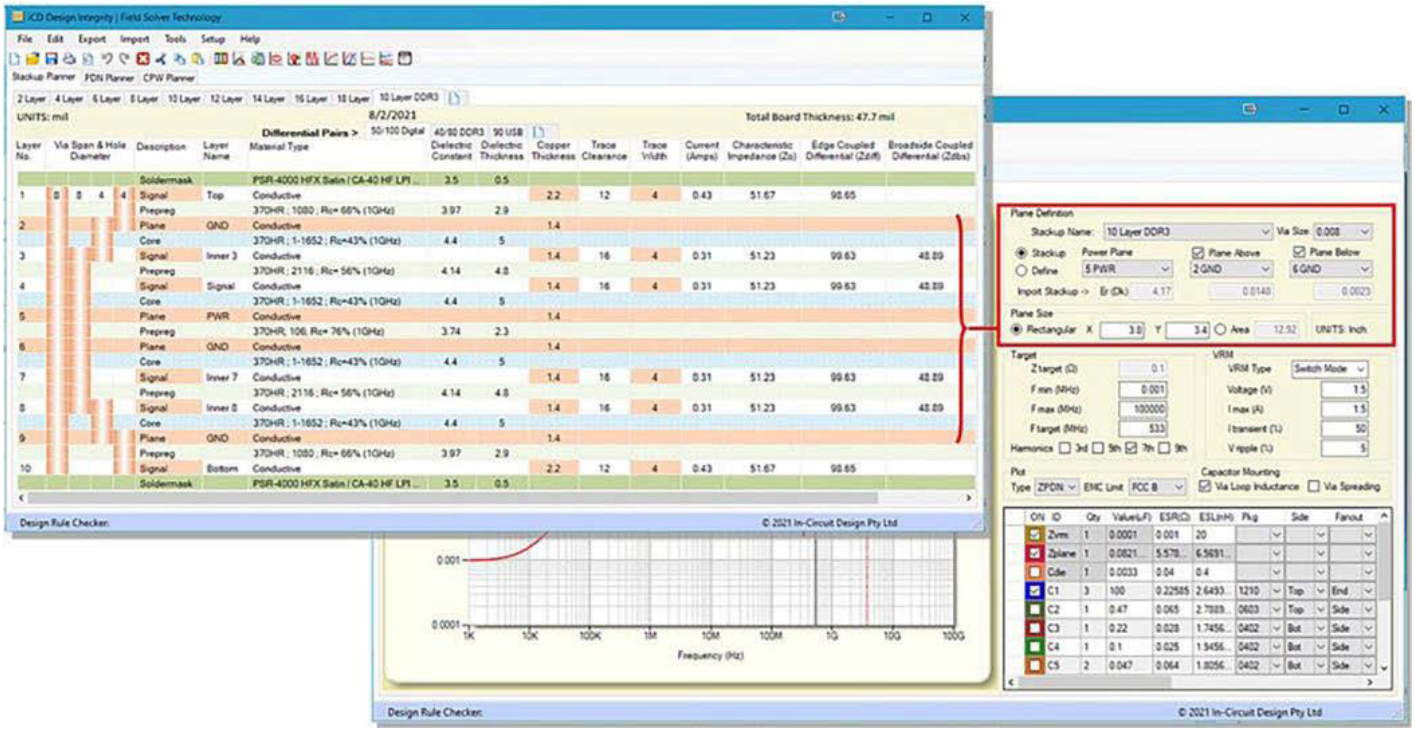

Figure 2: Plane data is extracted from the stackup to build the plane definition of the PDN. (Source: iCD Design Integrity)

to use planar capacitance during the analysis. Planar capacitance is important as it dramatically reduces inductance at frequencies where decaps are out-of-range.

Capacitor manufacturers are now mainly providing capacitor profiles in the form of S-parameter (S_{11}) data which makes analysis more difficult. Gone are the days when you could look at the V-curves from the capacitor ESL, ESR, and value. S-parameter data can be imported into the iCD PDN Planner to model the combination of decaps, planar capacitance, and mounting inductance.

PDN issues impact the project schedule. By incorporating PDN simulation into your design process you can avoid the likelihood of a costly respin and a delay in the schedule. PDN Planners are now very affordable and so there is no reason why every product designer should not have access to the simulation tool.

Key Points

- PDN analysis is now a proven technology that should be adopted by mainstream developers.
- The goal of robust PDN planning is to design a stable power source for all the required onboard power supplies.
- One solution to reduce the PDN size is to combine up to eight DC-to-DC converters in the same IC package.
- The trend in lower DC voltages also requires tighter voltage noise tolerances and higher currents.
- The target impedance approach to analyzing the PDN is the combination of the worst-case transient current and the voltage noise specification, which act together to set the maximum allowable AC impedance with assured performance.
- As current demands increase and voltage noise fluctuation tolerances reduce, we must lower the AC impedance even further with higher density capacitance.
- Planar capacitor laminate or embedded capacitor materials are becoming a cost-effective solution to further improved power integrity.
- Embedded capacitance technology provides distributive decoupling capacitance and takes the place of conventional discrete decoupling capacitors over 1 GHz.
- Ultra-thin laminates allow a significant layer count reduction in PCBs with better signal performance.
- Increasing the converter switching frequency reduces the size of the PDN but is less efficient—producing more heat.
- Switched tank converters create resonant tanks which require much less space than traditional switched capacitor converters.
- Simulation is the key to resolving trade-offs. And, simulation allows the designer to perform what-if analysis of the PDN before the board assembly is produced.
- It is imperative to be able to extract the plane data from the stackup and import the information into the PDN profile. This allows one to use planar capacitance during the analysis.
- Capacitor manufacturers are now mainly providing capacitor profiles in the form of S-parameter (S_{11}) data. **DESIGN007**

Resources

1. Beyond Design: Learning the Curve, Plane Crazy Part 1 and Part 2, The Target Impedance Approach to PDN Design, Impact of PDN Impedance on EMI, by Barry Olney.

2. KEMET and Mouser Electronics: 7 Experts on New Approaches for Power Distribution Network Design - Mighty Guides

Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded at www.icd.com.au. To read past columns or contact Olney, click here.

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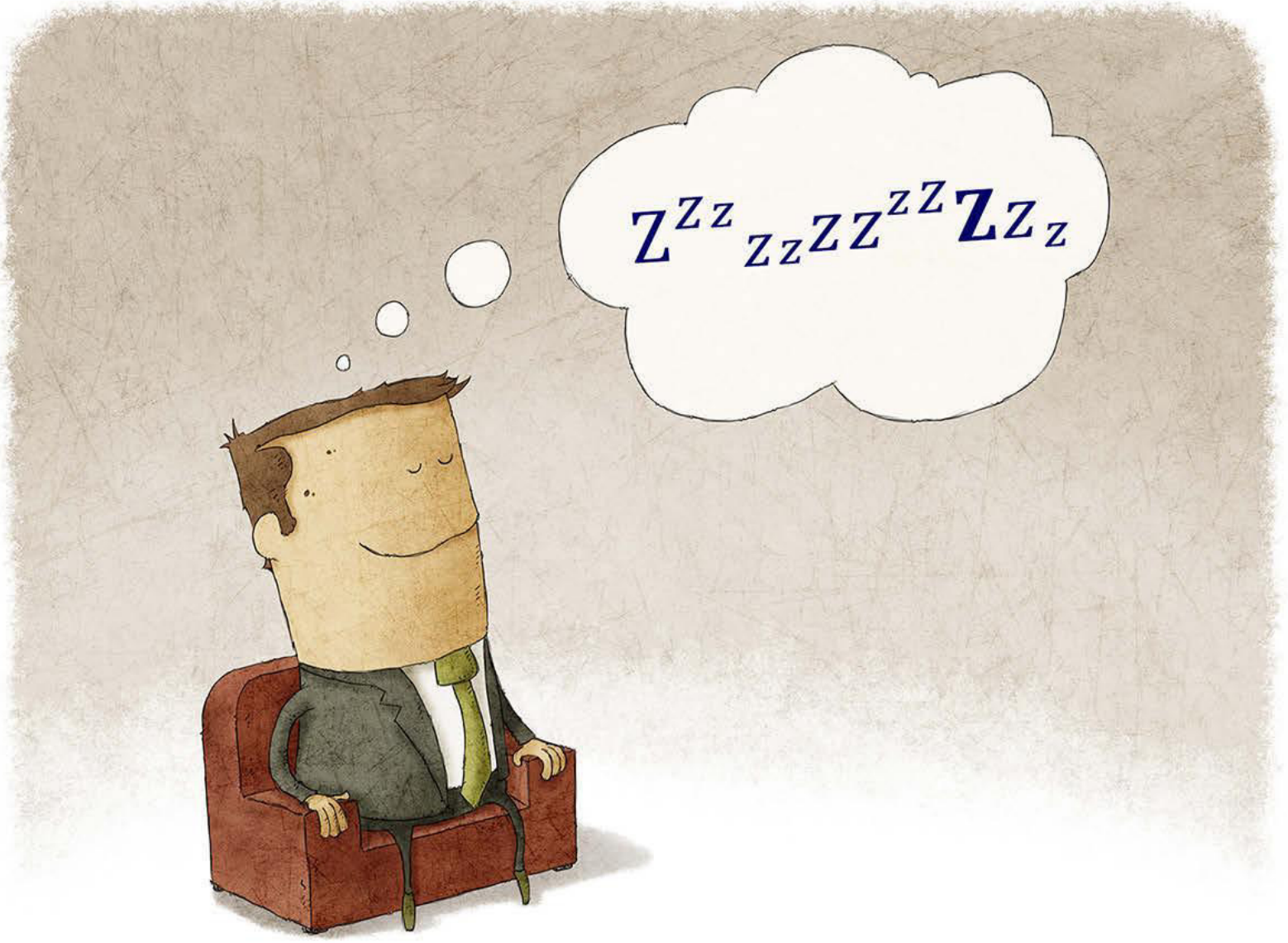

Did you know that two seemingly unrelated concepts are the foundation of a product's performance and reliability?

- Transmission line impedance and
- Power Distribution Network impedance

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