PDN Planning and Capacitor Selection – Part 2

by Barry Olney | In-Circuit Design Pty Ltd |Australia

In last month's column, PDN Planning and Capacitor Selection Part 1, we looked closely at how to choose the right capacitor to lower the AC impedance of the Power Distribution Network (PDN) at a particular frequency. We also examined capacitor properties and types of capacitors that are readily available and touched on the target frequency approach for analyzing a PDN. This month we will continue on from there looking at the one capacitor value per decade and optimized value approaches.

Figure 4 shows the affect of using the one value per decade approach where capacitors, from each decade, are added in parallel. Now to be fair, I have added three of each value from 100uF to 1pF to total 27 capacitors as the target frequency approach, in Figure 2, had a total of 29 capacitors. In this case, the impedance is below the target impedance from 10KHz to 110MHz.

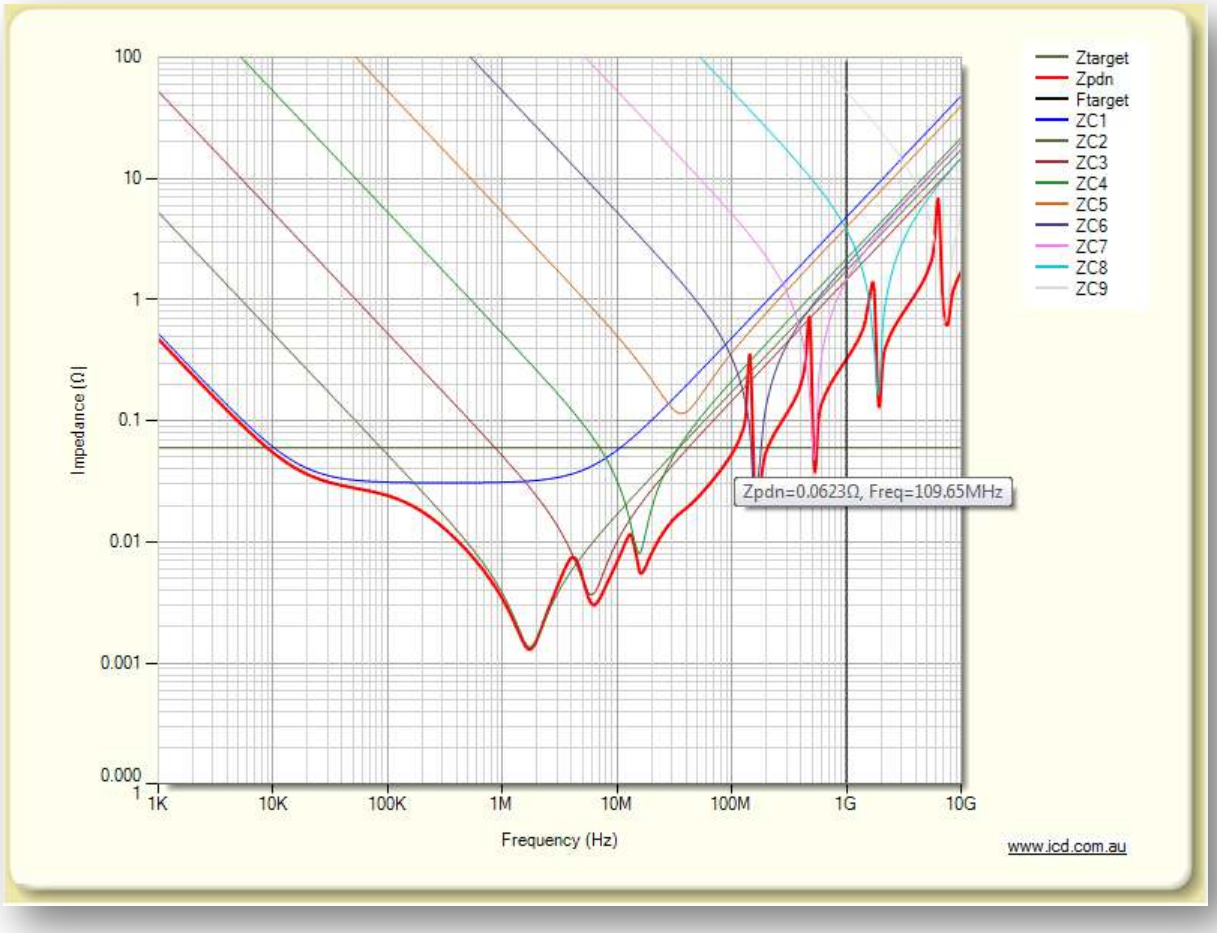

Figure 4 – One value capacitor per decade approach

Notice how the combination of capacitors causes anti-resonant (parallel resonant) peaks where the higher frequency capacitor goes capacitive while the lower frequency capacitor is inductive. This occurs as the LC network produced by the combination is effectively a tank circuit that has parallel resonance at the crossing frequency. This happens each time a different value of capacitor is added. These peaks exceed the 60mΩ impedance of the V shape of the target frequency approach – some as high as 800mΩ below 1GHz which is 13 times higher than the target impedance. If an odd harmonic

was to fall on that particular frequency, then emissions would also be very high at that frequency. From extensive simulations, I have noticed that there is a direct correlation between AC impedance peaks and electromagnetic radiation. In fact, if a board fails electromagnetic compliancy, emissions can be dampened by changing the capacitors to ones that have a Self Resonant Frequency (SRF) close to the radiating frequency.

The optimized value approach, illustrated in Figure 5, has 21 capacitors of different values and numbers to optimize the overall AC impedance. In this case, 21 capacitors from 10uF to 4.7nF are used. This approach gives a response below the target impedance from 2MHz to 158MHz. The low end is of little consequence, as the operating frequency of concern is much higher. And you will also note, that there are no anti-resonant peaks, in this case, because the values are so close together the overlaps dampen the peaks. When the SRFs are spread, the parallel resonant impedance sets the limits to the PDN performance. There are a few ways to reduce the anti-resonant peaks:

1. Adjust the capacitor values so that the SRFs are closer to the anti-resonate peaks
2. Add a capacitor with a SRF at the anti-resonant peak.
3. Add more ESR by increasing the number of capacitors.
4. Increase the capacitance of the planes by using thinner plane to plane dielectrics.

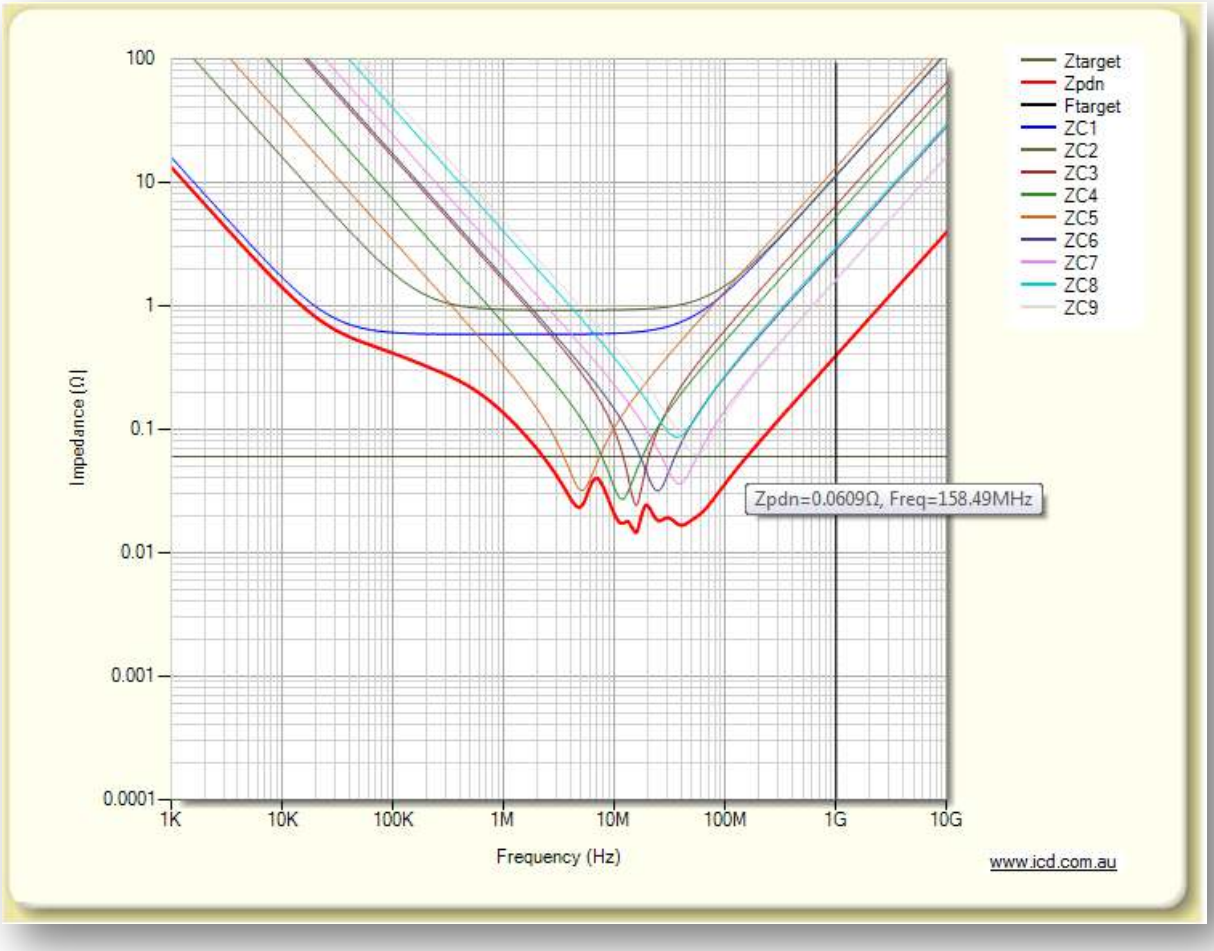

Figure 5 – the optimized value approach with 21 capacitors

The resonant and anti-resonant peaks of the bypass and decoupling capacitors have now been taken into account but we also need to deal with the plane resonance. Ideally the planes, a perfect lumped

element capacitor of this size, should provide a very low impedance between power and ground at very high frequencies (several hundred MHz and higher). But planes, left open at the edges, behave like wide un-terminated traces, from a signal integrity point of view, reflecting at the ends creating resonances in the transmission line. As the frequency increases to half wavelength, the series resonance builds up a standing wave pattern reflecting from the open edges of the plane. Fortunately, this happens above 1GHz.

Also, the mounting inductance of each capacitor needs to be taken into account. The mounting inductance is comprised of three components: Capacitor footprint and fanout, capacitor height above or below the plane and power plane spreading inductance. These three elements describe the loop in which current must flow – the bigger the loop, the more the inductance. The footprint (land pattern) for a capacitor dominates the total ESL. It consists of via placement with respect to the pad, the length and width of traces connected to the pad, and the way the vias are connected to the power and ground planes. The location of the power/ground planes in the PCB stackup controls the height of the via. Inductance directly depends on the magnetic field, so reducing the energy associated with the loop area reduces overall inductance.

The inductance associated with current spreading, into the power/ground planes, also contributes to the total mounted inductance. Current in the planes becomes concentrated in the vicinity of the vias. This current creates a high magnetic field and therefore contributes to inductance.

With the continuous trend to smaller feature sizes and faster signal rise times, Planar Capacitor Laminate or Embedded Capacitor Materials (ECM) is becoming a cost-effective solution for improved power integrity. This technology provides an effective approach for decoupling high-performance ICs whilst also reducing electromagnetic interference.

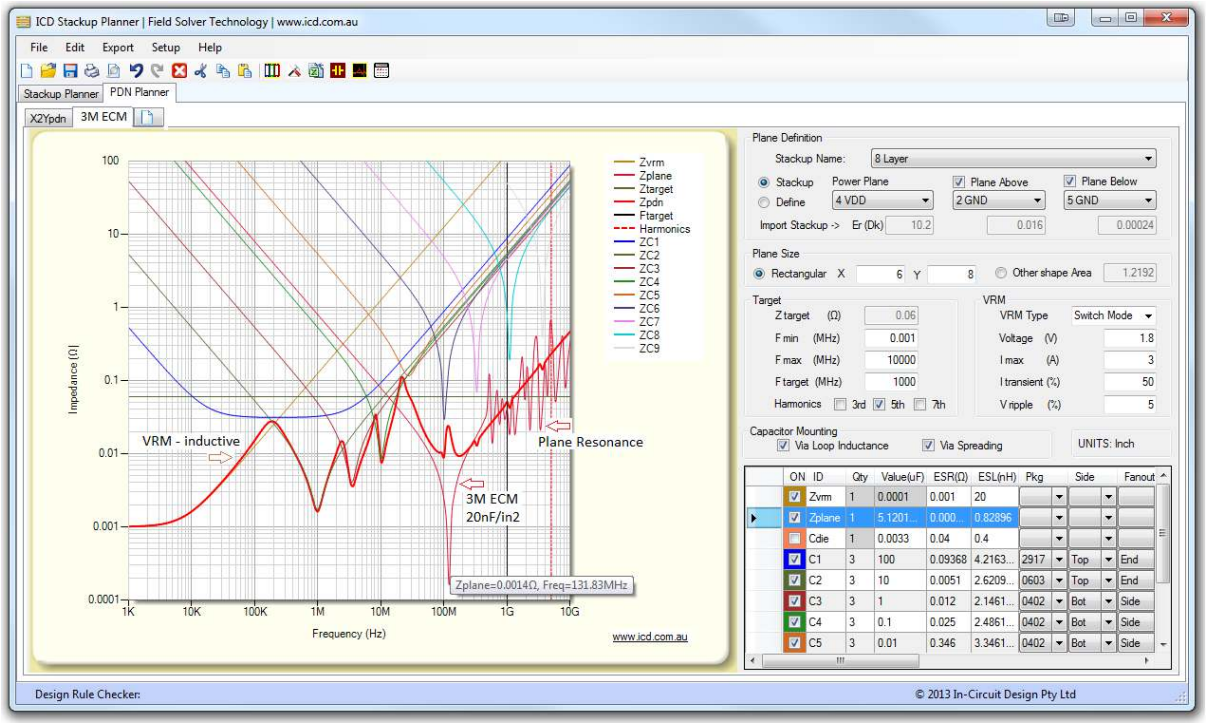

Figure 6 – One value capacitor per decade approach including VRM, loop inductance and plane capacitance of 3M ECM

Planar Capacitor technology, allows for a very thin dielectric layer (0.24 – 2.0mil) that provides distributive decoupling capacitance, of 20nF/in^2 in this case. This also increases real estate (space), reduces the number of vias and opens up routing channels. Unfortunately, standard decoupling capacitors have little affect over 1GHz and the only way to reduce the AC impedance of the Power Distribution Network above this frequency is to use ECM or alternatively on-die capacitance. These ultra thin laminates replace the conventional power and ground planes and have excellent stability of Dielectric Constant and Loss up to 15GHz.

In Figure 6, the ICD PDN Planner shows the one value per decade approach including the Voltage Regulator Module (VRM) which is mainly inductive, the total loop inductance of each capacitor, via spreading inductance and the plane capacitance. The plane resonance can be seen on the right. In each case, a 0.24mil, 3M Embedded Capacitor Material (ECM), that provides 20nF/in^2, was used to drop the PDN to below the simulated target impedance up to 1.3GHz. By comparison, the target frequency and the optimized value approached in Figure 7, also have the VRM, loop inductance and plane capacitance of 3M ECM included.

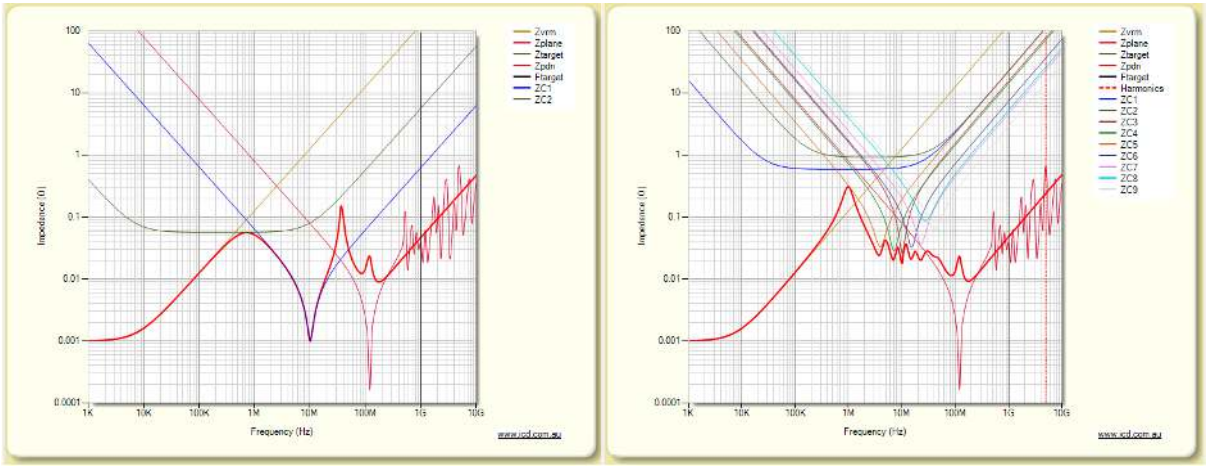

Figure 7 – Target frequency and optimized value approaches including VRM, loop inductance and plane capacitance of 3M ECM

So which approach is best?

1. The target frequency approach gives a clean “V” shape with just one small anti-resonant peak at 40MHz and is below the target impedance up to 1.3GHz;
2. The one value capacitor per decade approach has one peak at 23MHz and is also below the target impedance up to 1.3GHz and
3. The optimized value approach is also good from 2.3MHz to 1.3GHz with a peak at 1MHz.

But, in reality, only plane capacitance, on-die capacitance or changing the plane size (area) can reduce the impedance beyond several 100MHz.

So it is really six of one and half a dozen of the other! Personally, I prefer the target frequency approach, as it is less time consuming to analyze and requires fewer parts – which means the BOM count is reduced, holding stock is reduced and assembly equipment setup and placement times are greatly reduced. This all leads to reduction in cost and time to market and of course a more reliable end product. Also, this method can be used to dampen electromagnetic emissions at a particular frequency. Whichever way, each PDN on the board should be analyzed to give confidence in the final product.

Points to remember:

- There are three approaches to analyzing the PDN: target frequency, one value capacitor per decade or optimized value.
- Poor PDN design can result in unusual, intermittent signal integrity issues including high crosstalk and excessive emission of radiation.
- The integrity of the PCB stackup and the PDN are the basis for a stable product.
- Decoupling is not the process of placing a capacitor adjacent to the IC, but rather it is the process of placing an L-C network adjacent to the IC to supply the high transient switching current.
- Decoupling capacitors supply instantaneous current – at different frequencies – to the drivers until the power supply can respond.
- For bulk decoupling at the supply level, tantalum is usually preferred, due to the availability of high capacitance ratings.
- Large capacitance value ceramics provide effective decoupling at about 25% of the nominal capacitance value compared to standard tantalums.
- The capacitance of a capacitor is determined by three factors. The number of layers in the part, the dielectric constant and the active area.
- The dielectric thickness is inversely related to the capacitance – so the thicker the dielectric, the lower the capacitance value.
- The rating compared to working voltage for Multi-layer Ceramic Capacitors is 2:1.
- The Dielectric Constant depends on the ceramic material used. NP0 has the lowest dielectric constant, followed by X7R and Y5V.
- Dissipation Factor (Df) is the percentage of energy wasted as heat in the capacitor.
- While X2Y MLCCs offer superior performance and space wise, they are about five times the price of standard 0402.
- A capacitor's equivalent circuit is basically a series capacitor, resistor and inductor. These are referred to as the capacitance value, ESR and ESL respectively.
- The downward slope of the capacitor is capacitive, then as the capacitor approaches its SRF it becomes resistive, then as the frequency increases the inductance takes over raising the impedance again.
- To meet the target (low) impedance at a particular frequency, a capacitance value is chosen so that when mounted on the PCB, it will resonate at the desired frequency, and have an impedance that is equal to its ESR.
- The combination of capacitors causes anti-resonant peaks, where one goes capacitive while the other is inductive.
- When the SRFs are spread, the parallel resonant impedance sets the limits to the PDN performance.
- The mounting inductance is comprised of three components: Capacitor footprint and fanout, capacitor height above or below the plane and power plane spreading inductance.
- Embedded Capacitance technology allows for a very thin dielectric layer (0.24 – 2.0mil) that provides distributive decoupling capacitance and takes the place of conventional discrete decoupling capacitors over 1GHz.

References:

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Signal and Power Integrity Simplified – Eric Bogatin
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SMT Capacitor Comparison - Kemet
Understanding capacitor inductance – X2Y
The ICD PDN Planner can be downloaded from www.icd.com.au

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Bio - Barry Olney is Managing Director of In-Circuit Design Pty Ltd (ICD), Australia. The company developed the ICD Stackup Planner and ICD PDN Planner software, is a PCB Design Service Bureau and specializes in high-speed, board level simulation.