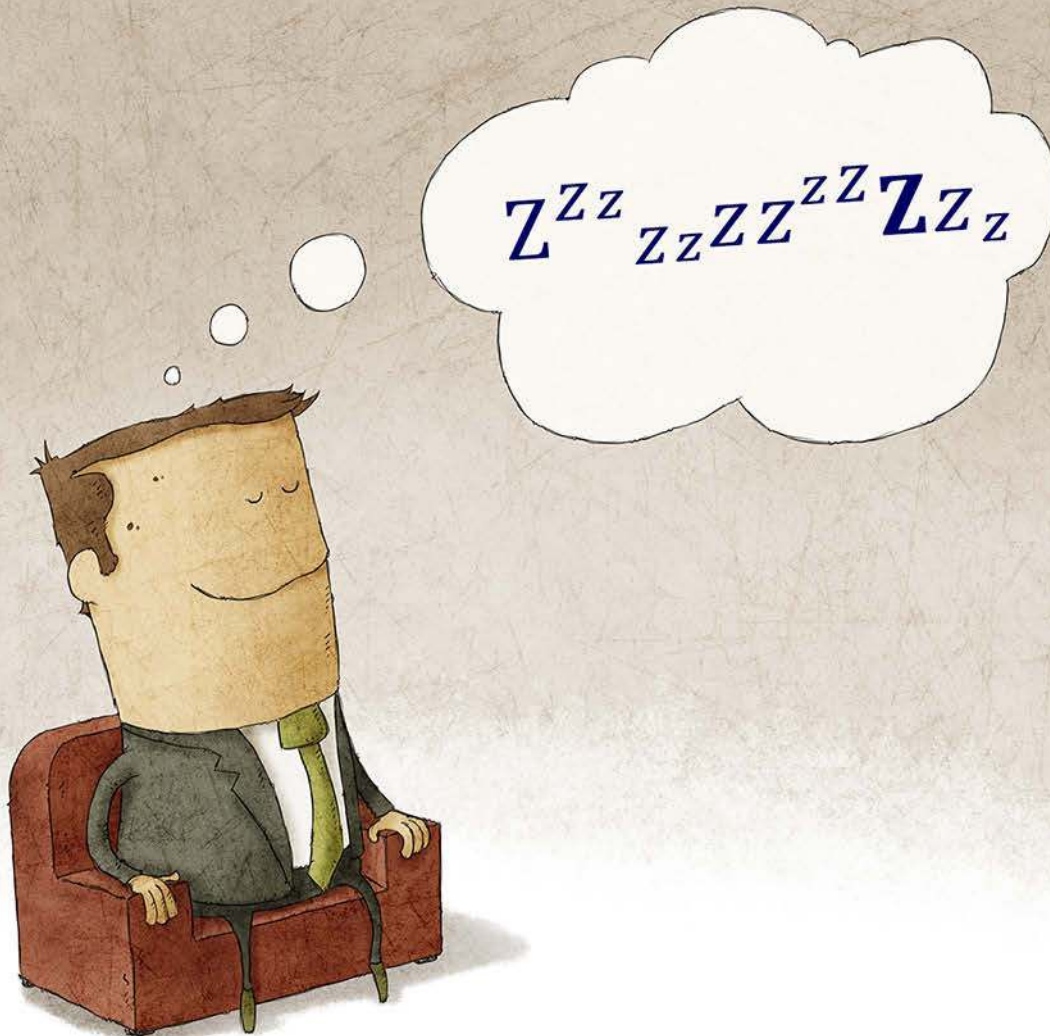


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PCB Design Challenges: Change is Good

Beyond Design

Feature Column by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

In 2022, PCB designers are faced with two big challenges: demands for increased performance and a condensed product footprint. So, what's new? I recall some 50-odd years ago the challenges for the electronics professional were much the same. I had just become comfortable with valves and then came diodes, transistors, and LEDs. After mastering germanium and then silicon diodes/transistors, along came op-amps. Now, these devices were very mysterious. Basically, they have several transistors acting as pre-built functional blocks packaged into an 8-pin DIL package. They had many uses from amplifiers to comparators and issued in the start of digital electronics. And who could forget the 555 timer with its millions of applications?

Next were digital logic gates. Now, these multiple gate devices could be run at an astonishing 10 MHz which seemed incredibly fast at the time. You could combine them to perform almost any digital function. Analog-to-digital (ADC) and digital-to-analog (DAC) convert-

ers allowed us to mix the analog world with the digital.

Then in 1974, Intel released the 8080 8-bit microprocessor followed closely by the 8086 16-bit chip. In the early 1980s, I was working in the Microprocessor Research Lab at the University of Western Australia. We were building portable computers into desks on wheels for the Masters' and PhD candidates using these processors. These machines were a major step-up from the departmental PDP-1140. The Z80 CPU, which was an extension of the 8080, became very popular with enthusiasts. I bought a UK-developed MicroBee Z80 kit which had 16K of RAM expandable up to 64K (if I would ever have a use for such a huge amount of memory).

I recall that some colleagues totally rejected computers and never took the time to step up to the new emerging technology and were left behind. Whereas those of us who embraced it were whisked along with the trending computer upsurge.

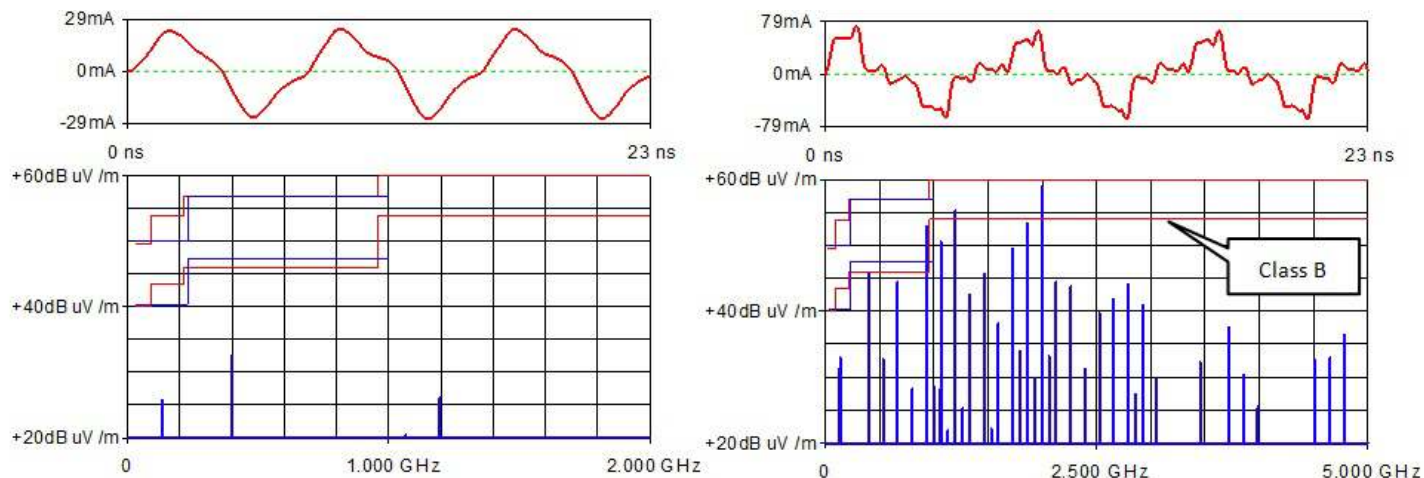


Figure 1: Radiated emissions from the 10 ns edge rate (left) and 1 ns (right).

By 1986, surface mount technology (SMT) had gained popularity and was accounting for 10% of the market. The need to increase functionality and to reduce the product size and time-to-market forced product designers to adopt this new technology. In 1990, I took on the challenge, attended the many trending SMT conferences and training courses, and changed our product development to the process.

Programmable devices enabled us to use the same hardware with different strains of software allowing the creation of multiple products from the one PCB design. FPGAs reduced the need for application-specific ICs. The list goes on, but there was always constant change.

As system performance increases, the PCB designer's challenges become more complex. The impact of lower core voltages, high frequencies, and faster edge rates has forced us into the high-speed digital domain. Power consumption has become a primary factor for FPGA selection. Whether the concern is absolute power consumption, usable performance, battery life, thermal challenges, or reliability, power consumption is at the center of it all. To reduce power consumption, IC manufacturers have moved to lower core voltages and higher operating frequencies which, of course, mean

faster edge rates. The enhancements in driver edge rates have a significant impact on signal quality, timing, crosstalk, and EMC.

The faster edge rate for the same frequency and same length trace creates ringing in an unterminated transmission line. This also has a direct impact on radiated emissions. Figure 1 shows the massive increase in emissions from 10 ns to 1 ns. When dealing with sub-nanosecond rise times, the emissions can easily exceed the FCC/CISPR Class B limits for an unterminated transmission line.

As signal rise times increase, consideration should be given to the propagation time and reflections of a routed trace. If the propagation time and reflection from source to load are longer than the edge transition time, an electrically long trace will exist. If the transmission line is short, reflections still occur but will be overwhelmed by the rising or falling edge and may not pose a problem. But even if the trace is short, termination may still be required if the load is capacitive or highly inductive, to prevent ringing. Note that series terminators are the most effective for high-speed design.

Power distribution network (PDN) planning is another relatively new technology that has become an essential, interrelated component of signal integrity analysis. However, main-

stream PCB developers have yet to adopt PDN analysis as a common design process. But now that the technology is proven and the uptake costs have decreased dramatically, there is no reason why all designers should not take advantage of the technology to improve the reliability and performance of their products. The goal of robust PDN planning is to design a stable power source for all the required onboard power supplies (Figure 2).

The trend in lower DC voltages also requires tighter voltage noise tolerances and higher currents. Market demands are forcing product designers to create PDNs with greater density, higher power efficiencies and lower costs, making the process even more challenging.

Soon there will be major advances in the following fields:

1. Renewable energy technologies to reduce our carbon footprint and climate change. Fusion reactors. Electric and hydrogen vehicles and battery technology.
2. Quantum computers. They will significantly shorten product development cycles and reduce the costs for R&D. New data encryption technologies.
3. Artificial intelligence. Advances in self-driving vehicles. Virtual spaces bringing us closer together.
4. A new era in medicines. CRISPR gene editing and mRNA vaccines and their many uses.
5. Communications and streaming services. 5G networks are already in use. And constellations of Starlink satellites will bring low latency internet access globally and to lower earth orbit.
6. Space tourist, space exploration, and asteroid mining.
7. 3D printed construction. A cost-effective way to build houses, factories, and space structures. Not forgetting built-up multilayer PCB construction.

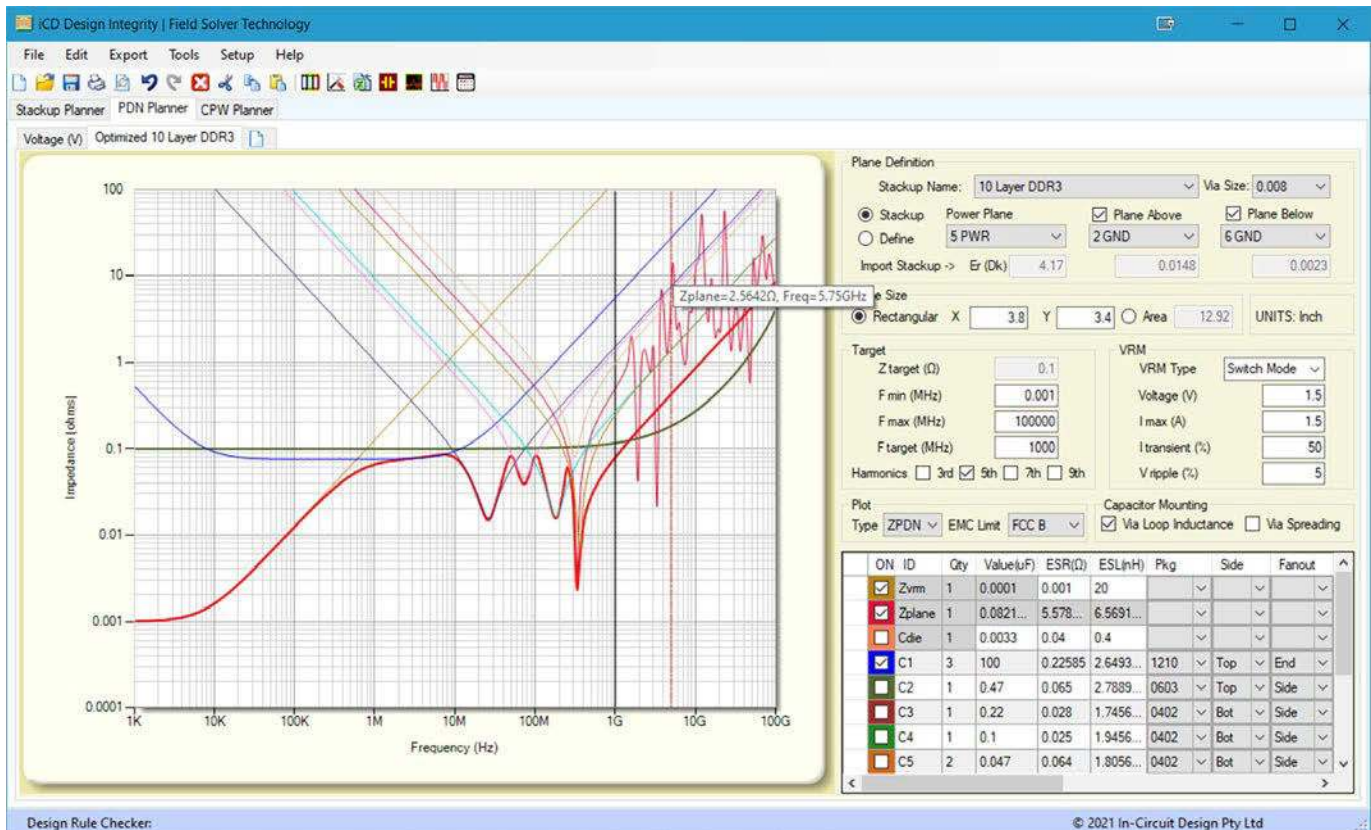


Figure 2: AC impedance profile of a DDR3 supply. (Source: iCD PDN Planner)

I'm sure there will be many more. All these technologies require new or adaptive ways of producing electronic products. Smaller size, flexible design with improved performance all adds up to advances in PCB design techniques. Designers can expect to see more high-speed serial links and faster buses and memory devices requiring signal and power integrity skills. With the advancements in automotive technologies, one would expect a merger of microwave/RF techniques in the PCB design realm.

There has also been a change in the demographics of the PCB design team over the past decade. Boards have been chronically designed by a PCB designer who is a specialist in the field. However, with fewer designers entering the workforce than retiring, the response has been to involve more degreed engineers with PCB design. The engineers will not be specialists and will only design one or two boards a year, but they bring advantages too. They are much more familiar with the constraints, and why they are important. They may also have a much greater understanding of signal integrity, power distribution network design, signal propagation, and thermal characteristics. Future designs will be more complex and require these skills.

We feel comfortable and secure in doing things the way we have always done them. But constant change is part of being in the field of electronics. So why not embrace change and learn new technologies and master new skills? I have always said that change is good. It brings new challenges but also rewarding opportunities. Look for opportunities and act on them.

Key Points

- As system performance increases, the PCB designer's challenges become more complex.
- The impact of lower core voltages, high frequencies, and faster edge rates has forced us into the high-speed digital domain.

- If the propagation time and reflection from source to load are longer than the edge transition time, an electrically long trace will exist.
- Power distribution network (PDN) planning is another relatively new technology that has become an essential, interrelated component of signal integrity analysis.
- The trend in lower DC voltages also requires tighter voltage noise tolerances and higher currents.
- Smaller size, flexible design with improved performance all adds up to advances in PCB design techniques.
- With fewer designers entering the workforce than retiring, the response has been to involve more degreed engineers with PCB design.
- Constant change is part of being in the field of electronics. **DESIGN007**

Resources

1. [Beyond Design: Signal Integrity Part 1 of 3](#), by Barry Olney, *The PCB Design Magazine*, October 2014.



Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating

the iCD Stackup, PDN, and CPW Planner. The software can be downloaded at www.icd.com.au. To read past columns or contact Olney, [click here](#).