Beyond Design: There are no one way trips!

by Barry Olney | In-Circuit Design Pty Ltd |Australia

One of the greatest myths, of PCB design, is that we only have to route signal traces from pin-to-pin to make a complete connection. And, that ensuring these traces have matched delay is the only timing issue we need to consider. However, current is not a one way trip – it must complete the circuit back to the source in order to provide the round trip current loop. This misconception comes from the fact that we only draw the pin-to-pin connections on the schematic and ground the chips at one point.

Current always flows in a loop. However it does not go down to the end of the trace, to the load, and then begin to make its way back to the source. But rather, the outbound pulse charges the local parasitic capacitance as it propagates down the transmission line and returns to the driver. As the pulse progresses, down the line, current returns to the source as the wave front moves until it finally reaches the load. If the return path is disrupted and does not flow directly beneath the trace, the loop area and hence delay is extended. This generally results in increased emissions of radiation.

In a previous column, Beyond Design: The Dumping Ground, I discussed why the ground plane is not a dumping ground for unwanted signals. Most PCB designers think that the ground only serves to make the routing easier, allowing the designer to ground anything, anywhere without having to run multiple tracks. Generally a component requiring a ground connect, is just grounded at any point on the board creating the connection. But, this does not consider the return current path which is just as important as the actual trace routing for high-speed design.

In a DC circuit, the return current takes the path of least resistance. But at high-speed, the return current takes the path of least inductance which just happens to be the reference plane (either ground or power) directly above or below the trace.

The planes in a high-speed, digital board perform four crucial functions:

1. Provide a reference voltage for the exchange of digital signals
2. Distribute stable power to all logic devices
3. Control crosstalk between switching signals
4. Provide a shield for electromagnetic radiation on internal layers

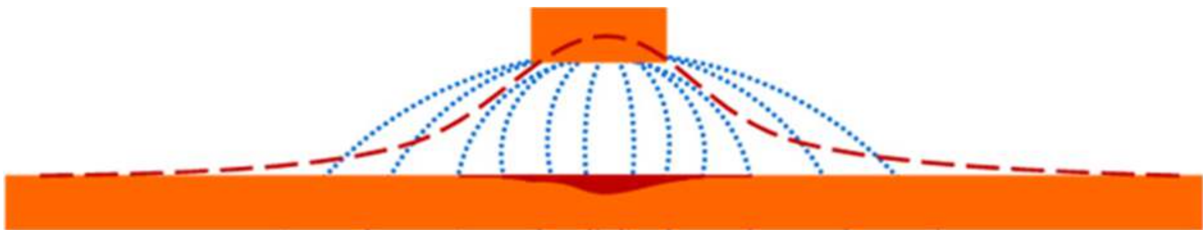


Figure 1 – Microstrip plane return current distribution

Figure 1, illustrates the cross-section on a microstrip (outer layer) trace and its associated plane return current distribution (red). Where the electric fields (blue) are more tightly coupled to the plane – directly below the trace – the return current also exhibits tighter coupling. But where the field spreads out from the trace, the larger loop area, between the signal and the return current path, increases the inductance. Return current tends to couple to the signal conductor, falling off in intensity, with the square of increased distance. A stripline (inner layer) return current distribution is narrower with the fields more intense above and below the trace.

Because of the skin affect, the high frequency fields cannot penetrate the plane and so the reference plane return currents will exist where the electric field lines terminate on the adjacent plane. Magnetic fields, which are not illustrated, circle the trace and radiate outward.

For a microstrip trace the return current density J(x) is given by:

$$J(x) = \frac{I}{w\pi}\left[tan^{-1}\left(\frac{2x-w}{2h}\right) - tan^{-1}\left(\frac{2x+w}{2h}\right)\right]$$

where: Equation 1

I is the total loop current
x is the horizontal distance out from the centre of the trace
w is the width of the trace and
h is the distance of the trace from the plane

The current density will be the same regardless of the frequency. The only constraint is that the frequency is high enough so that the resistance of the plane is negligible, compared with the inductive reactance. Typically, this occurs at frequencies above a few hundred kilohertz – so that's basically any digital PCB.

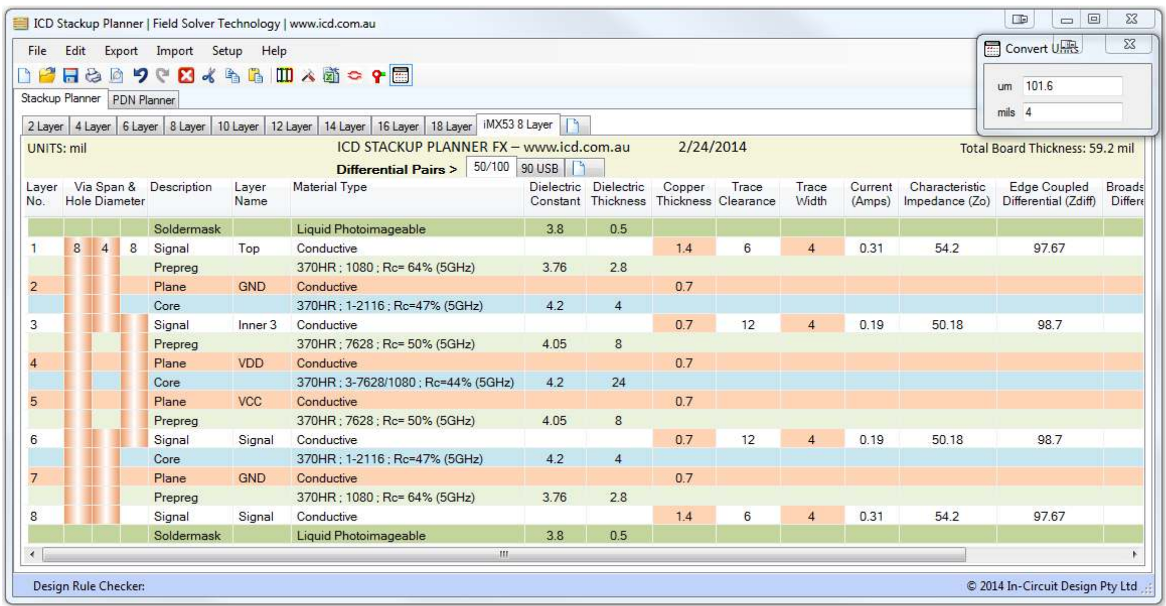
Crosstalk between adjacent traces (edge-coupled) is the result of the interaction of these fields.

$$Crosstalk = \frac{h^2}{x^2}$$

Equation 2

Equation 2, shows that the crosstalk between adjacent microstrip traces is proportional to the square of the trace height above the plane divided by the square of the separation distance. This illustrates an important point – that placing the trace closer to the reference plane will reduce crosstalk even if the trace spacing remains the same. This provides an effective way to reduce crosstalk without using up valuable real estate on the board which would be the case if the trace separation were increased.

Now that we have established the fact that the return current follows the path of least inductance, and that it has a defined distribution in the reference plane, we need to now look at how the return current propagates in the planes.



Layer No.	Via Span & Hole Diameter			Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broads Differe
				Soldermask		Liquid Photoimageable	3.8	0.5							
1	8	4	8	Signal	Top	Conductive			1.4	6	4	0.31	54.2	97.67	
				Prepreg		370HR ; 1080 ; Rc= 64% (5GHz)	3.76	2.8							
2				Plane	GND	Conductive			0.7						
				Core		370HR ; 1-2116 ; Rc=47% (5GHz)	4.2	4							
3				Signal	Inner 3	Conductive			0.7	12	4	0.19	50.18	98.7	
				Prepreg		370HR ; 7628 ; Rc= 50% (5GHz)	4.05	8							
4				Plane	VDD	Conductive			0.7						
				Core		370HR ; 3-7628/1080 ; Rc=44% (5GHz)	4.2	24							
5				Plane	VCC	Conductive			0.7						
				Prepreg		370HR ; 7628 ; Rc= 50% (5GHz)	4.05	8							
6				Signal	Signal	Conductive			0.7	12	4	0.19	50.18	98.7	
				Core		370HR ; 1-2116 ; Rc=47% (5GHz)	4.2	4							
7				Plane	GND	Conductive			0.7						
				Prepreg		370HR ; 1080 ; Rc= 64% (5GHz)	3.76	2.8							
8				Signal	Signal	Conductive			1.4	6	4	0.31	54.2	97.67	
				Soldermask		Liquid Photoimageable	3.8	0.5							

Figure 2 – An 8 layer stackup using Isola 370HR, 5GHz material

Figure 2, shows the ICD Stackup Planner (download from www.icd.com.au) creating an 8 layer stackup for an iMX53 processor and DDR2 memory combination. In this case, layers 1 & 3 and layers 6 & 8 are used for the layer pairs and all routing encircles the ground planes on layers 2 and 7. Since the ground is referenced is all cases, ground stitching vias can be placed near layer transitions (vias) to allow the return current to change planes where required. This limits the loop area, hence radiation.

Or maybe using a buildup microstrip layer would be better if you are risk aversive? In Figure 3, I have added another buildup layer to the stackup (top and bottom). Copper plating on outer layers attributes considerable variations in trace width and thickness, hence impedance variations. You should avoid routing controlled impedance signals on these layers, but they can be used for pads/lands and traces that are non-critical. Via-in-pad could be used or a just short (<200mil) fanout to layer 2 using a 12 mil trace in an attempt to maintain impedance.

Layer No.	Via Span & Hole Diameter	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)
		Soldermask		Liquid Photoimageable	3.8	0.5						
1	8 4 8	Signal	Top	Conductive			1.4	20	12	0.69	50.19	98.28
		Prepreg		370HR ; 1080 ; Rc= 64% (5GHz)	3.76	2.8						
2		Signal	Inner 2	Conductive			0.7	15	4	0.19	50.7	98.52
		Prepreg		370HR ; 1080 ; Rc= 64% (5GHz)	3.76	2.8						
3		Plane	GND	Conductive			0.7					

Figure 3 – 10 Layer Buildup alternative stackup (only top shown)

In order to change reference planes:

- If there are multiple ground planes, then place a stitching via as close as possible to each layer transition (signal via).
- If power planes are also used as the reference plane, then place decoupling capacitors as close as possible to each layer transition.

When you plan your stackup, be aware of which plane(s) – either power or ground – will be the return path for your critical signals and make sure there is an unobstructed return path. The best way to think of this is to imagine routing a return trace adjacent to each signal trace on the reference plane – where is the best place for the current to flow and is it unobstructed? The reference plane(s) adjacent to each signal layer allows the return current to flow as closely as possible to the signal trace, reducing inductance and loop area. A large loop area will create higher emissions of electromagnetic radiation, so we need to keep these as tightly coupled to the trace as possible.

The best way to go about this is to look at each signal layer with respect to its associated reference plane. Figure 3, shows an internal signal layer and the ground plane. Make sure that there are no large cut-out areas or lines of anti-pads on connectors that completely block off the ground, forcing the return paths to deviate from their associated traces. This is best done in a CAM/Gerber viewer as what you see – is what you get. Whereas, in the CAD database you may not see the correct antipad or plane cut-out sizes. You may have to reduce the size of the anti-pads if they are too close. SMT boards are not so bad, in this respect, but through-hole connectors generally create issues.

Also, keep in mind that high speed signals should not be routed on the outer layers. Embedding the signals between the planes (on layers 3 & 6) reduces the radiation by at least 10 dB. So, fanout from the driver and drop to the internal signal layer routing up to the load through a short stub.

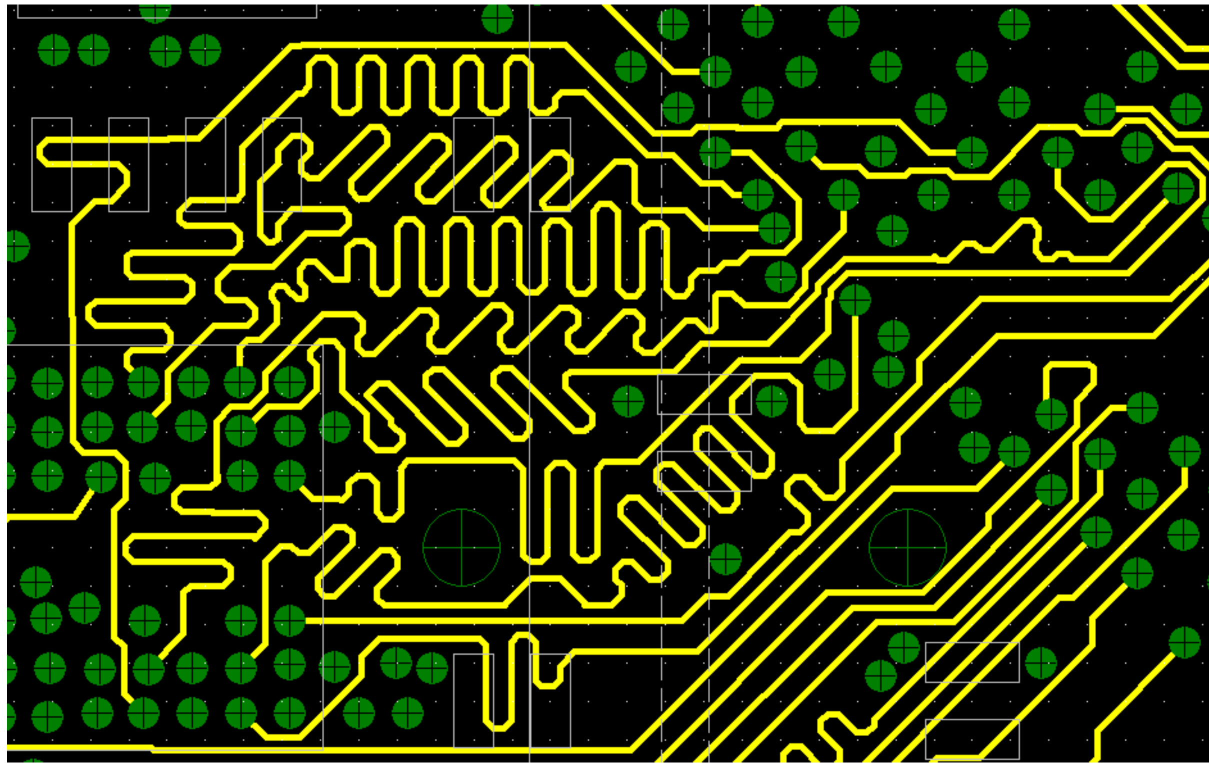


Figure 3 – Signal layer 3 with respect to ground plane layer 2

In conclusion, apart from routing pin-to-pin, it is important to also consider how the return current propagates in the planes. When you plan your stackup, be aware of which plane(s) – either power or ground – will be the return path for your critical signals and make sure there is an unobstructed return path.

Points to Remember:

- Current always flows in a loop. The outbound pulse charges the local parasitic capacitance as it propagates down the transmission line and returns to the driver.
- The ground plane is not a dumping ground for unwanted signals.
- In a DC circuit, the return current takes the path of least resistance.
- At high-speed, the return current takes the path of least inductance which just happens to be the reference plane (either ground or power) directly above or below the trace.
- Return current tends to couple to the signal conductor, falling off in intensity, with the square of increased distance.
- Because of the skin affect, the high frequency fields cannot penetrate the plane.
- The current density will be the same regardless of the frequency.
- Placing the trace closer to the reference plane will reduce crosstalk even if the trace spacing remains the same.
- It is important to consider how the return current propagates in the planes. When you plan your stackup, be aware of which plane(s) – either power or ground – will be the return path for your critical signals and make sure there is an unobstructed return path.
- If there are multiple ground planes, then place a stitching via as close as possible to each layer transition (signal via).
- If power planes are also used as the reference plane, then place decoupling capacitors as close as possible to each layer transition.

References:
Beyond Design: The Dumping Ground – Barry Olney
Beyond Design: Embedded Signal Routing – Barry Olney
High-speed Signal Propagation – Howard Johnson
Electromagnetic Compatibility Engineering – Henry Ott
The ICD Stackup Planner and PDN Planner can be downloaded from www.icd.com.au

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Bio - Barry Olney is CEO of In-Circuit Design Pty Ltd (ICD), Australia. The company developed the ICD Stackup Planner and ICD PDN Planner software, is a PCB Design Service Bureau and specializes in high-speed, board level simulation.