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Mixed Digital-Analog Technologies

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SUMMARY: *The key to a successful, mixed digital-analog design is functional partitioning, understanding the current return path, routing control and management, and using a common ground plane.*

Introduction

Field programmable gate arrays (FPGAs) are becoming more complex, integrating functions such as processors, multi-gigabit SERDES transceivers and support for multiple I/O standards. However, designing power management and signal paths (including analog-to-digital converters, operational amplifiers and interface) around these FPGAs is no easy task.

Selecting the Best (Power Distribution Network) PDN Architecture

Linear regulators are simple and easy to use and in most cases, ideal for analog circuitry as they source clean, low noise. But the downside with linear regulators is power dissipation. The power that is not required by the circuit is dissipated as heat. Linear regulators are typically used in the following scenarios: 1) when an output current less than 1A is required; 2) when

ultra-low dropout is required; and 3) for low-noise applications.

On the other hand, switching regulators offer high-efficiency, low-heat dissipation, and the ability to step-up or step-down a voltage. Plus, they can source high currents (>5A) if required by digital systems. These are ideal when high-efficiency is required, combined with high current output or low-duty cycles.

Also, today's high-density, high-performance FPGAs typically require a number of different power supplies (for example 3.3V, 2.5V, 1.8V and 1.5V) to power the core and I/O. These are best sourced from a switch mode power supply. Core current consumption depends upon utilization of the part (such as clock speed and internal elements used), but maximum values range from 1.5A to 10A. Current consumption for the I/Os depends on the voltage and the utilization of the I/O elements; however, for all I/O banks operating together, the maximum current demand can exceed 10A.

Another power management consideration that needs to be addressed is the monotonic rise of voltage in the core and I/O to their steady state levels. This consideration is critical for the correct operation of the FPGA because if the voltage sags during boot-up, the device may not reset. While many power supplies take this requirement into consideration, it is recommended to further support this requirement by the use of adequate bulk capacitance in the PDN.

Linear power supplies, because of their low current and limited frequency range, generally do not require analysis, although it is a good design practice to provide immediate, low-impedance power at all frequencies of interest. Figure 1 illustrates the use of the

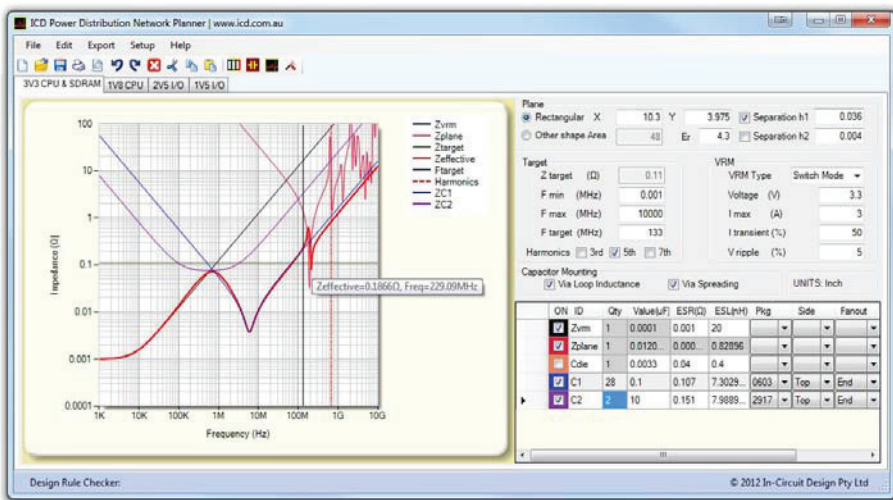


Figure 1: The ICD PDN Planner analyzes the AC impedance of a 3.3V FPGA supply.

ICD PDN Planner (downloadable from www.icd.com.au) to analyze the AC impedance of a 3.3V CPU and SDRAM power supply—in order to minimize the impedance across the entire frequency range.

When planes are used to distribute power, crosstalk—or common-mode impedance coupling—can pass through the ground-return path associated with high-speed digital signals. Essentially, return current causes a ground-potential rise due to the DC resistance of the plane. This problem can be significant, especially with noise-sensitive analog circuitry.

The question you may be asking at this point is: How do we prevent digitally-induced ground currents from contaminating the low-level analog circuitry?

Partition the PCB into Separate Sections

All components on a PCB must be grouped into functional sections: RF, high-speed digital, analog, switch mode supplies, etc. Typically, this is done at the schematic-entry level where symbols are grouped into rooms or classes. Using schematic to PCB cross-probing, the functional blocks are then transferred to the PCB database and placed accordingly.

Each of these sections may require different power supplies, possibly driving the need for power planes to be split—in order to provide

access—if there are not enough planes in the stackup for each supply. This is fine, provided that continuous current return paths under high-speed digital signals are not compromised in the process. (It is important to note that a power plane can provide a low-impedance current-return path just like a ground plane.)

If a digital signal(s) must cross a split in the power reference plane, a plane jumper decoupling capacitor (100nF) can be placed close to the offending signal(s) to provide a path for the return current between the two supplies (e.g., 3.3V —||— 1.5V).

Confine Logic Families Geographically

Since crosstalk is induced by an aggressor trace(s) onto the victim trace, it is obvious that the higher the aggressor voltage, the more crosstalk will be induced. Therefore, it is best to further segregate groups of nets according to their signal amplitude. This strategy prevents larger voltage nets (e.g. 3.3V) from affecting lower-voltage nets (e.g. 1.5V) that have lower noise margins.

It is also preferable to partition these groups by rise time and frequency—positioning the fastest devices closest to the connector—as shown in Figure 2, and graduating the placement—in descending order of speed—down to the analog sections farthest from the connector, to avoid noise coupling into sensitive devices.

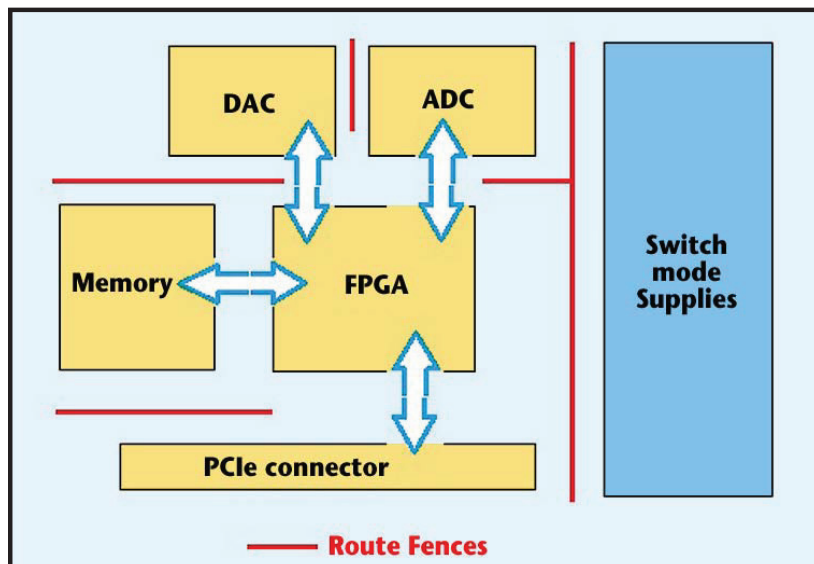


Figure 2: Route fences are used to control the routing.

Separate the Sections by Route Fences

Stating the obvious, all the analog signals should be routed in the analog section and all the digital signals have to be kept in the digital section, etc. Of course, control signals must route between them. The separation method, which I have used for many years, is to employ route “fences” or route keep-outs. Route fences can be defined by placing elongated keep-outs on all layers. Route fences are placed such that they direct the routing, so that no signal can cross these fences on any layer. Figure 2 illustrates a typical scenario.

It is important to keep in mind that high-speed return currents follow the path of least inductance rather than the path of least resistance. If, for instance, a trace is routed from the digital-to-analog converter (DAC) to the FPGA, the return current path will be directly below that trace and will not wander into nearby sections. Route fences control the autorouter, as well, by not allowing signals to cross, yet allowing the control signals to pass.

When the stackup is planned, be aware of which plane(s), either power or ground, will be the return path for your critical signals and make sure return paths are unobstructed. The best way to think of this is to imagine routing a return trace adjacent to each signal trace on the reference plane—where is the best place for the current to flow, and is it unobstructed? The reference plane adjacent to each signal layer allows the return current to flow as closely as possible to the signal trace, reducing inductance and the current-loop area.

One Common Ground Plane

The key to a successful mixed digital analog design is functional partitioning, understanding the current return path and routing control and management—not a split ground plane. It is always better to have only one single reference (ground) plane for a system.

So, we have one common ground plane, but it acts as if it were split into sections since all the traces go around—rather than through—the critical sections. Whereas, if the ground plane was split, with traces crossing the split, there would be no return path near the trace, and the current would have to flow in a large loop—causing an impedance discontinuity, crosstalk, and generating radiation.

There may also be multiple ground planes in the stackup. These ground planes should be stitched with ground vias, as close as possible to the signal vias, to allow the return paths to transition from plane to plane.

Digital-to-analog crosstalk issues arise when digital signals are routed in the analog section of the board, or vice-versa. Using the route fence approach, analog signals can be routed only in the analog section of the board (on any layer), and digital signals can be routed only in

the digital section of the board (on any layer).

The approach that I use—with one common ground, partitioned into sections, and with routing controlled by route fences—can usually solve an otherwise difficult layout problem without creating the additional issues associated with a split ground plane.

Points to Remember:

1. Linear regulators are ideal for analog circuitry as they feature clean, low noise at low current outputs.
2. Switching regulators offer high-efficiency, low heat dissipation, and high current, ideal for digital technologies.
3. The AC impedance of the PDN should be analyzed for each individual supply voltage.
4. Ensure that the signal return currents have an unobstructed path.
5. Group all components on a PCB into functional sections.
6. Confine logic families geographically to avoid noise coupling into sensitive devices.
7. Separate the sections by route fences to control and manage routing.
8. Use one common ground plane—not split ground planes. **PCB**

References

Analog Design Guide for Altera FPGAs and CLPDs—National Semiconductor.

Electromagnetic Compatibility Engineering—Henry Ott.

High Speed Digital Design—Howard Johnson.
The ICD PDN Planner may be downloaded from www.icd.com.au.



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