

# HIGH-SPEED PCB DESIGN TRAINING

---

- One-on-one mentoring
- Develop your skills with confidence
- Ensure your next design performs reliably



[LEARN MORE](#)



# Matched Length $\neq$ Matched Delay

by **Barry Olney**

IN-CIRCUIT DESIGN PTY LTD | AUSTRALIA

In previous columns, I have discussed matched length routing and how matched length does not necessarily mean matched delay. But, all design rules, specified by chip manufacturers regarding high-speed routing, specify matched length—not matched delay. In this

month's column we'll take a look at the actual differences between the two.

Typically, more than one layer change is required when routing traces to matched length. Figure 1 illustrates the DDR2 address bus routing I did in Altium Designer, my preferred lay-



Figure 1: Matched delay T-section DDR2 address routing in Altium Designer.

**Matched Length  $\neq$  Matched Delay** *continues*

out tool. In this case, each address signal has four layer changes. The red and green traces are the top and bottom layers—which should be kept as short as possible—and the yellow and orange traces are inner layers embedded between the planes. This was a particularly difficult route as there were two DDR2 memory chips placed on both the top and bottom sides of the board, so each address signal had to go to four different chips and still maintain the correct delay.

The longest routes should be placed on the inner layers as this reduces electromagnetic ra-

diation. With all other factors being equal, generally, a trace routed on the inner stripline layer exhibits 4–10 dB less noise than a trace routed on the outer microstrip layer. Also, please note that there are more high harmonics on the top layer routing. The high-frequency components radiate more readily because their shorter wavelengths are comparable to trace lengths, which act as antennas. Consequently, although the amplitude of the harmonic frequency components decreases as the frequency increases, the radiated frequency varies depending on the trace's characteristics.

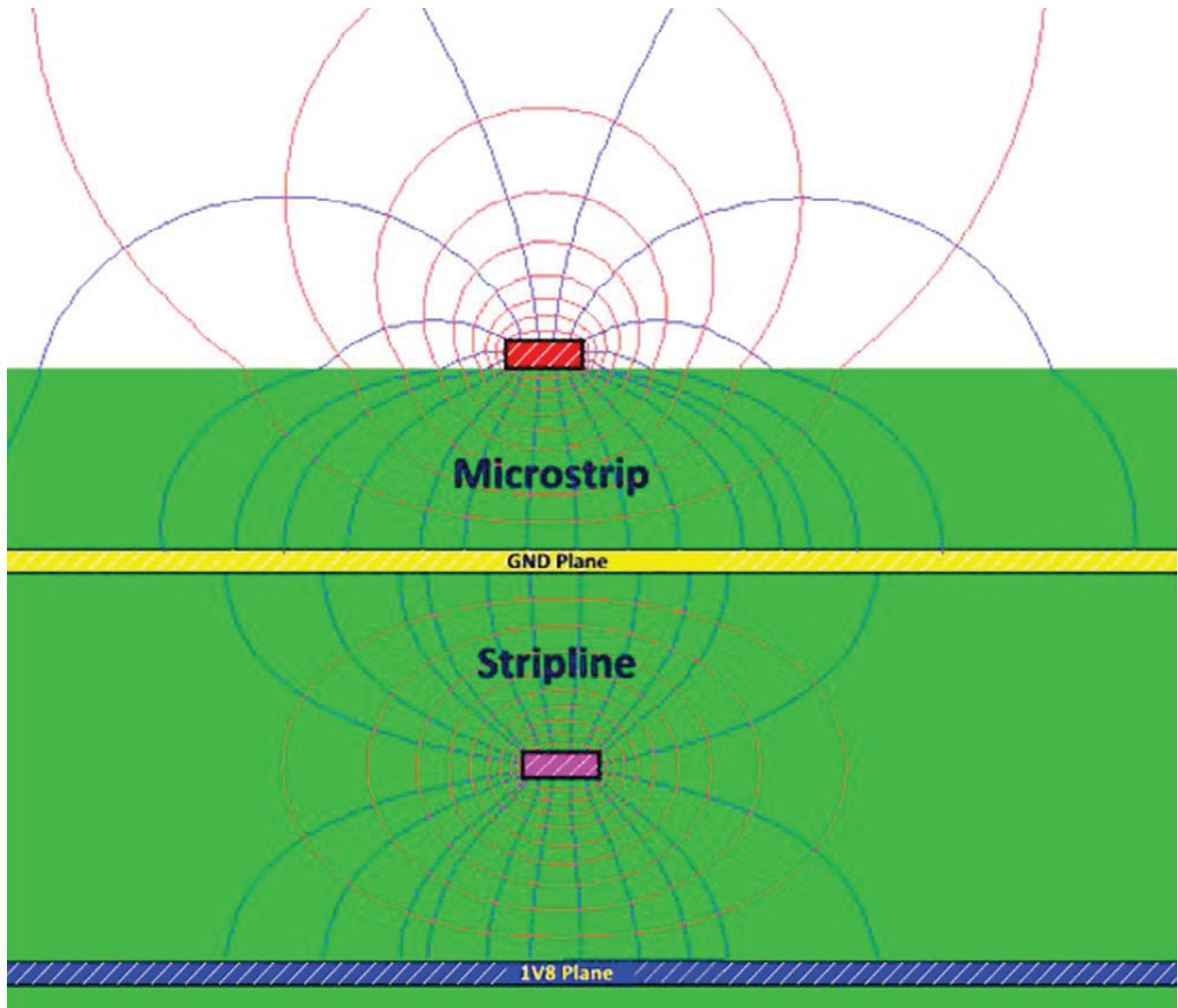


Figure 2: Electric (blue) and magnetic (red) field lines radiation from microstrip and stripline layers.

Microstrip layers are those that are fabricated on the outside of the substrate, top and bottom. Traces on these layers are referenced to the plane below/above, whether it be a ground or power plane. The trace has a dielectric material on either side: FR-4 below and air above. If you look closely at Figure 2, you can see where the field lines refract as they pass from the FR-4 (green) to the air dielectric. This is because the dielectric constant of FR-4 for example (~4.3) changes to air (1.0). The electric field is absorbed by the plane on one side and both the electric and magnetic fields also radiate into the air.

Stripline traces however, are totally embedded in dielectric material between planes. This may be a combination of materials—and dielectric constants—if for example multiple prepregs are stacked to obtain the desired thickness. The electric field is completely contained within the dielectric and blocked by the planes. The magnetic field still tends to radiate, from the board edges, but is limited somewhat.

Since the electromagnetic fields of microstrip layers partly reside within the surrounding air, the speed of propagation of a signal traveling on the microstrip trace is therefore partly determined by the dielectric properties of the PCB material and partly by the surrounding air. Microstrip traces are usually faster than stripline traces because the dielectric constant of air is lower than that of FR-4.

There are two exceptions to this:

1. If you use a microstrip prepreg with a high dielectric constant (Isola 370HR, 3.92) and in the stripline configuration a low dielectric

constant (fastRise FR-27 & TSM-26, ~2.7) as in Figure 3. The combination of air (1.0) and Isola 370HR (3.92) brings the total dielectric constant to approximately that of the Taconic fastRise materials, thus the traces exhibit a similar delay.

2. If you add a liquid photo-imageable solder mask, with a dielectric constant of say 3.3, to the outer layers, then the microstrip delay changes again. So it is best to compare the delays using a simulator otherwise you are just guessing.

Contrary to what you may believe, the propagation delay of a serpentine trace is less than the delay through an equivalent length straight trace. The signal is sped up because a portion of the signal will propagate perpendicular to the serpentine. And, this also varies with the type of serpentine pattern used. For example, the serpentine pattern may have long parallel lengths spaced close together in the “U” bend coupling the signal many times through the serpentine pattern. This self-coupling (forward and reverse crosstalk) shortens the electrical path. But in theory, the forward crosstalk—far-end crosstalk—does not exist in the stripline configuration. Please see my previous column, [Beyond Design: A New Slant on Matched-Length Routing](#), for further details.

Also, if two traces of equal length are referenced to different planes, then the return paths may be considerably different and add round-trip delay. This cannot be simulated, so it is important that the return paths are determined to be as short as possible. If planes are changed, then stitching vias or capacitors need

Layer No.	Via Span & Hole Diameter	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)
1	8, 4, 4	Signal	Top	Conductive			1.4	6	6	0.42	52.46	92.91	
		Prepreg		Isola 370HR : 2113 ; Rc= 56% (10GHz)	3.92	3.6							
2		Plane	GND	Conductive			1.4						
		Core		Taconic TSM-26; (10GHz)	2.6	3.5							
3		Signal	Inner 3	Conductive			1.4	12	6	0.42	47.13	91.84	50.06
		Prepreg		Taconic FR-27-0042-75; (10GHz)	2.73	5.2							
4		Signal	Inner 4	Conductive			1.4	12	6	0.42	47.13	91.84	50.06
		Core		Taconic TSM-26; (10GHz)	2.6	3.5							
5		Plane	1V8	Conductive			1.4						

Figure 3: Isola 370HR (microstrip) and fastRise FR-27 & TSM-26 (stripline) exhibit similar delay.

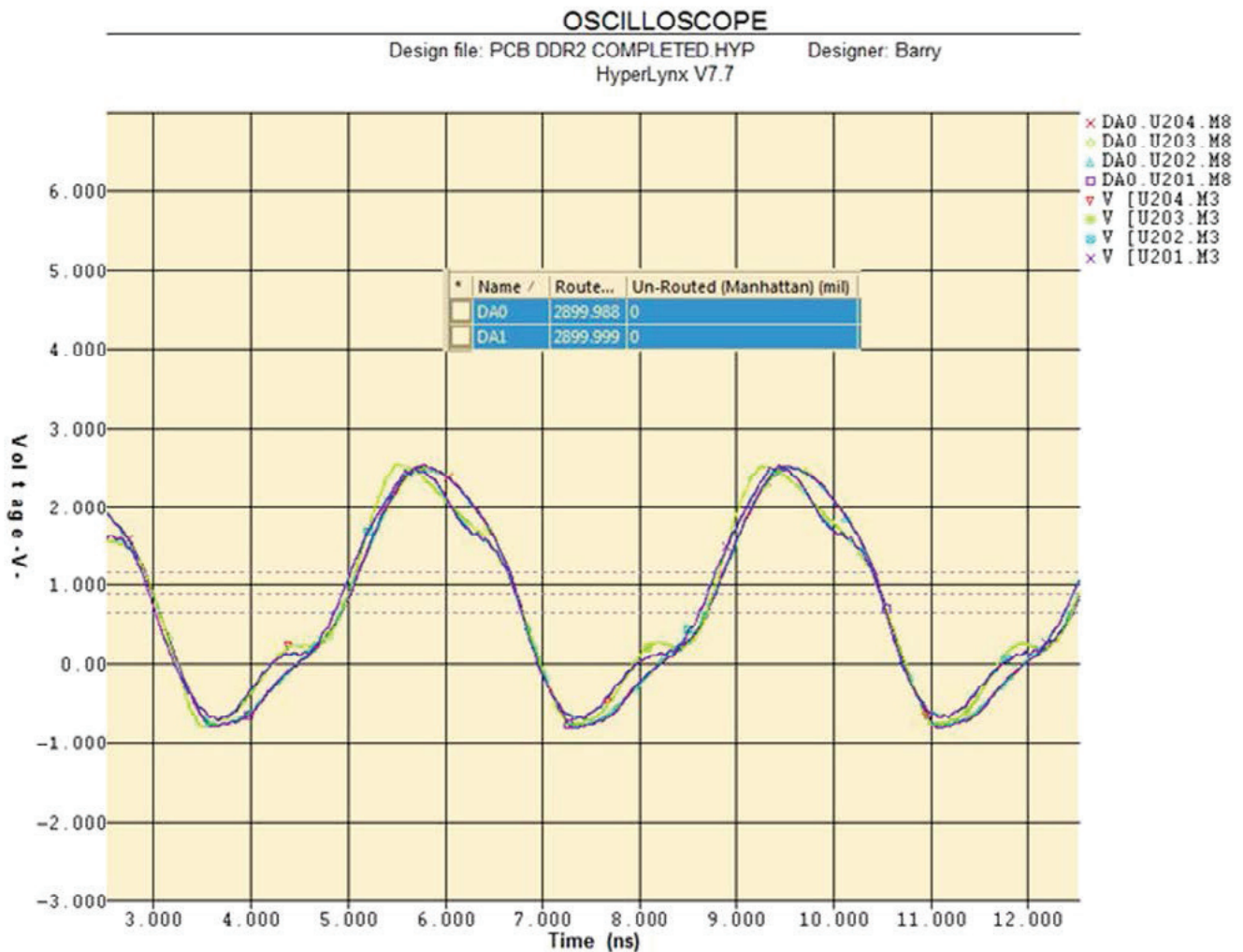
Matched Length  $\neq$  Matched Delay *continues*

Figure 4: Comparison of two matched length (2,900 mil) traces.

to be employed close to the layer transitions. Decoupling capacitors are normally placed near the processor and memory devices which help alleviate this issue.

To prove my point that two matched length traces both of 2,900 mil do not have equal delay, I have simulated two address signals and the results are shown in Figure 4. The delay difference here is 60ps—but still within spec. This is not much admittedly, but they are not matched, as the matched length would suggest. So, although these two signals are exactly the same length, because of the different combination of microstrip and stripline layers plus the fact that the signal propagates faster through serpentine routes, the delays are different.

The slight deviation in the signal waveforms, in Figure 4, is due to the impedance mismatch as the traces separate into two T-sections. Matching the impedance of bifurcated traces is practically impossible with tight routing constraints. However, this is not an issue in this case, since the waveform is stable and the variance does not appear near the trigger point (Vinh).

#### Points to Remember

- Matched length does not necessarily mean matched delay.
- The longest routes should be placed on the inner layers, as this reduces electromagnetic radiation.

**Matched Length  $\neq$  Matched Delay** *continues*

- A trace routed on the inner stripline layer exhibits 4–10 dB less noise than a trace routed on the outer, microstrip layer.
- Microstrip layers are those that are fabricated on the outside of the substrate, top and bottom. The trace has a dielectric material on either side—FR-4 below and air above.
- Microstrip traces are usually faster than stripline traces.
- Stripline traces are totally embedded in dielectric material between planes.
- The propagation delay of a serpentine trace is less than the delay through an equivalent length straight trace. The signal is sped up because a portion of the signal will propagate perpendicular to the serpentine.
- If two traces of equal length are reference to different planes then the return paths may be considerable different and add round-trip delay.
- Although two signals are exactly the same length, they may exhibit different delays.

**PCBDESIGN****References**

1. Barry Olney, Beyond Design: [Impedance Matching: Terminations, Skewed Again, A New Slant on Matched-Length Routing, Differential Pair Routing, Embedded Signal Routing](#)
2. Howard Johnson: [High-Speed Digital Design](#)
3. The ICD Stackup Planner and PDN Planner: [www.icd.com.au](http://www.icd.com.au)



Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. This PCB design service bureau specializes in board-level simulation, and has developed the ICD Stackup Planner and ICD PDN Planner software. To read past columns, or to contact Olney, [click here](#).

**video interview****Steinberger Papers A Big Hit**

by *Real Time with...*  
PCBDesign007



Dr. Michael Steinberger discusses a few of the papers he is presenting or co-wrote for DesignCon. Steinberger's papers always generate a great response at DesignCon, year after year.



[realtimewith.com](http://realtimewith.com)

