

# BOARD LEVEL SIMULATION SPECIALISTS

ICD Stackup Planner - offers engineers/PCB designers unprecedented simulation speed, ease of use and accuracy at an affordable price

- 2D (BEM) field solver precision
- Characteristic impedance, edge-coupled & broadside-coupled differential impedance
- Unique field solver computation of multiple differential technologies per stackup
- Heads-up impedance plots of signal and dielectric layers
- User defined dielectric materials library - over 16,250 materials up to 100GHz

ICD PDN Planner - analyze multiple power supplies to maintain low impedance over entire frequency range dramatically improving product performance

- Fast AC impedance analysis with plane resonance
- Definition of plane size/shape, dielectric constant & plane separation for each on-board power supply
- Extraction of plane data from the integrated Stackup Planner
- Definition of voltage regulator, bypass/decoupling capacitors, mounting loop inductance
- Frequency range up to 100GHz
- Extensive Capacitor Library – over 5,250 capacitors derived from SPICE models

# Losing a Bit of Memory

by Barry Olney

IN-CIRCUIT DESIGN PTY LTD | AUSTRALIA

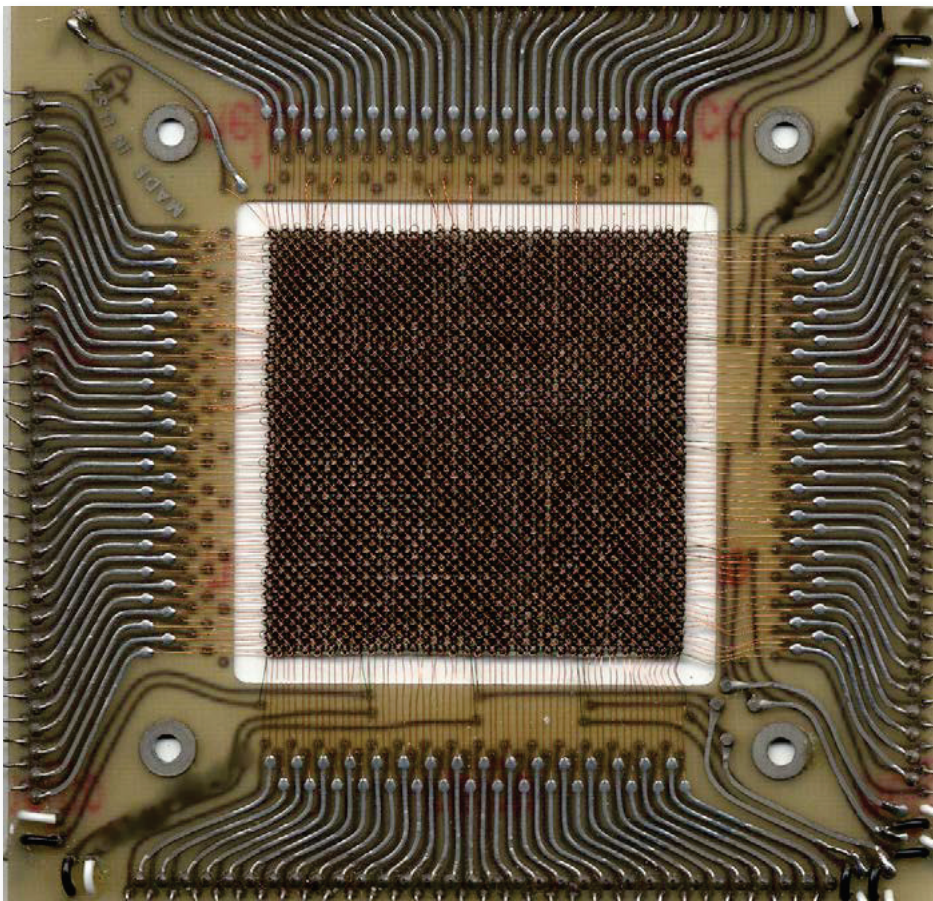
**SUMMARY:** *No matter what type of memory you are designing with, the clock should always have the longest delay. This ensures that the other signals have time to settle before the clock arrives at the device and samples the bus.*

In the early 1980s, when I was working in the Microprocessor Research Lab at the University of Western Australia, we had the opportunity to dismantle an old DEC mainframe that had served its useful purpose. The main reason was to salvage any useable components. Whilst rummaging through the scrap, we found a number of blocks of magnetic core memory. I ex-

tracted one of the cards from a block and found it was made up of thousands of small toroidal magnets that seemed to have three enameled copper wires running through each toroid. This was just one kilobyte of memory. I'm not sure if this is fact, but at the time, I was told that the women of the Fijian Islands sewed the threads of wire, which were used to weave fine fishing nets. Even with my excellent eyesight (at the time), it was difficult to see. An expanded view of the toroidal coils is in Figure 1.

This magnetic core memory was the first random access memory technology. The three wires were X, Y, and a sense/inhibit that ran diagonally through all cores. These wires were used to create the magnetic charge, remove the charge, and to read the state of the charge. And since the sense/inhibit wire ran through the entire matrix, only a single bit could be read at one time. Also, since the process of reading erased the data it held, it was automatically restored after read (write-after-read cycle). It is hard to believe, but core memory was the memory of choice for about 20 years, until semiconductors took over.

Core memory was extremely durable compared to today's technology, as it had no moving parts, was non-volatile and resistant to heat and electromagnetic interference. It was used extensively in the early space shuttles and survived not only the explosion but



**Figure 1:** One kilobyte of magnetic core memory (Source: [www.wikimedia.org](http://www.wikimedia.org)).

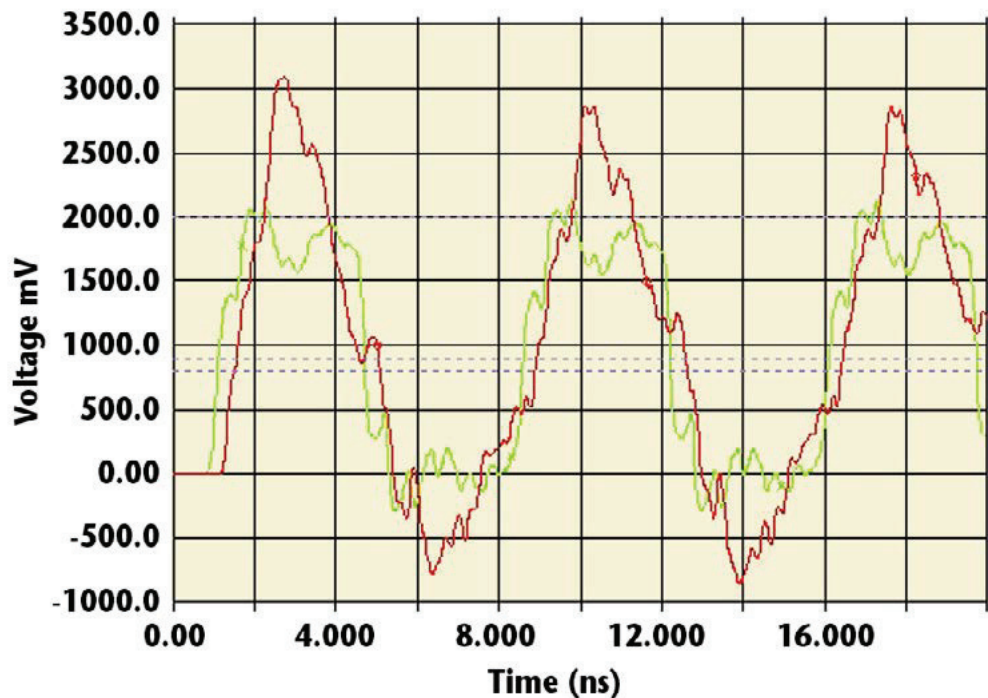
**LOSING A BIT OF MEMORY** *continues*

also the plunge to Earth when the Space Shuttle Challenger exploded shortly after launch in 1986. NASA was able to recover and read the contents of the memory. The shuttle's IBM AP-101 computers originally had a massive 424 kilobytes of magnetic core memory and used a high-level language called HAL/S (what else?).

Today, DRAM is still the memory of choice for computers, but is packaged in multi-gigabyte DIMMs. It is considered random access because you can access any cell directly if you know the row and column that accesses the cell. It still needs to be refreshed as the transistor-capacitor pair loses its charge over time and must be periodically refreshed to retain the cell's data.

The two main drawbacks with DRAM: It is slow, compared to flash memory, and the cells lose their memory when power is removed. Flash memory (as used in USB sticks), on the other hand, retains its data when powered down and is much faster than DRAM, but it requires more silicon real estate, making it more expensive.

Double Data Rate Synchronous Dynamic Random Access Memory (DDR SDRAM), now up to DDR4, uses both the rising and falling edge of the clock to accomplish two data transfers per clock cycle. Of course, this halves the clock frequency and reduces the signal integrity requirements of the PCB layout. Compared to SDRAM (Single Data Rate), DDR makes higher data rates possible by more strict control of the timing of the data and clock signals. But from an engineering point of view, DDR is more difficult to control and route.



**Figure 2:** Clock (green) leads the address (red) by 450ps.

Synchronous buses, as typically used in DDR designs, benefit from an extraordinary immunity to crosstalk. Crosstalk only occurs when the signals are being switched and this crosstalk only has an effect within a small window around the moment of the clocking. So providing the receiver waits sufficiently long enough for the crosstalk to settle, before sampling the bus, the crosstalk has no effect on the signal quality at the receiver.

In-Circuit Design has been doing customer simulations for 10 years now, and one issue that we see constantly is timing skew between clock/address and strobe/data. An example of a design is shown in Figure 2, where the clock arrives at the memory device (NAND Flash in this case) 450ps before the address signal. For some reason, this design worked, although intermittently. Our recommendation was to re-route the clock to ensure it was delayed longer than the address and data signals.

The customer's hardware engineer described the results: "We received our adapter boards yesterday and were able to test the Ethernet connection and load programs into Flash mem-

LOSING A BIT OF MEMORY *continues*

**Figure 3:** Comparison of straight and serpentine traces of the same length. Top, a 12" straight trace (reference trace), with a 12" serpentine trace with close coupling below.

ory. Board #2 now runs very solid, no odd command error traps or program errors. It ran over 5 million IDN queries last night without any errors. It looks very good."

And this brings me to the main point of this article: No matter what type of memory you are using, the clock (or strobe) should always have the longest delay so the other signals have time to settle, before the clock arrives at the device, and samples the bus.

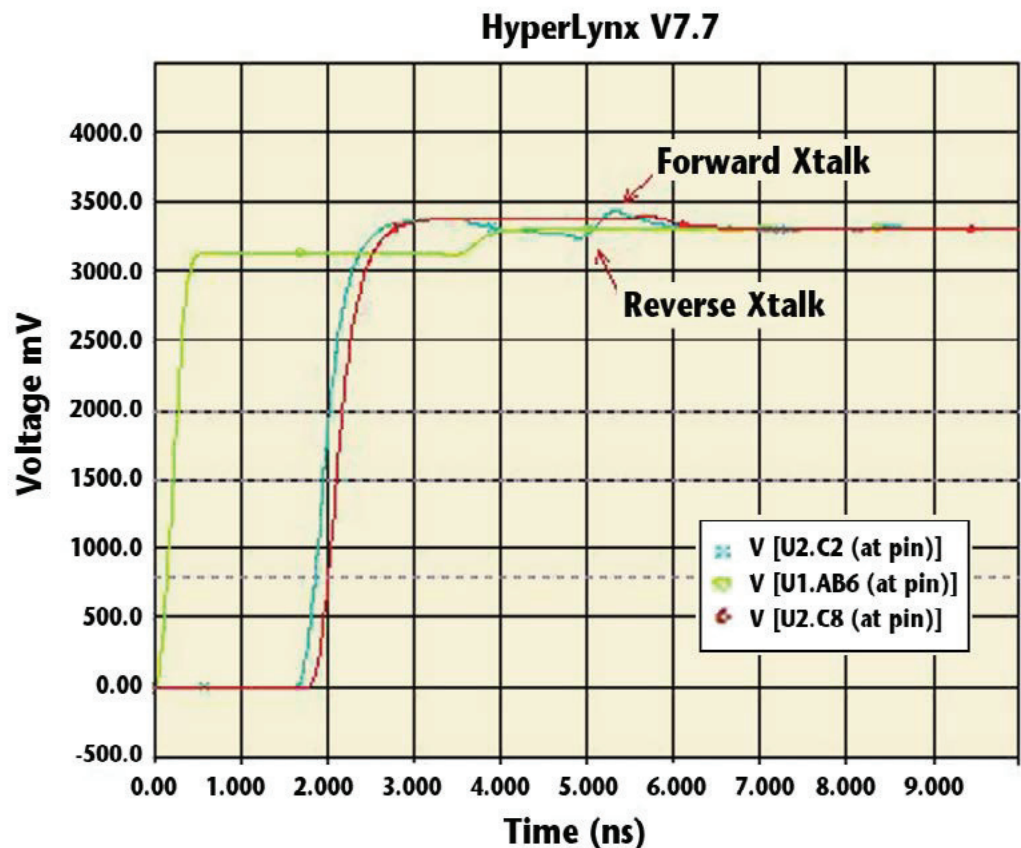
These same principles apply to any memory (although DDR3/4 routing can be accomplished by routing by byte group as well). Routing all signals to the same delay can seem more difficult at first because of the lack of real estate, the tight space to drop vias and the large number of interconnects. However, it is the best way because it makes the signal timing analysis straightforward.

Remember: The clock must have the longest delay, which is not necessarily the longest length.

In a previous column, [Beyond Design: A New Slant on Matched-Length Routing](#), I discussed this issue further.

Matching the lengths does not mean that the propagation delay for each signal will be the same. Also, traces routed to length on different layers exhibit different delays and this is most evident when comparing microstrip (outer layers) to stripline (inner layers). This is due to the difference in dielectric materials surrounding the traces.

Typically, serpentine traces (or meander lines) are used to match the length of critical signals, assuming that the extra length of



**Figure 4:** Closely coupled serpentine trace vs straight trace (microstrip).

the serpentine pattern will be electrically the same as a straight trace and no parasitics are introduced. But as technology advances, and demands for smaller traces with less clearance and faster rise times become more typical, this assumption may no longer be valid.

Contrary to what you may believe, the propagation delay of a serpentine trace is less than the delay through an equivalent length straight trace. The signal is sped up because a portion of the signal will propagate perpendicular to the serpentine. And this varies with the type of serpentine pattern used. For example, the serpentine pattern may have long parallel lengths spaced close together in the 'U' bend coupling the signal many times through the serpentine pattern. This self-coupling (forward and reverse crosstalk) shortens the electrical path.

In Figure 4, green is the driver, red is the straight (reference) trace, and blue is the closely coupled serpentine trace which leads the reference trace by 150ps. The peaks in the blue serpentine trace (from 4 to 6nS) are the reverse and forward crosstalk respectively from the close coupling.

So, although these two traces are routed to exactly the same length, the serpentine trace is 150ps faster than the straight trace. If this serpentine trace were the clock, then it would arrive 150ps before the other signal has settled resulting in an intermittent, unreliable product. This delay should always be confirmed by simulation tools – not by comparison of trace length.

#### Points to remember:

- Magnetic core memory was the first random access memory technology and was the memory of choice for about twenty years until semiconductors took over.
- The two main drawbacks with DRAM are: It is slow, compared to flash memory, and the cells lose their memory when power is removed. Flash memory, on the other hand, retains its data when powered down and is much faster than DRAM, but it requires more silicon real estate, making it more expensive.

- DDR SDRAM uses both the rising and falling edge of the clock to accomplish two data transfers per clock cycle.

- Synchronous buses, as typically used in DDR designs, benefit from an extraordinary immunity to crosstalk.

- A common issue, in memory design, is timing skew between clock/address and strobe/data.

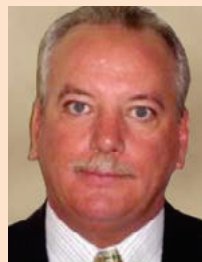
- The clock must have the longest delay, which is not necessarily the longest length.

- The propagation delay of a serpentine trace is less than the delay through an equivalent length straight trace.

- No matter what type of memory you are using, the clock (or strobe) should always have the longest delay so the other signals have time to settle before the clock arrives at the device and samples the bus. **PCBDESIGN**

#### References

1. Advanced Design for SMT – Barry Olney
2. [Beyond Design: Embedded Signal Routing](#) – Barry Olney
3. [Beyond Design: Differential Pair Routing](#) – Barry Olney
4. [Beyond Design: A New Slant on Matched-Length Routing](#) – Barry Olney
5. [Board Level Simulation and the Design Process: Plan B: Post Layout Simulation](#) – Barry Olney
6. [It Was Rocket Science](#)
7. [Space Shuttle](#), Wikipedia
8. [High Speed Digital Design](#) – Howard Johnson
9. JEDEC DDR2 Specification JESD79-2E
10. The ICD Stackup and PDN Planner can be downloaded from [www.icd.com.au](http://www.icd.com.au)



Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. The company is a PCB design service bureau that specializes in board-level simulation, and is the developer of the ICD Stackup Planner and ICD PDN Planner software. Contact Barry [here](#).