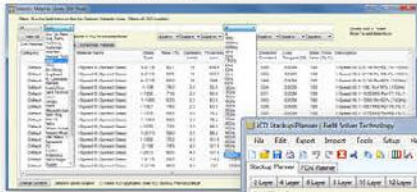


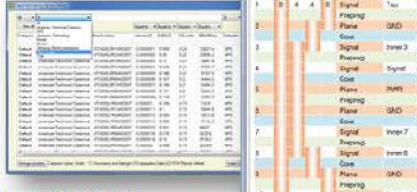
# iCD Design Integrity

incorporates the iCD Stackup and PDN Planner software. Offers PCB Designers unprecedented simulation speed, ease of use & accuracy at an affordable price

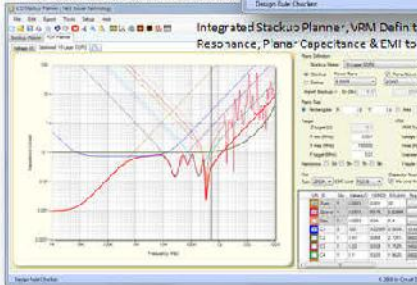
**Dielectric Materials Library**  
30,700 Rigid & Flex Materials to 100GHz



**Extensive Capacitor Library**  
5,650 Decaps Derived from SPICE Models



**iCD PDN Planner**  
AC Impedance Analysis & Plane Resonance



**iCD Stackup Planner**

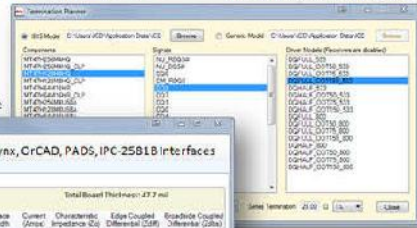
Field Solver Accuracy, Characteristic Impedance, Edge & Broadside Coupled Differential Impedance

Allegro, Altium, Excel, HyperLynx, OrCAD, PADS, IPC-2581B Interfaces

Layer	Via Type	Flow Direction	Description	Layer Name	Material Type	Differential Pairs	Dielectric Constant	Dielectric Loss Tangent	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Ω)	Edge Coupled Differential (dB)	Broadside Coupled Differential (dB)
1	3	4	4	4	Soldermask	PPS4000 PPS3600 (G4-40) HF LPI	3.5	0.0	2.2	17	6	0.88	42.53	87.33	
2			Prepreg	GND	330HR 3500 (R4-35) HF LPI		3.97	0.3	1.4						
3			Core		330HR 51502 (R4-43) HF LPI		4.4	0	1.4						
4			Prepreg		330HR 2150 (R4-21) HF LPI		4.14	0.3	1.4	12	6	0.42	42.70	82.21	37.58
5			Core		330HR 51502 (R4-43) HF LPI		4.4	0	1.4						
6			Prepreg		330HR 1105 (R4-11) HF LPI		3.14	0.3	1.4						
7			Core		330HR 51502 (R4-43) HF LPI		4.4	0	1.4						
8			Prepreg		330HR 2150 (R4-21) HF LPI		4.14	0.3	1.4	12	6	0.42	42.70	82.21	37.58
9			Core		330HR 51502 (R4-43) HF LPI		4.4	0	1.4						
10			Prepreg		330HR 1105 (R4-11) HF LPI		3.97	0.3	1.4						
11			Core		PPS4000 PPS3600 (G4-40) HF LPI		3.5	0.0	2.2	17	6	0.88	42.53	87.33	

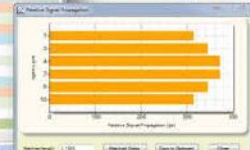
**Termination Planner**

Extracts IV Curves from IBIS Models  
Calculates Series Terminator of the Distributed System Including Loads



**Matched Delay Optimization**

Relative Signal Layer Propagation  
Ideal DDRx Trace Delay Matching



## iCD Stackup Planner

Offers Engineers & PCB Designers unprecedented simulation speed, ease of use and accuracy at an affordable price

- Industry Leading 2D (BEM) Field Solver precision
- Characteristic impedance, edge-coupled & broadside-coupled differential impedance
- Relative Signal Propagation with 'Matched Delay Optimization'—ideal for DDRx design
- Termination Planner - series termination based on IBIS models & distributed system
- Unique Field Solver computation of multiple differential technologies per signal layer
- Extensive Dielectric Materials Library—over 30,700 rigid & flexible materials up to 100GHz
- Interfaces—Allegro, Altium, Excel, HyperLynx, OrCAD, PADS, Zmetrix TDR, Zuken & PC-2581B

## iCD PDN Planner

Analyze multiple power supplies to maintain low AC impedance over entire frequency range dramatically improving product performance

- Fast AC impedance analysis with plane resonance and projected EMI
- Definition of plane size, dielectric constant & plane separation
- Extraction of plane data from the integrated iCD Stackup Planner
- Definition of voltage regulator, bypass/decoupling capacitors, mounting loop inductance
- PDN EMI Plot with FCC, CISPR & VCCI Limits. Frequency range up to 100GHz
- Extensive Capacitor Library—over 5,650 capacitors derived from SPICE models

*"iCD Design Integrity software features a myriad of functionality specifically developed for high-speed design."*

- Barry Olney



# When Legacy Products No Longer Perform

by Barry Olney

IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

As IC die sizes continue to compact due to demand for smaller and faster technology, and as switching speeds continue to improve, rise and fall times are creeping down into the sub-nanosecond realm, a territory previously reserved for microwave engineers. This relentless shrinking trend that perpetuates Moore's Law can create a huge problem for legacy designs as faster switching intensifies signal integrity issues. Over the years, as logic drivers have continued to switch faster and faster, problems with ringing, crosstalk and electromagnetic emissions (EMI) have become progressively worse.

It is a common quandary that established products that have worked flawlessly for years suddenly stop performing reliably, due to a new batch of ICs that is used in the latest production run. The cause of this problem is rise time shrinkage. Figure 1 illustrates the consequences of three different rise times for the same clock frequency.

This example brings home two very important points. Firstly, for a given layout, faster switching produces spurious signals exhibiting excessive overshoot and ringing. This problem is unavoidable. It can only be prevented,

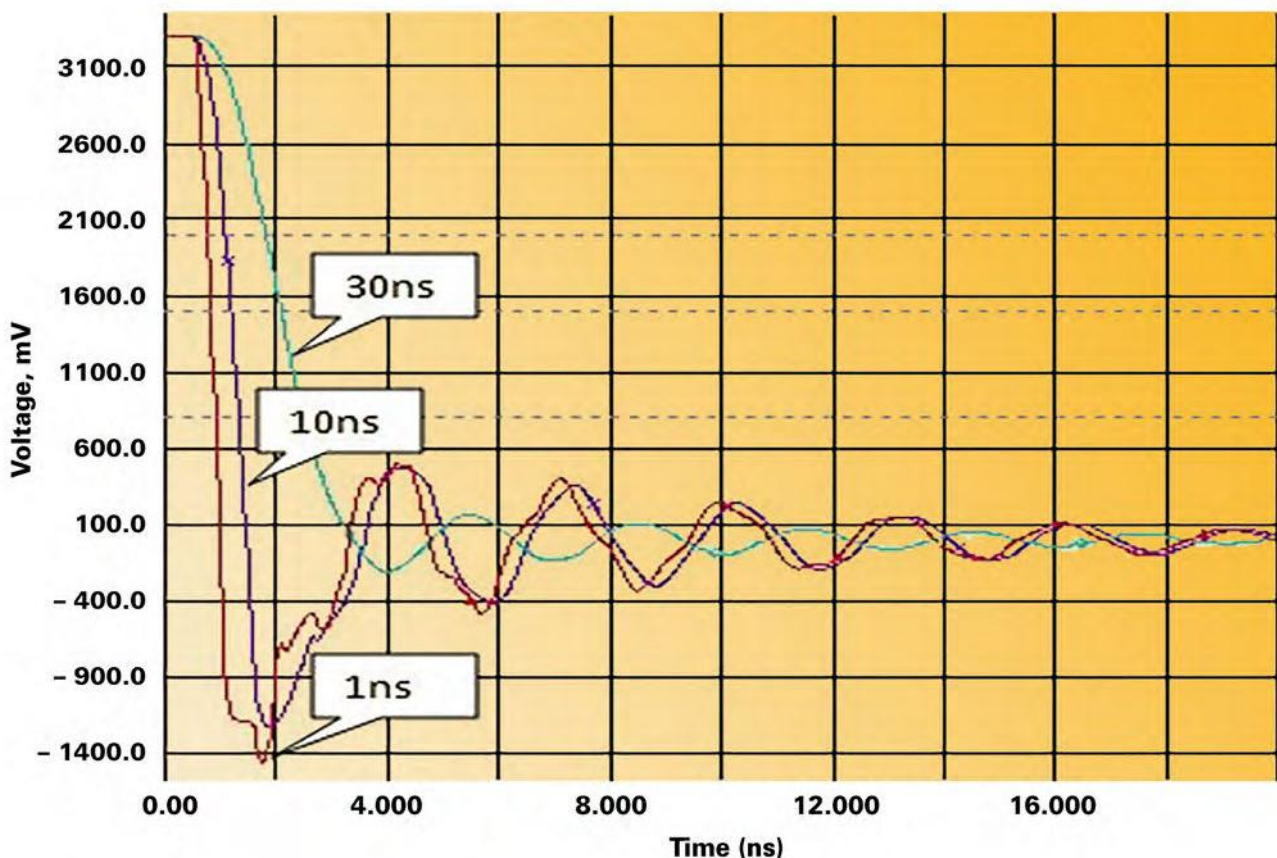


Figure 1: Increased ringing with faster rise times (simulated in HyperLynx).

to some extent, by improving the layout and routing, reducing the number of loads and/or adding terminators. Secondly, IC manufacturers are not always doing us a favor when they begin shipping “new and improved” logic circuits. When substituted into a legacy design, the increase in speed may buy nothing but headaches.

From the perspective of an IC manufacturer, shrinking a die is a winning proposition because the new chip is almost certain to meet or exceed its published specifications at a lower cost. However, from the perspective of the designer, shrinking a die, in an existing product design, can be a daunting prospect, because the new rising and falling edges are almost certain to switch considerably faster.

Faster edge rates mean reflections and signal quality problems. So, even when the package hasn’t changed and the clock speed hasn’t changed, a problem may exist for legacy designs. The enhancements in driver edge rates have a significant impact on signal quality, timing and crosstalk. This also has a direct impact on radiated emissions.

Figure 2 shows the massive increase in emissions from the slowest to the fastest rise time previously discussed. When dealing with subnanosecond rise times, the emissions can easily exceed the FCC/CISPR Class B limits for an unterminated transmission line.

The ratio of signal rise time to physical delay of an interconnect determines how the circuit behaves. A small ratio, meaning a short

rise time compared with the innate time delay of the interconnect, produces distributed behavior. Whereas a large ratio invokes lumped-element behavior that requires little attention. When considering any aspect of your circuit geometry, the relationship between physical size and rise time determines the relative importance of that object in the overall scheme of the circuit. The signal rise time, rather than the signal clock frequency, determines the critical signal speed. Basically, any rise time of 1ns or less may be of concern.

An ideal square wave clock signal with the spectrum of a 50% duty cycle, and a zero picosecond rise time, has frequency components (harmonics) only at multiples of the clock frequency. The Fourier Transform converts a time domain waveform into its spectrum of sine wave frequency components. The amplitude of the even harmonics is zero, as they cancel out in the Fourier Transform due to the even mark-to-space ratio. The amplitude of the odd harmonics is given by:

$$V(\text{harmonics}) = \frac{2}{\pi \cdot n}$$

where n is the odd harmonic number

For example, the amplitude of the 1<sup>st</sup> harmonic, where n = 1, is 2/(3.14 x 1) = 0.64V. The amplitude of the 3<sup>rd</sup> harmonic, n = 3 is 2/(3.14 x 3) = 0.21V. The amplitude of each harmonic

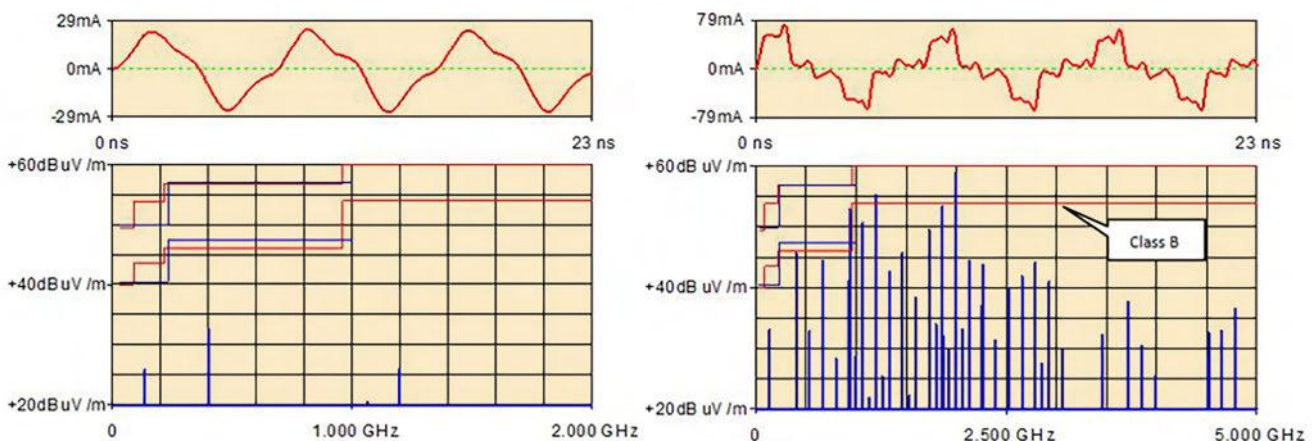


Figure 2: Radiated emissions from the 30ns edge rate (left) and 1ns (right).

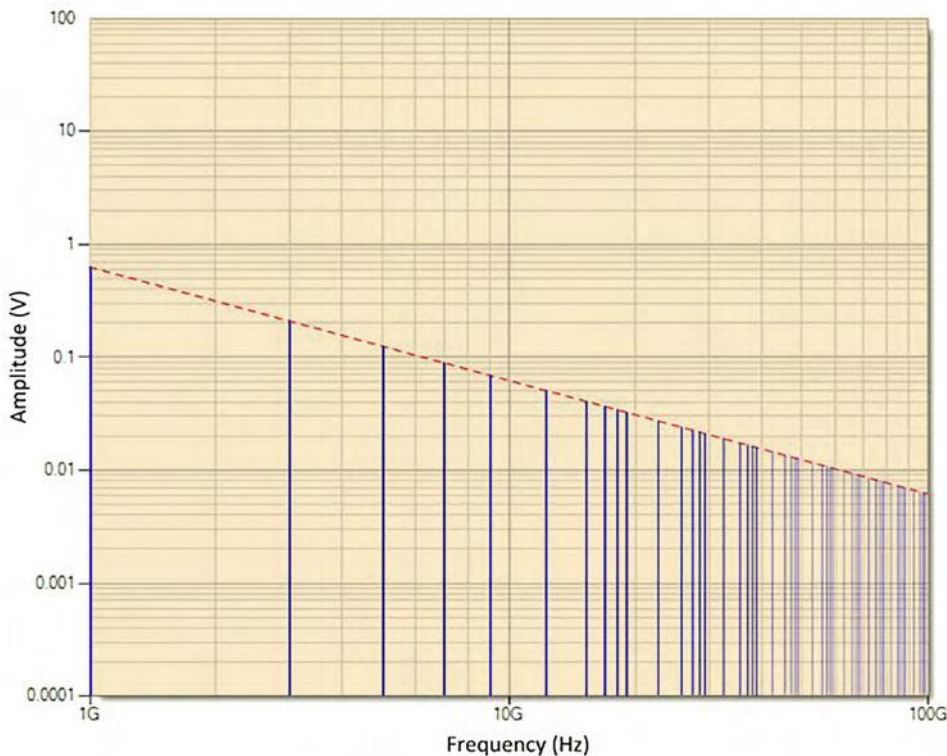


Figure 3: Odd harmonics of a 1GHz fundamental clock.

drops off with the inverse of frequency, since each harmonic is a higher frequency. Figure 3 shows the calculated harmonic amplitudes of an ideal 1GHz clock signal for the odd harmonics up to 100GHz.

However, in practice, the signal rise time has an impact on the maximum signal bandwidth. Understanding the frequency band, that really matters, for digital design is very important. Traditionally, we used  $0.35/\text{Tr}$  (where  $\text{Tr}$  is the rise time in ps) for the upper bandwidth. However, a more accurate approach is to use an upper knee frequency of  $0.5/\text{Tr}$ , which forms a crude but useful translation between time and frequency domains. If, for instance, the rise time is 500ps, which is typical these days, then the upper bandwidth is actually 1GHz regardless of the clock frequency. It is possible to have two different waveforms, with exactly the same clock frequency but different rise times and therefore different bandwidths.

When selecting the most appropriate dielectric materials for a design, one should consider the bandwidth up to the 5<sup>th</sup> harmonic. The bandwidth of an interconnect refers to the high-

est sine wave frequency that can be transmitted by the interconnect without significant loss. For our 1GHz example, the maximum bandwidth to consider is the 5<sup>th</sup> harmonic at 5GHz if the rise time is unknown.

FR-4, the glass epoxy material commonly used for multilayer printed circuit fabrication, has negligible loss at frequencies below 1GHz. But since the dielectric loss is frequency-dependent, at higher frequencies, the dielectric loss of FR-4 increases. So, for high-frequency digital, RF and microwave designs, alternative materials that exhibit lower losses need to be considered. (To

make this selection process easier, over 31,000 rigid and flexible materials, up to 100GHz, can be sourced from the iCD dielectric materials library.)

Electromagnetic emissions arise from each frequency component of the signal. For the worse offender—the common-mode currents—the amount of radiated emissions will increase linearly with frequency. Although the amplitude of each harmonic drops off with the inverse of frequency, the ability to radiate increases linearly, so all harmonics contribute equally to EMI. To minimize EMI, the design goal is to use the absolute lowest bandwidth possible whilst still maintaining the specified data throughput.

Any ringing in the circuit may increase the amplitude of higher-frequency components and thus increase the magnitude of radiated emissions. High-frequency harmonics can also beat with the resonant frequency of the plane pairs, as they approach half wave length, creating a rough wave effect which, in extreme cases, can cause total system failure. This is the reason why solving signal integrity issues is always the best starting place to minimizing EMI.

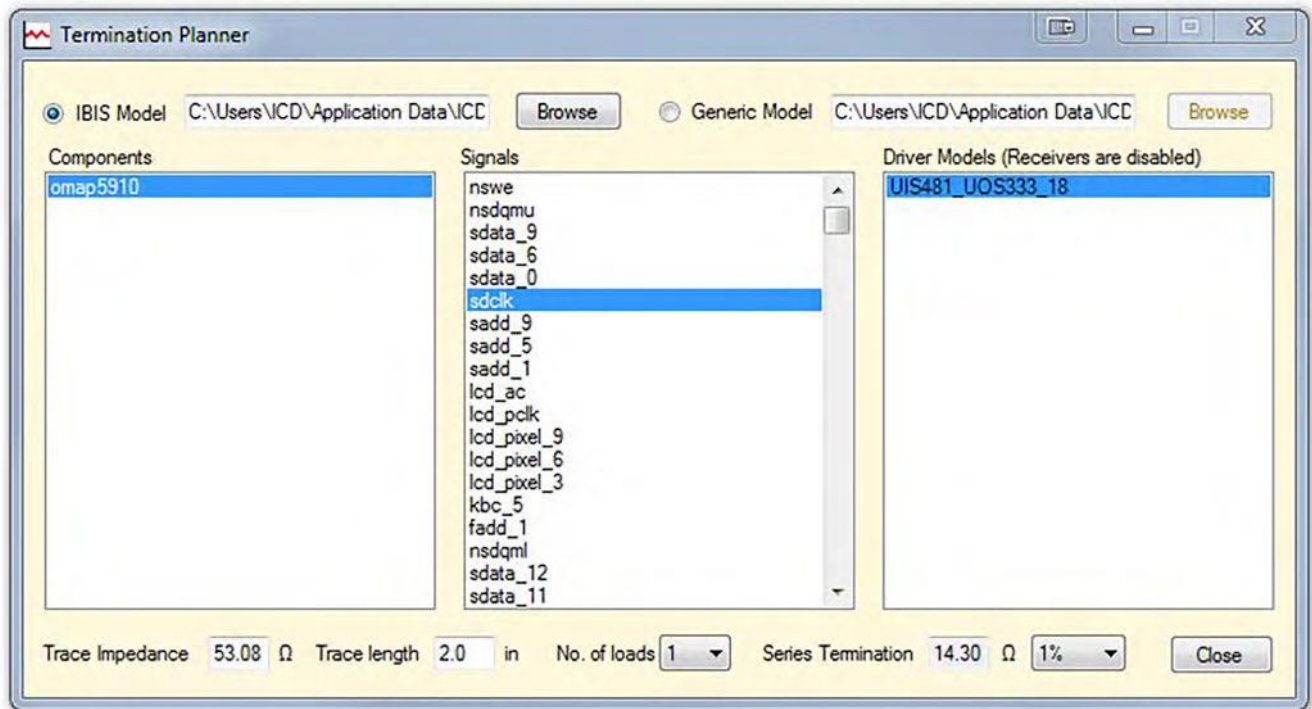


Figure 4: Series terminator value determined for an FPGA clock (source: iCD Design Integrity).

To improve signal integrity, hence EMI, one needs to slow down the rise time of the signal to reduce the high-frequency components. This is easily achieved by placing a termination resistor in series with the transmission line at the source. The value of this terminator is determined by extracting the IV curves from the IC IBIS model, and then the required series termination resistance is calculated, based on a distributed system, to match the transmission line for the selected layer as shown in Figure 4. So, to fix that legacy product that now exhibits intermittent operation, simply add a series terminator. In fact, it is always good design practice to allow space for a series terminator by adding a zero-ohm resistor to the critical interconnects to future-proof the design.

### Points to Remember:

- Faster switching intensifies signal integrity issues by producing spurious signals exhibiting excessive overshoot and ringing. This also has a direct impact on radiated emissions.
- Established products can suddenly stop performing reliably due to a new batch of ICs. The cause of this problem is rise time shrinkage.

- Even when the package hasn't changed and the clock speed hasn't changed, a problem may exist for legacy designs.
- The emissions from sub-nanosecond rise times, can easily exceed the FCC/CISPR Class B limits for an unterminated transmission line.
- The ratio of signal rise time to physical delay, of an interconnect, determines how the circuit behaves.
- An ideal square wave clock signal has frequency components only at odd multiples of the clock frequency.
- In practice, the signal rise time has an impact on the maximum signal bandwidth.
- The upper knee frequency of  $0.5/Tr$ , forms a translation between time and frequency domains.
- When selecting the most appropriate dielectric materials for a design, one should consider the bandwidth up to the 5<sup>th</sup> harmonic.
- For high-frequency digital, RF and microwave design alternative materials that exhibit lower losses need to be considered.
- Although the amplitude of each harmonic drops off with the inverse of frequency, the ability to radiate increases linearly—so all harmonics contribute equally to EMI.

- High-frequency harmonics can beat with the resonant frequency of the plane pairs creating a rough wave effect which can cause total system failure

- Solving signal integrity issues is always the best starting place to minimizing EMI.

- To improve signal integrity, hence EMI, one needs to slow down the rise time of the signal to reduce the high-frequency components. This is easily achieved by placing a termination resistor in series with the transmission line at the source.

- It is always good design practice to allow space for a series terminator by adding a zero-ohm resistor to the critical interconnects to future-proof the design. **PCBDESIGN**

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2. Eric Bogatin, Signal and Power Integrity Simplified, [Rule of Thumb #1: Bandwidth of a signal from its rise time.](#)

3. Howard Johnson, Martin Graham. [High-speed Digital Design.](#)



**Barry Olney** is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN and CPW Planner. The software can be downloaded from [www.icd.com.au](http://www.icd.com.au). To read past columns, [click here](#).

## Simultaneous Design and Nanomanufacturing Speeds Up Fabrication

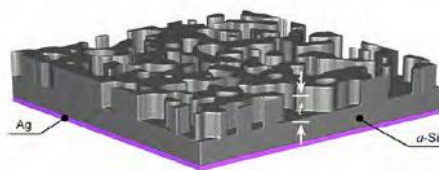
Design and nanomanufacturing have collided inside a Northwestern University laboratory.

An interdisciplinary team of researchers has used mathematics and machine learning to design an optimal material for light management in solar cells, then fabricated the nanostructured surfaces simultaneously with a new nanomanufacturing technique.

"We have bridged the gap between design and nanomanufacturing," said Wei Chen, the Wilson-Cook Professor in Engineering Design and professor of mechanical engineering in Northwestern's McCormick School of Engineering.

"The concurrent design and processing of nanostructures paves the way to avoid trial-and-error manufacturing, increasing the cost effectiveness to prototype nanophotonic devices," said Teri Odom, Charles E. and Emma H. Morrison Professor of Chemistry in Northwestern's Weinberg College of Arts and Sciences.

Researchers are currently interested in nanophotonic materials for light absorption in ultrathin, flexible solar cells. The same



principle could also be applied to implement color into clothing without dyes and to create anti-wet surfaces. For solar cells, the ideal nanostructure surface features quasi-random structures, meaning the structures appear random but do have a pattern.

To bypass the issues of nano-lithography, Odom and Chen manufactured the quasi-random structures with wrinkle lithography, a new nanomanufacturing technique that can rapidly transfer wrinkle patterns into different materials to realize a nearly unlimited number of quasi-random nanostructures.

"Importantly, the complex geometries can be described computationally with only three parameters — instead of thousands typically required by other approaches," Odom said. "We then used the digital designs in an iterative search loop to determine the optimal nanowrinkles for a desired outcome."

Next, the team plans to apply its method to other materials, such as polymers, metals, and oxides, for other photonics applications.