

# BOARD LEVEL SIMULATION SPECIALISTS

ICD Stackup Planner - offers engineers/PCB designers unprecedented simulation speed, ease of use and accuracy at an affordable price

- 2D (BEM) field solver precision
- Characteristic impedance, edge-coupled & broadside-coupled differential impedance
- Unique field solver computation of multiple differential technologies per stackup
- Heads-up impedance plots of signal and dielectric layers
- User defined dielectric materials library - over 16,250 materials up to 100GHz

ICD PDN Planner - analyze multiple power supplies to maintain low impedance over entire frequency range dramatically improving product performance

- Fast AC impedance analysis with plane resonance
- Definition of plane size/shape, dielectric constant & plane separation for each on-board power supply
- Extraction of plane data from the integrated Stackup Planner
- Definition of voltage regulator, bypass/decoupling capacitors, mounting loop inductance
- Frequency range up to 100GHz
- Extensive Capacitor Library – over 5,250 capacitors derived from SPICE models

# Learning the Curve

by Barry Olney

IN-CIRCUIT DESIGN PTY LTD



Currently, power integrity is just entering the mainstream market phase of the technology adoption life cycle. The early market is dominated by innovators and visionaries who will pay top dollar for new technology, allowing complex and expensive competitive tools to thrive. However, the mainstream market waits for the technology to be proven before jumping in. Power distribution network (PDN) planning was previously overlooked during the design process, but it is now becoming an essential part of PCB design. But what about the learning curve? The mainstream market demands out-of-the-box, ready-to-use tools.

The mainstream market, representing more than 65% of the total EDA software market, wants established technology at an affordable

price. The majority of high-end tools require a PhD to drive. However, the mainstream market demands tools that are intuitive and can be used by any member of the development team from EEs to PCB designers to achieve quick results.

Inadequate power delivery can exhibit intermittent signal integrity issues. These include high crosstalk and excessive emission of electromagnetic radiation, degrading performance and reliability of the product. The PDN must accommodate variances of current transients with as little change in power supply voltages as possible. So the goal of PDN planning is to design a stable power source for all the required power supplies. As with stackup planning, the PDN design is required before a single IC is placed on the board.

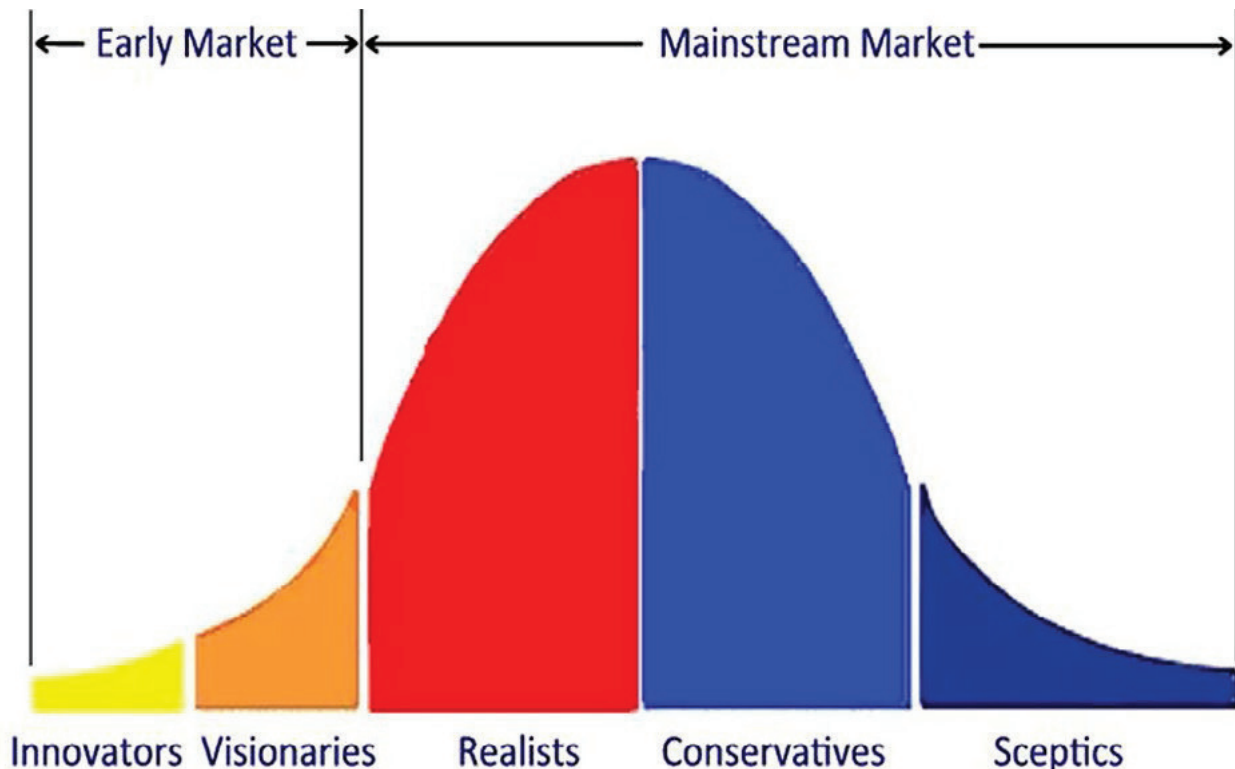


Figure 1: Technology adoption life cycle (Geoffrey A. Moore's Crossing the Chasm).

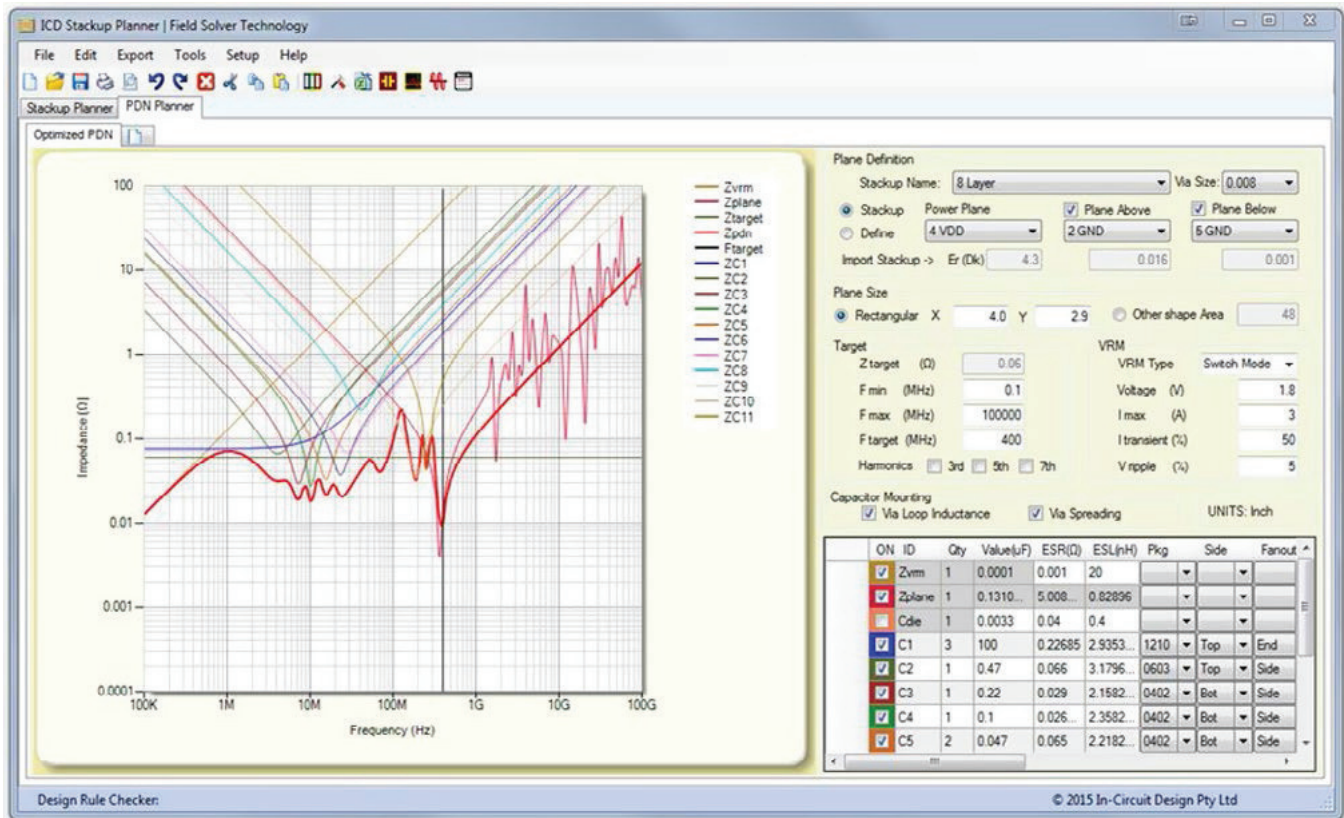
LEARNING THE CURVE *continues*

Figure 2: PDN with optimized decoupling.

Also, the same PDN connections (planes) that are used to transport high-transient currents are used to carry the return currents for critical signal transmission lines. If high-frequency switching noise exists on the planes, coupling may occur, resulting in ground bounce, bit failure or timing errors. Many failures to pass electromagnetic compliance (EMC) are due to excessive noise on the PDN coupling into external cables and radiating emissions.

If you are not familiar with a PDN plot (AC impedance vs. frequency), it can be awfully daunting at first. Figure 2 shows the ICD PDN Planner with a typically 400MHz fundamental frequency and with an optimized capacitor selection. Please refer to my previous series [PDN Planning and Capacitor Selection](#) to understand the effects of bypass and decoupling capacitors on the PDN, as this column will focus on the plane resonance.

The AC impedance (thick red curve) should be below the target impedance up to the maxi-

mum bandwidth. For a 400MHz fundamental frequency, the maximum bandwidth is 2GHz to take in the 5<sup>th</sup> harmonic. But I am frequently asked one question: Does it have to be low all the way up to 2GHz?

In Figure 2, you will notice the ringing in the top right corner of the plot. This is the plane resonance. As the frequency approaches half wavelength, the planes (power and ground) act as an unterminated transmission line and start to resonate. This resonance is not a problem unless it falls on the fundamental frequency or one of the odd harmonics. A Fourier series expansion of a square wave is made up of a sum of odd harmonics. If the waveform has an even mark-to-space ratio then the even harmonics cancel.

Figure 3 illustrates the typical electromagnetic (EM) radiation spectrum analyzer plot for a 400MHz DDR2 data signal. The fundamental frequency generally has little radiation, but then increases up to the 5<sup>th</sup> harmonic and re-

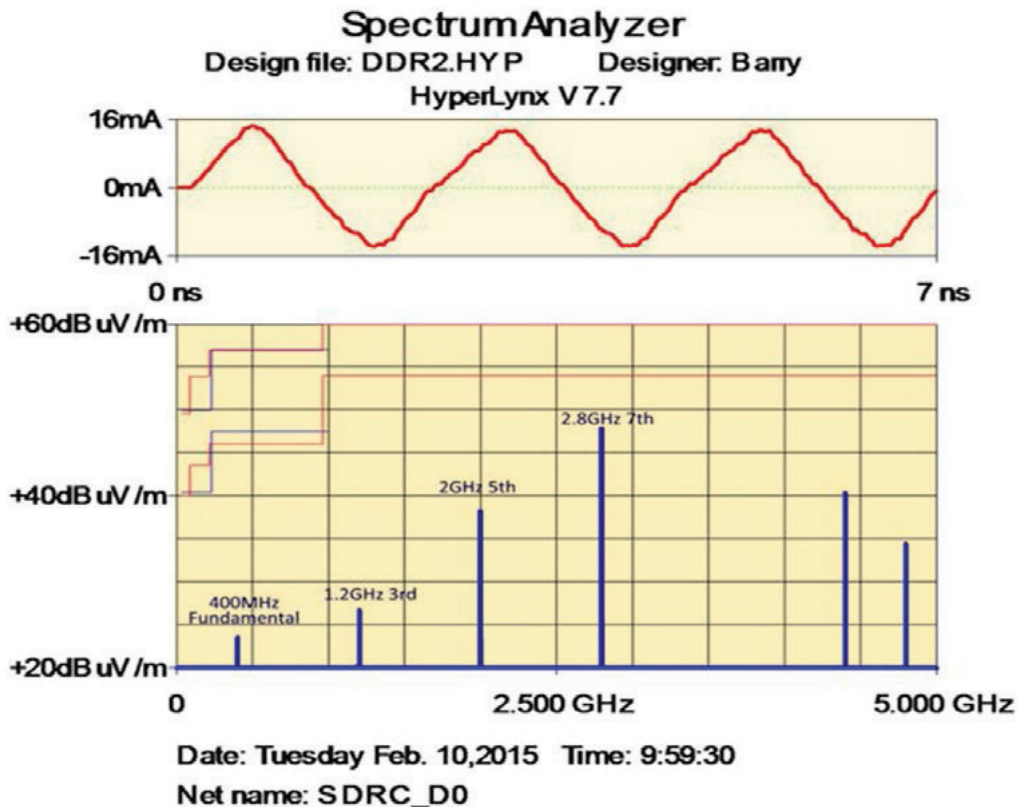


Figure 3: EM radiation from a DDR2 data signal @ 400MHz.

duces again with the higher harmonics. But I have seen cases where even the 11<sup>th</sup> harmonic—4.4GHz in this instance—can create problems.

So what does this EM radiation have to do with the PDN analysis? If the AC impedance is high at the fundamental frequency or at any of the odd harmonics, then the board will radiate. In Figure 4, I have superimposed the EM radiation on the PDN plot. Look at where both the radiation and plane resonance peak. If these coincide, then you will have excessive radiation at that particular frequency. In this case, the fundamental 400MHz has a very low impedance so it will not be an issue. But, the 7<sup>th</sup> harmonic is high and the 5<sup>th</sup> is borderline. Fortunately, the amplitude diminishes as the frequency decreases.

I have pointed out a possible issue on the 5<sup>th</sup> and 7<sup>th</sup> harmonics in Figure 4, so how do we fix it? Decoupling capacitors are only effective below 1GHz, so no matter how many are added, to the PDN, they will not reduce the 2 and

2.8GHz peaks. However, above 1GHz, there are a number of ways to reduce the AC impedance:

1. On-die capacitance. Capacitors are placed on the IC itself by the manufacturer and generally cannot be changed. However, in some cases, the capacitors are on the top of the IC. It may be possible to piggyback parallel capacitors to increase their effect.

2. Reduce the loop inductance of the decoupling capacitors. This can be achieved by moving the decaps to the top side of the board so that the fanout vias have less distance to travel to the power and ground planes in the substrate. The loop inductance can also be reduced by using multiple vias per land and spacing them close to each other to reduce the loop area. But this reduced inductance has minimal effect above 1GHz.

3. Select a material with lower dielectric constant. This will push the plane resonance to a higher frequency.

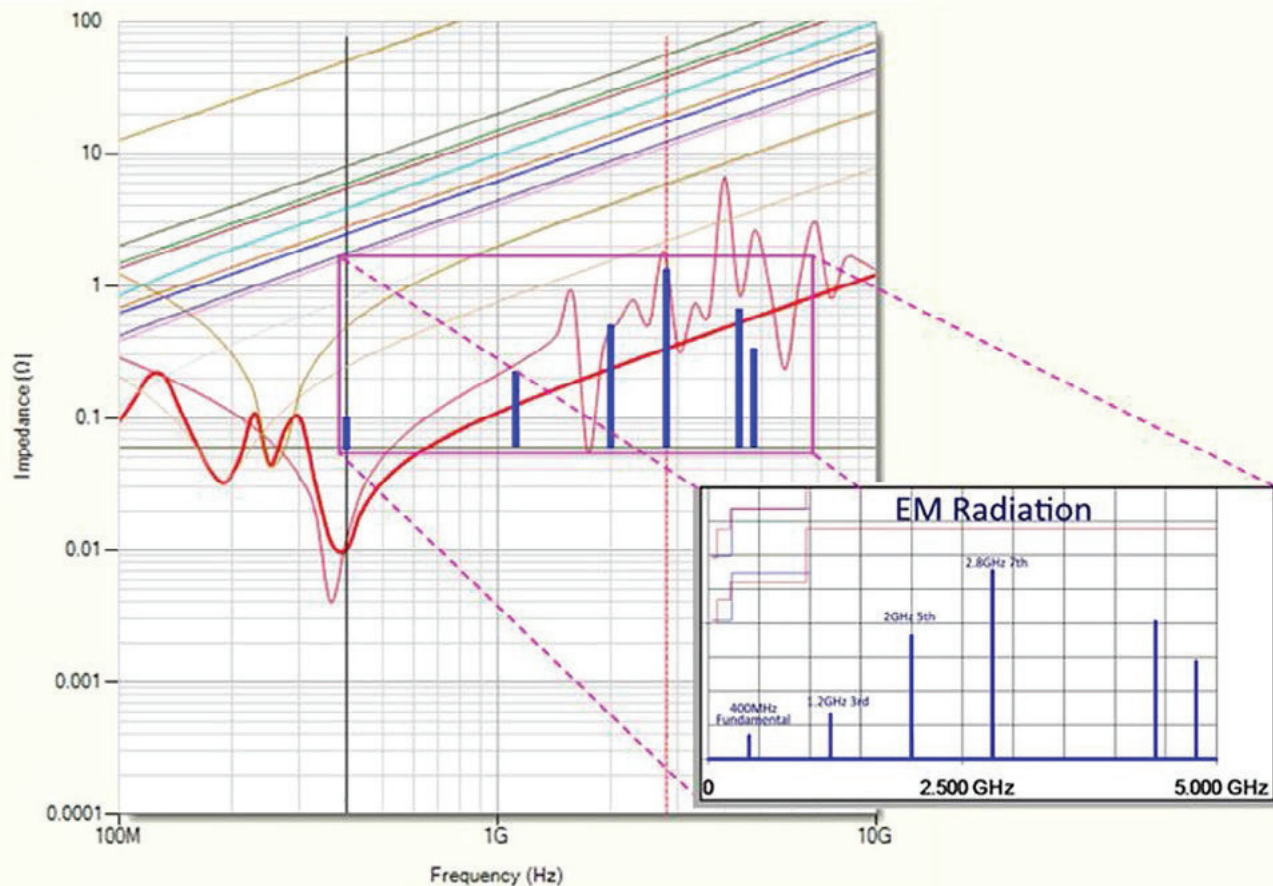
LEARNING THE CURVE *continues*

Figure 4: EM radiation overlapped on the PDN plane resonance.

4. Increase the planar capacitance. This is where the tight integration between the ICD Stackup Planner and PDN Planner comes into play. You can add, say, 3M embedded capacitance materials between the planes and then import this stackup back into the PDN Planner. This material typically has 20nF/in<sup>2</sup> capacitance and significantly reduces the AC impedance above 1GHz. Ultra-thin laminates are very expensive, but another option is to put two plane pairs, of twice the dielectric thickness, in parallel to achieve the same effect at a lower cost.

5. Modify the plane area (capacitance). Obviously, a DDR2 1.8V plane will not cover the entire area of the board. By reducing this area to as small as possible (2-square inches) the self-resonance of the plane will be moved up in frequency, reducing the AC impedance at the higher frequency and shifting the peaks. Reduc-

ing the plane area however, will also reduce the overall attenuation by increasing the characteristic impedance. Also, keep the area as square as possible. If you create a thin rectangular shape, then the plane resonances will increase due to the different standing wave ratios of the X and Y directions being uneven, thus creating more parallel resonance peaks.

The optimization of the PDN is a trial-and-error process that needs to be done in conjunction with the stackup materials to fully exploit all avenues. Suppressing the plane resonance peaks at the odd harmonics, to provide a low impedance profile at higher frequencies, also helps to minimize electromagnetic emissions.

#### Points to Remember

- The mainstream market waits for the tech-

nology to be proven before jumping in.

- This market, representing more than 65% of the total EDA software market, wants established technology at an affordable price.

- Inadequate power delivery can exhibit intermittent signal integrity issues.

- The PDN must accommodate variances of current transients with as little change in power supply voltages as possible.

- The AC impedance should be below the target impedance up to the maximum bandwidth (5<sup>th</sup> harmonic).

- As the frequency approaches half wavelength, the planes act as an unterminated transmission line and start to resonate. This resonance is not a problem unless it falls on the fundamental frequency or one of the odd harmonics.

- The fundamental frequency generally has little radiation but then increases up to the 5<sup>th</sup> harmonic and reduces again with the higher harmonics.

- If the AC impedance is high at the fundamental frequency or at any of the odd harmonics, the board will radiate.

- Above 1GHz, there are a number of ways to reduce the AC impedance. The most effective being increasing planar capacitance and modifying the plane area. **PCBDESIGN**

#### References:

1. Barry Olney's Beyond Design columns: [PDN Planning and Capacitor Selection, Part 1](#) & [Part 2](#); [Power Distribution Network Planning](#)

2. Geoffrey Moore: [Crossing the Chasm](#)  
For information on the ICD Stackup and PDN Planner, [click here](#).



Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. The company developed the ICD Stackup Planner and ICD PDN Planner software, is a PCB Design Service Bureau and specializes in board level simulation. To read past columns, or to contact Olney, [click here](#).

## Breakthrough in Thermoelectric Materials

French physicist Jean Charles Athanase Peltier discovered a key concept necessary for thermoelectric (TE) temperature control in 1834. His findings were so significant that TE devices are now commonly referred to as Peltier devices. Since his work, there have been steady advancements in materials and design. Despite the technological sophistication Peltier devices, they are still less energy efficient than traditional compressor/evaporation cooling.

In the 1960s, Peltier devices were primarily made from Bismuth-Telluride (Bi<sub>2</sub>Te<sub>3</sub>) or Antimony-Telluride (Sb<sub>2</sub>Te<sub>3</sub>) alloys and had a peak efficiency (zT) of 1.1, meaning the electricity going in was only slightly less than



the heat coming out. Since the 1960s there have been incremental advancements in alloy technology used in Peltier devices.

TE alloys are special because the metals have an incredibly high melting point. Instead of melting the metals to fuse them, they are combined through a process called sintering which uses heat and/or pressure to join the small, metallic granules.

The applications for such a material are abundant. As new fabrication techniques are developed, Peltier cooling devices may be used in place of traditional compression refrigeration systems. More importantly, as electrical vehicles and personal electronic devices become more ubiquitous in our daily lives, it is becoming increasingly necessary to have more efficient systems for localized electrical power generation and effective cooling mechanisms. This new thermoelectric alloy paves the way for the future of modern TE devices.