

Interconnect Impedance

Beyond Design

by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

Arguably, the most critical factor in high-speed PCB design is the impedance of the interconnect. We know that transmission line drivers must be matched to the impedance of the line for the perfect transfer of energy. Energy is never lost but rather transforms into other forms of energy. Specifically, in the case of an unmatched transmission line, energy can be transferred into heat, coupled into adjacent elements, reflected, or radiated. In this month's column, I will look at why interconnect impedance is so important to the correct performance of the system.

Impedance is an extension of the definition of resistance to alternating currents (AC). Impedance includes both resistance (the opposition of the electric current) and reactance (the measure of opposition as the current alternates). Reactance also includes the effects that vary with frequency due to distributed parasitic inductance and capacitance of the transmission line.

Impedance is at the core of the methodology that is used to solve signal integrity issues:

1. Signal quality issues arise because voltage signals reflect and are distorted whenever the impedance changes along a transmission line.

2. Crosstalk arises from the coupling of electric and magnetic fields between adjacent traces or coupling between traces and return paths. The inductance and capacitance between the traces establish an impedance, which determines the amount of coupling.
3. Differential mode propagation can be converted to common mode by parasitic capacitance or any imbalance caused by impedance variation, signal skew, rise/fall time mismatch, or asymmetry in the channel. Common mode currents are the main source of electromagnetic radiation.

Not only are the problems associated with the signal integrity best described by the use of impedance, but the solutions and design methodology for good signal integrity are also based on the use of impedance. The two key processes—modeling and simulation—are based on converting electrical properties into an impedance and then analyzing the impact of that impedance on the signals.

The iCD Stackup Planner in Figure 1 illustrates the three most common transmission line structures of a multilayer PCB. For embedded

UNITS: mil		12/2/2019										Total Board Thickness: 44.2 mil					
Layer No.	Via Span & Hole Diameter	Description	Layer Name	Material Type	Differential Pairs >	50/100 Digital	40/80 DDR3	90 USB	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)
		Soldermask		PSR-4000 HFX Satin / CA-40 HF LPI					3.5	0.5							
1	8 8 4 4	Signal	Top	Conductive							2.2	12	4	0.43	51.67	98.65	Embedded Microstrip
		Prepreg		370HR; 1080; Rc= 66% (1GHz)					3.97	2.9							
2		Plane	GND	Conductive							1.4						
		Core		370HR; 1-7628; Rc=42% (1GHz)					4.4	7							Asymmetric Stripline
3		Signal	Inner 3	Conductive							1.4	10	4	0.31	53.26	99.85	
		Prepreg		370HR; 7628; Rc= 50% (1GHz)					4.19	8							
4		Plane	PWR	Conductive							1.4						
		Core		370HR; 1-1652; Rc=43% (1GHz)					4.4	5							
5		Signal	Inner 5	Conductive							1.4	16	4	0.31	51.23	99.63	Dual 48.89
		Prepreg		370HR; 2116; Rc= 56% (1GHz)					4.14	4.8							Symmetric
6		Signal	Inner 6	Conductive							1.4	16	4	0.31	51.23	99.63	Stripline 48.89
		Core		370HR; 1-1652; Rc=43% (1GHz)					4.4	5							
7		Plane	GND	Conductive							1.4						

Figure 1: Embedded microstrip, asymmetric, and dual symmetric stripline configurations.

microstrip (solder mask coated microstrip), the electromagnetic field propagates partially in the dielectric material, solder mask, and air. Whereas in both stripline structures, the electromagnetic field propagates in the dielectric material sandwiched between the planes.

Interconnect impedance is a function of the geometry of the conductors and the dielectric constant of the material adjacent to or separating them. For PCB traces, the most critical dimension is the ratio of trace width to height above/below the reference plane(s). Impedance is also inversely proportional to the square root of the dielectric constant. Clearly, the accurate control over impedance requires precise management of both the physical geometries and the material characteristics along the entire length of the interconnect.

Figure 2 illustrates the variation of impedance with the three most influential variables: trace width, dielectric thickness, and dielectric constant. These impedance plots were simulated by multiple passes of the field solver in the iCD Stackup Planner. Note that the microstrip impedance (top row) varies almost twice as much as the stripline impedance (bottom row) to the same changes in the variables. Conse-

quently, microstrip transmission lines are more vulnerable to change in impedance, which is another good reason not to route critical signals on the outer layers. Any slight variation in any of the total of five variables (including copper thickness and differential clearance) will dramatically change the localized impedance of a microstrip interconnect. These are physical properties of the multilayer PCB that the fabricator must control to maintain a constant impedance.

Having a PCB fabricated to controlled impedance specifications does not necessarily control the impedance of your routed traces; it only controls the impedance of the test coupons. Only you can control the impedance of the signal interconnect. As technology progresses, developers are specifying controlled impedance boards more frequently. The PCB fabricator does their best to control the impedance, of the bare board, given all the manufacturing variables. The fabricator will initially predict the stackup trace impedance using a field solver. They should then place impedance test coupons on the outer edge of the PCB to check that the manufactured product matches the predicted impedance using a time-domain reflectometer (TDR).

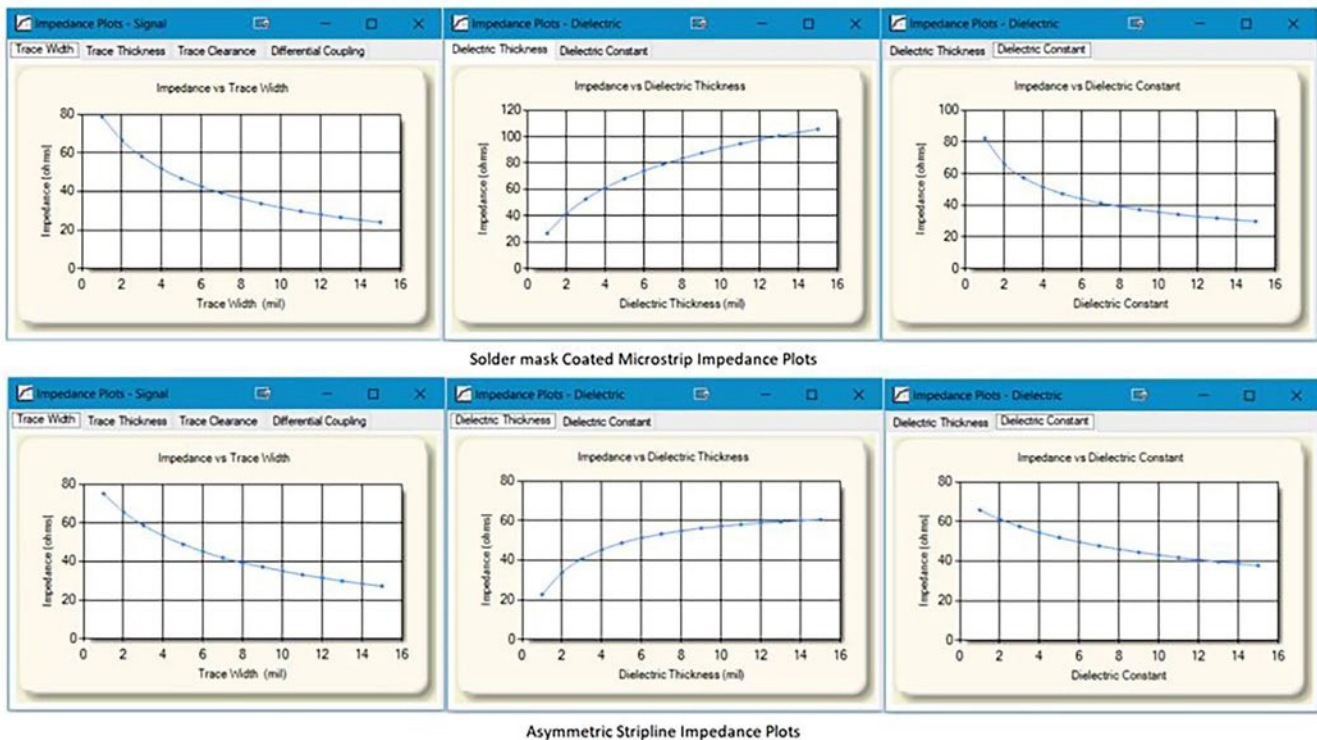


Figure 2: Comparison of microstrip and stripline impedance variations. (Source: iCD Stackup Planner)

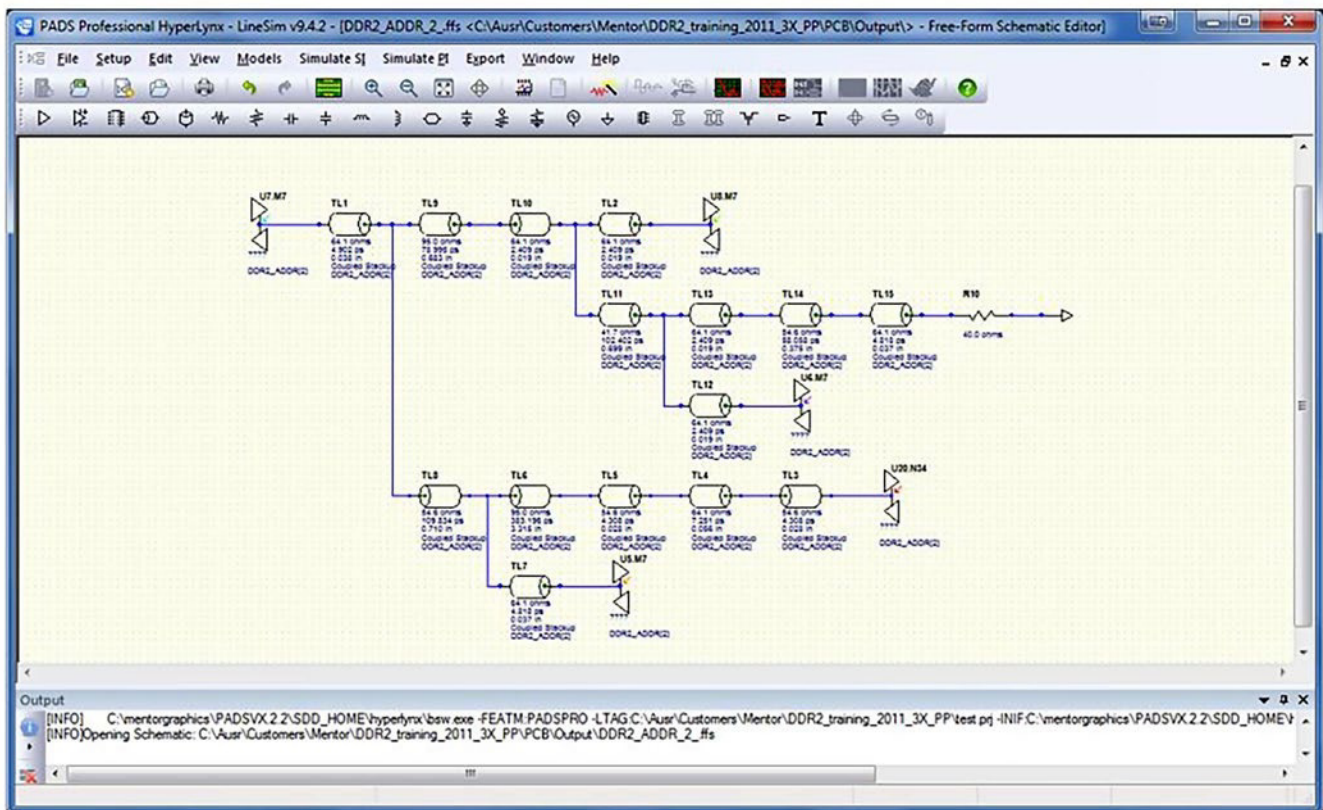


Figure 3: Free-form schematic model of a DDR2 address signal (simulated in HyperLynx).

Impedance variations along the transmission line are much more critical than a precise value of impedance. A flat impedance profile is vital, and it is the PCB designer's responsibility to ensure that there is no impedance discontinuity due to inadequate signal routing. Unfortunately, differential mode propagation can be converted to common mode by any imbalance caused by impedance variation.

Having a PCB fabricated to controlled impedance specifications does not necessarily control the impedance of your routed traces; it only controls the impedance of the inactive test coupons. The impedance test coupons do not take into account all of the possible issues that can occur throughout the maze of routing from driver to load. Only you can control the impedance of the signal interconnect. If you extract the interconnect topology (Figure 3), from a PCB layout to free form schematic models, the result can be terrifying—not quite that simple trace that was routed. In this case, any of the 15 individual transmission lines that form the entire interconnect can create issues if incorrectly routed.

The key to controlled impedance design is to maintain consistency along the entire length of the interconnect, providing a flat impedance profile.

1. Reflections occur whenever the impedance of the transmission line changes along its length. This can be caused by unmatched drivers/loads, layer transitions, dissimilar dielectric materials, stubs, vias, connectors, and IC packages. Terminate transmission lines, avoid layer transitions that don't have a common reference plane, and reduce the length of stubs.
2. These reflections augment crosstalk that is caused by close coupling of signal traces to other structures. Designers should couple traces close to the reference plane, avoid long parallel trace segments, and increase spacing to aggressor signals.
3. There are a number of recommendations to control skew caused by a glass-weave effect. But the simplest by far is to use two combined layers of 1067-style prepreg dielectric material between the signal and

reference plane. This ensures a constant percentage of resin to glass fiber in the dielectric material and controls the comparative propagation delay to < 2 ps/12 in.

4. Signal skew also occurs when differential pairs are not properly matched. Differential skew refers to the time difference between the two single-ended signals in a differential pair. Any mismatch in delay will result in changing part of the differential signal into common-mode current. If there is a mismatch (e.g., on a bend), it should be balanced by lengthening the appropriate trace where the bend occurs.
5. Do not route critical signals on the outer (microstrip) layers, as these are more vulnerable to change in impedance and also difficult for the fabricator to control the plating thickness.
6. Avoid placing copper pours next to signal traces, as the copper pour will lower the impedance on the adjacent trace segment. Use three times the dielectric height as an effective copper pour to trace clearance rule.

Establishing comprehensive design constraints can prevent many of the above issues from occurring in the first place and will certainly warn you when not enforced, depending on the level of your tool's electrical rule checking (ERC). (In addition, you could download the free HyperLynx DRC add-on, which can be used to identify PCB design issues affecting EMC and signal and power integrity.)

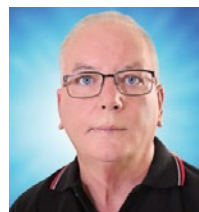
Key Points

- Energy is never lost but rather transforms into other forms of energy
- An unmatched transmission line's energy can be transferred into heat, coupled into adjacent elements, reflected or radiated
- Impedance is at the core of the methodology that is used to solve signal integrity issues
- Interconnect impedance is a function of the geometry of the conductors and the dielectric constant of the material adjacent to or separating them

- The most critical dimension is the ratio of trace width to height above/below the reference plane(s)
- Microstrip transmission lines are more vulnerable to change in impedance, which is another good reason not to route critical signals on the outer layers
- Impedance variations along the transmission line are much more critical than a precise value of impedance
- A flat impedance profile is vital, and it is the PCB designer's responsibility to ensure that there is no impedance discontinuity due to inadequate signal routing
- Having a PCB fabricated to controlled impedance specifications does not necessarily control the impedance of your routed traces; it only controls the impedance of the inactive test coupons
- The key to controlled impedance design is to maintain consistency along the entire length of the interconnect, providing a flat impedance profile **DESIGN007**

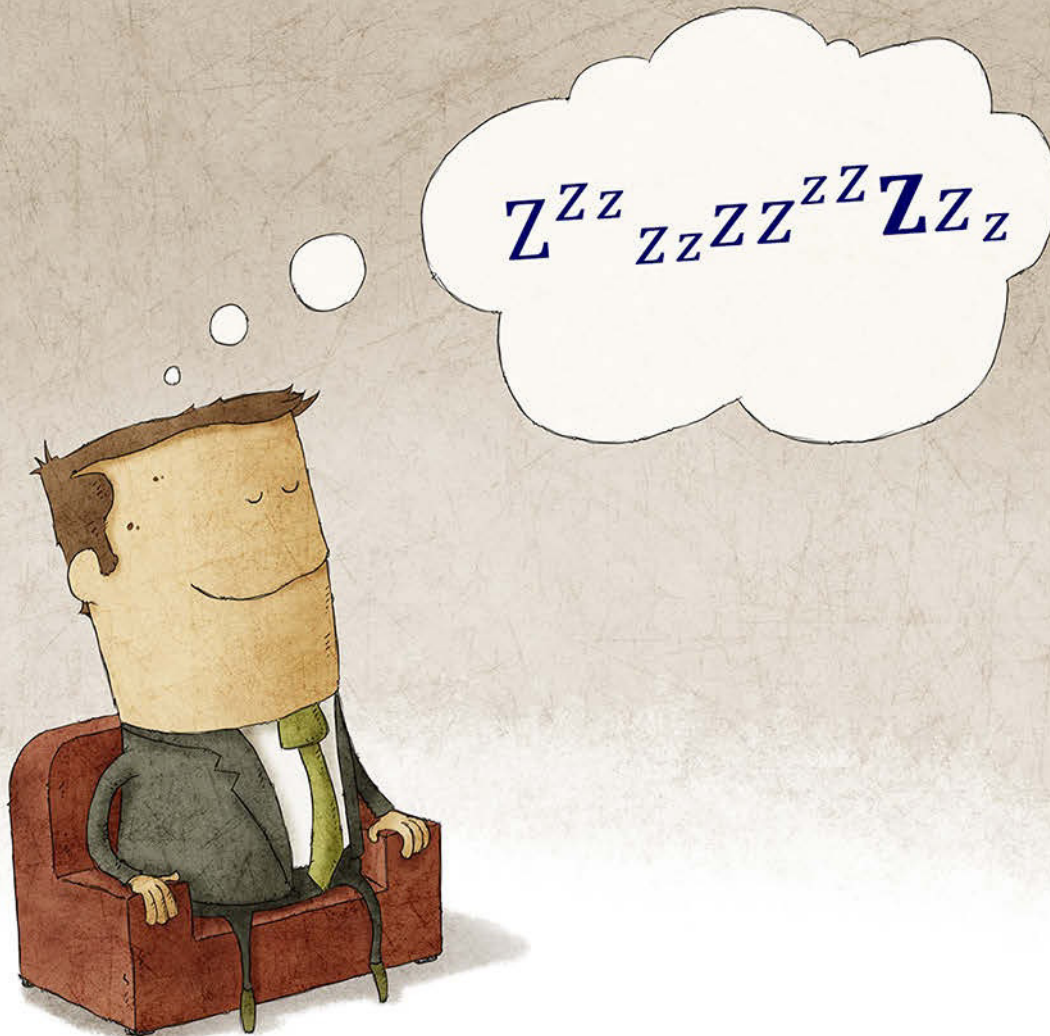
Further Reading

- B. Olney, "Beyond Design: Controlled Impedance Design," *The PCB Design Magazine*, May 2015.
- B. Olney, "Beyond Design: Transmission Lines—From Barbed Wire to High-speed Interconnects," *The PCB Design Magazine*, May 2014.
- B. Olney, "Skewed Again," *The PCB Magazine*, June 2013.
- B. Olney, "Differential Pair Routing," *The PCB Magazine*, October 2011.
- E. Bogatin, *Signal and Power Integrity: Simplified*, Prentice Hall, 2008.
- H. W. Johnson & M. Graham, *High-Speed Digital Design: A Handbook of Black Magic*, Prentice Hall, 1993.
- G Havermann & L. Ritchey, "[SI-LIST] Forum."



Barry Olney is managing director of In-Circuit Design Pty Ltd. (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded at icd.com.au. To read past columns or contact Olney, [click here](#).

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Did you know that two seemingly unrelated concepts are the foundation of a product's performance and reliability?

- Transmission line impedance and
- Power Distribution Network impedance

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"iCD Design Integrity software features a myriad of functionality specifically developed for PCB designers."

– Barry Olney

