# AI-driven Inverse Stackup Optimization

## Beyond Design

**Feature Column by Barry Olney,** IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

Artificial intelligence (AI) is transforming how we conceptualize and design everything from satellites to PCBs. Traditionally, stackup planning is a manual process that can be multifaceted and relies heavily on the designer's expertise. Despite having best practices and various field solvers to optimize parameters, stackup planning remains challenging for complex layers, multiple power pours, and controlled impedance requirements.

This month, I explore inverse stackup optimization (ISOP), a machine learning-assisted framework that automates the stackup design process for advanced package design.

ISOP changes the game by using machine learning to efficiently search for the best

| Differential Pairs > | 50/100 Digital | 40/80 DDR3 | 90 USB | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Material Type | | Dielectric Constant | Dielectric Thickness | Copper Thickness | Trace Clearance | Trace Width | Current (Amps) | Characteristic Impedance (Zo) | Edge Coupled Differential (Zdiff) |
| PSR-4000 HFX Satin / CA-40 HF LPI ... | | 3.5 | 0.5 | | | | | | |
| | | | | 2.2 | 6 | 4 | 0.43 | 51.67 | 90.63 |
| | | | | 2.2 | 12 | 6 | 0.58 | 42.53 | 81.33 |
| | | | | 2.2 | 12 | 4 | 0.43 | 51.67 | 98.65 |
| 370HR ; 1080 ; Rc= 66% (1GHz) | | 3.97 | 2.9 | | | | | | |
| Conductive | | | | 1.4 | | | | | |

Figure 1: The goal-seeking algorithm solves the impedance for distinct technology rules within the same layer. (Source: iCD Stackup Planner)

specifications and optimize performance. The inverse PCB stackup optimization process searches for design parameters that meet the system specifications while optimizing a user-defined figure of merits (FoM). In physics, an inverse problem involves estimating the unknown parameters in reverse through measurements. Similarly, this optimization scheme searches for valid stackup design parameters by obtaining information about the target performance measurements. This optimization process is then accelerated by applying a machine language-based surrogate model.

Today, we essentially plan a stackup by examining the required target characteristic and differential impedance for each technology on each signal layer, then select the best fit from our dielectric materials library to meet our needs (Figure 1). The iCD Stackup Planner, for instance, has a goal-seeking algorithm built into the stackup list view that automatically fine-tunes the parameters.

Impedance goal-seeking algorithms help match trace width and clearance to achieve the desired characteristic or differential impedance. By entering the desired impedance value, multiple passes of the field solver automatically hone the variables to obtain the desired target impedance. This approach helps refine the parameters. However, while it essentially provides a close approximation, it does not determine the stackup structure or the dielectric material.

Alternatively, the inverse stackup optimization framework solves the PCB stackup optimization by incorporating a discrete domain hyper-parameter optimization (HPO), which searches for the best set of parameters in an optimization problem. HPO has been used to tune parameters in the design flow for very large-scale integration (VLSI) and field-programmable gate arrays (FPGA). It can also be used to optimize the hyper-parameters for individual stages, such as component placement and via spans. Besides parameter tuning, HPO also helps address the analog device sizing problem. The automated analog sizing methods work on the inverse design problem. Given target specifications, automatic analog sizing treats design parameters, such as transistor width, as hyper-parameters (configurable variables) and applies HPO to find the solution. HPO can be applied to automate the stackup design to adjust the

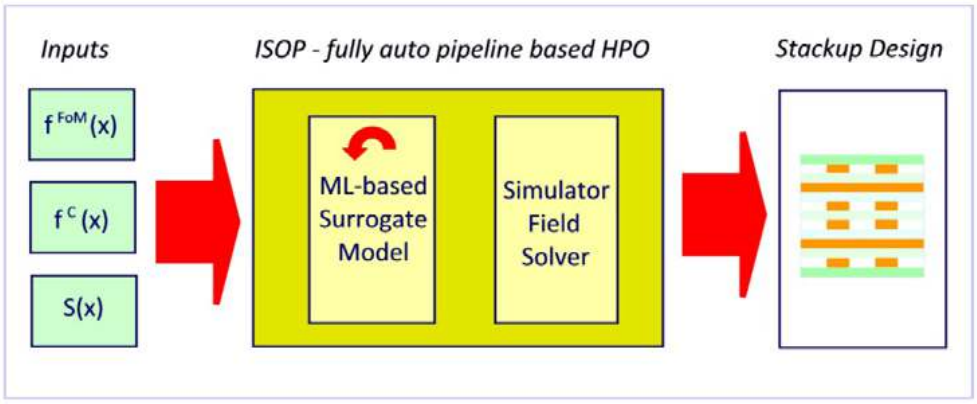


Figure 2: Overall process flow of ISOP framework.

trace width, clearance, and dielectric properties in inverse optimization.

The inverse stackup design optimization aims to find the optimal set of design parameters for each signal layer of a PCB stackup simultaneously. The final stackup design must meet performance specifications and optimize a specified performance FoM objective function. Both the constraints and FoM are from performance metrics and are non-trivial to evaluate. The traditional manual design flow relies on a designer's experience and a trial-and-error approach using multiple simulations. However, ISOP offers a more efficient and automated alternative. The ISOP framework solves the inverse PCB stackup optimization by incorporating a discrete domain HPO. Figure 2 shows an illustration of the overall process flow.

The HPO process begins with a user-defined function, a set of performance constraints, and parameter search spaces as inputs, then generates the stackup design parameters. It consists of two stages:

### *Early search exploration*

Globally, sampling parameters in the first stage allow for the exploration of the search space. Instead of relying on time-consuming EM simulations, it uses performance metrics from a machine learning (ML) surrogate model (approximation model). This approach allows for more samples to be evaluated and a rapid reduction of the search space, albeit with some accuracy trade-offs. This method is akin to reducing the simulation time of a 2D BEM field solver by narrowing the solution space to expedite impedance calculations. A machine learning model termed the "learner" then identifies a limited set of candidates within the input design space whose predicted outputs closely align with desired outcomes.

### *Candidate roll-out*

The second stage selects the final stackup design based on the initial results. The HPO then evaluates the designs with accurate EM simulations and selects the final solution based on the objective function. If specified by the user, ISOP can generate multiple design candidates ranked by FoM in the roll-out stage. A separate surrogate model, functioning as an "evaluator" assesses the reduced candidate space generated in the first stage. This evaluation process eliminates inaccurate and uncertain solutions guided by a user-defined coverage level.

The key innovation of this process lies in the successful integration of conformal inference (predictions), enabling seamless interactions between two machine-learning surrogates. One surrogate acts as a forward problem proxy, identifying promising solutions, while the other plays an advisory role, effectively eliminating inaccurate or uncertain outcomes.

The advantages of this framework over traditional single-stage inverse problems are twofold. First, it circumvents the need for intensive hyper-parameter optimization, as the evaluator model filters out undesired solutions in the second stage. Second, the framework exhibits remarkable applicability across a wide range of problems, owing to conformal inference's minimal distributional and model assumptions. By integrating conformal inference with any standard regression model, the framework readily provides prediction intervals, making it versatile and readily adaptable.

"The inverse stackup design optimization aims to find the optimal set of design parameters for each signal layer of a PCB stackup simultaneously."

Another promising research focus involves designing advanced protocols that enable more than two machine learning surrogates to

collaborate. This approach has the potential to eliminate even more undesired solutions from inverse problems. Evaluating the trade-offs between computational efficiency and accuracy improvements is essential in assessing the feasibility and effectiveness of such protocols.

## Key Points

- The inverse stackup optimization framework solves the PCB stackup optimization by incorporating a discrete domain hyperparameter optimization (HPO), which searches for the best set of parameters in an optimization problem.
- Besides parameter tuning, researchers also apply HPO to address the analog device sizing problem.
- HPO can be applied to automate the stackup design to adjust the trace width, clearance, and dielectric properties in inverse optimization.
- The first stage involves sampling parameters globally to explore the search space.
- A machine learning model termed the "learner" then identifies a limited set of candidates within the input design space whose predicted outputs closely align with desired outcomes.
- The second stage selects the final stackup design based on the initial results.
- A separate surrogate model, functioning as an "evaluator," assesses the reduced candidate space generated in the first stage.
- One surrogate acts as a forward problem proxy, identifying promising solutions, while the other plays an advisory role, effectively eliminating inaccurate or uncertain outcomes. **DESIGN007**

### Resources

- "Beyond Design: Stackup Planning: Three Decades of Innovation," by Barry Olney
- "Machine Learning-Assisted Inverse Stack-Up Optimization for Advanced Package Design" by Chae Hyunsu, et al.
- "Two-Stage Surrogate Modeling for Data-Driven Design Optimization with Application to Composite Microstructure Generation" by Farhad Pourkamali-Anaraki, et al.

Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software, incorporating the iCD Stackup, PDN, and CPW Planner. You can download the software at www.icd.com.au. To read past columns, click here.

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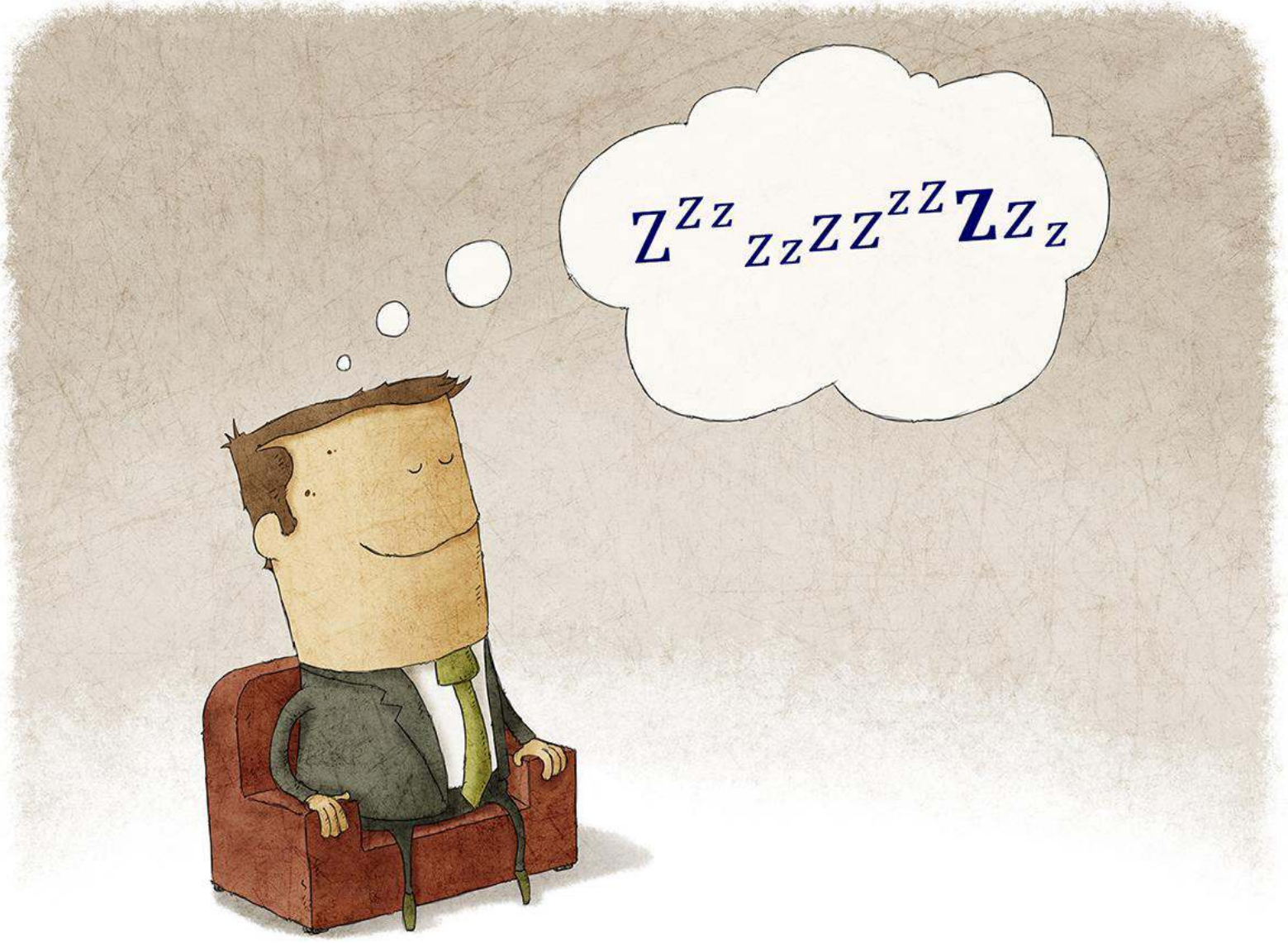


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