Integrated Circuit to PCB Integration

Beyond Design

Feature Column by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

Technologies such as artificial intelligence, autonomous cars, smartphones, and wearable devices are significantly transforming the semiconductor industry. The miniaturization trend drives the IC footprint to an even smaller profile, requiring tighter margins. From the PCB designer's perspective, smaller form factors are achievable, making devices more compact and lightweight. But double-sided SMT placement, reduced routing channels, and high-speed constraints create multiple challenges for designers. However, there are some advantages to miniaturization: shorter interconnects between the IC and the PCB reduce signal loss and electromagnetic interference. High-speed digital signals in the GHz range benefit from reduced parasitics.

Fortunately, most designers are not involved in this cutting-edge design paradigm. However, field programmable gate arrays (FPGAs)

Figure 1: Xilinx Virtex-5 FPGA board. (Source: Xilinx)

are now commonplace in most digital designs. These high-speed, high gate/pin count devices, which once only provided glue logic, are now offering embedded processors, digital signal processors (DSPs), graphics processors, memory blocks, and numerous input/output (I/O) pins in one massive ball grid array (BGA) package, not to mention the considerable number of power supplies required to power these devices. Accommodating 30 to 40 individual power supplies to the active devices is now commonplace. This added complexity has introduced many PCB layout challenges beyond the obvious fanout and route of the fine-pitch BGA.

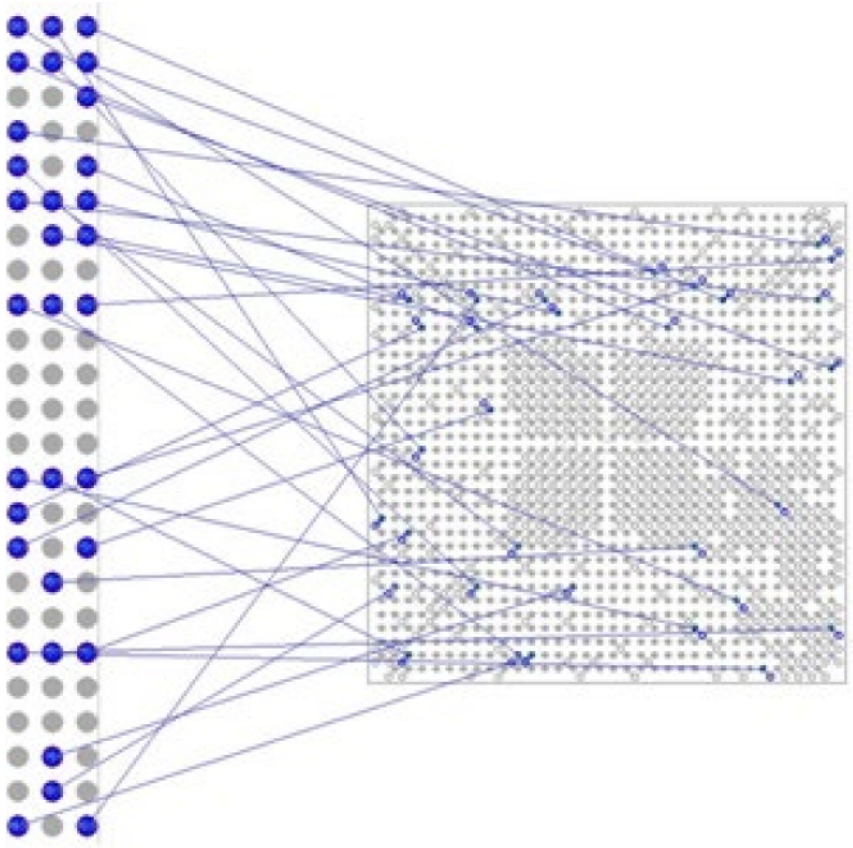

Figure 2: The dispersed connections need to be optimized to eliminate crossovers.

The primary issue is generating optimal FPGA pin assignments that do not add vias and signal layers to a PCB stackup or increase the time required to integrate the FPGA with the PCB. Engineers generally do not consider FPGA pin assignments that expedite the PCB layout. Hundreds of logical signals need to be mapped to the physical pin-out of the device and harmonized with the routing requirements while maintaining the electrical integrity of the design.

To further frustrate the situation, the FPGA I/O assignment is typically in a constant state of flux throughout the design process. Consequently, many PCB designs must be reiterated simply because the board and the FPGA design teams did not have the I/O pin-out synchronized. This has happened to me in the past. The board may go through the process of pre-layout simulation, place, and route, and then a post-layout simulation to verify all the timing is perfect, only to find on testing the assembly that the FPGA I/O pin-out is incorrect on the BGA footprint. Meanwhile, after days of delays, I re-routed, ran design rule checks, re-simulated the layout, and exported the deliverables. However, delays can have financial implications.

Figure 2 shows the rather disorganized I/O connections of a first-pass FPGA pin assignment. This is typically what a PCB designer has to deal with—straight from the FPGA place-and-route tools. To make this more routable, the designer needs to adjust the pin assignment to first be on one outer edge of the BGA and then order the pins to eliminate cross-overs.

Even if we manually reassign the pin-out, the problem now is how to back-annotate this modified BGA pin assignment to the FPGA design tools. The manual process is time-consuming, tedious, and error prone. The key issue is to ensure consistency between the tool sets used in the hardware description language (HDL), FPGA, and PCB environments. We must properly represent the language-based HDL representation of the FPGA as a sche-

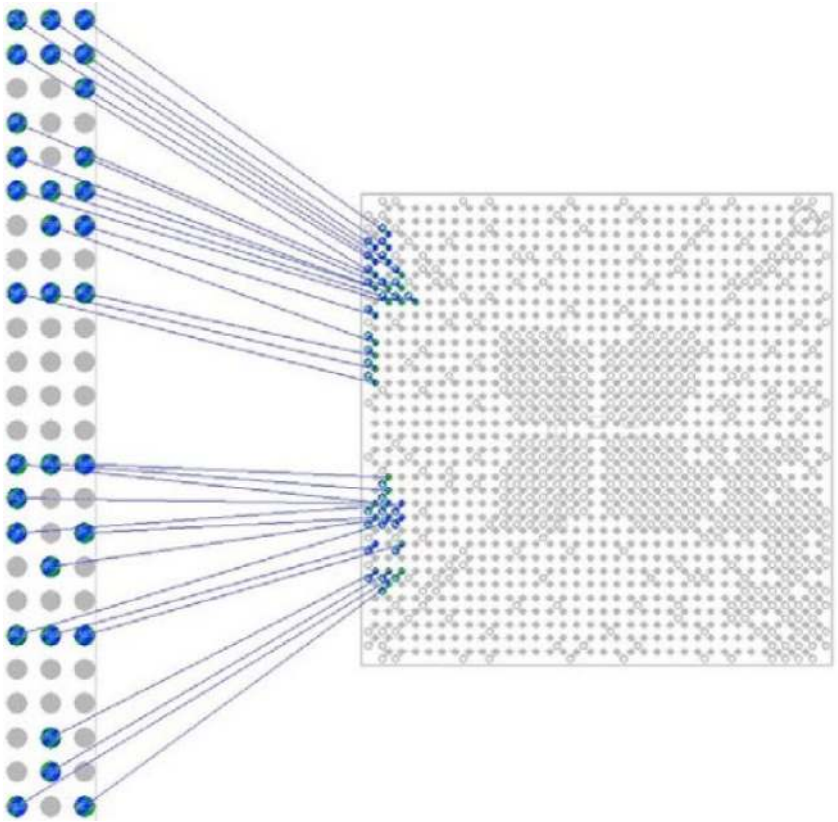

Figure 3: Modifying the pin assignment eliminates cross-overs.

matic symbol containing the correct pin data, as well as the appropriate mapping to the BGA footprint.

Alternatively, I/O optimization tools (Figure 3) can provide parallel paths of FPGA and PCB design, trimming days from the design process and delivery schedules and providing significant overall long-term cost benefits. We can meet these challenges with tools that add hardware description language (HDL) synthesis and advanced FPGA-PCB I/O optimization to the PCB layout software. This interface between the HDL design environment and the physical implementation on the PCB significantly reduces both time-to-market and manufacturing costs by automating the process, reducing errors and thus iterations.

At any stage of the project, the PCB design flow should tightly integrate I/O optimization and make it accessible. Keeping the schematic, PCB layout, and FPGA databases synchronized allows users to control the flow of design data in the project.

An FPGA vendor-neutral design environment that enables architecture-specific optimization takes advantage of the specific features of each FPGA device to meet the design requirements. Vendor-independent synthesis supports devices from Altera, Lattice, Microsemi, and Xilinx. Therefore, you can use the same HDL design source files and constraints to target any device and to obtain a synthesized netlist that can be used for place and route with the appropriate vendor tools. This vendor independence allows users to easily re-target and analyze results for any FPGA device, enabling you to find the best FPGA device to suit the design.

Automating this error-prone boundary between FPGA and PCB design makes sense. Most of the popular PCB vendors have I/O optimization tools. Cadence has its FPGA System Planner, Siemens has I/O Optimization, and Zuken has FPGA Co-design solutions. Design teams need to implement these new methodologies to ensure they do not negate the cost and time-to-market benefits of using programmable logic.

Key Points

- The miniaturization trend is driving the IC footprint to an even smaller profile, requiring tighter margins.
- Taiwan currently produces approximately 80% of the global supply of silicon chips.
- Double-sided SMT placement, reduced routing channels, and high-speed constraints are creating multiple challenges for designers.
- Shorter interconnects between the IC and the PCB reduce signal loss and electromagnetic interference.

- Accommodating 30 to 40 individual power supplies to the active devices is now commonplace. This added complexity has introduced many PCB layout challenges beyond the obvious fanout and route of the fine-pitch BGA.
- The primary issue is generating optimal FPGA pin assignments that do not add vias and signal layers to a PCB stackup, or increase the time required to integrate the FPGA with the PCB.
- Many PCB designs have to be reiterated simply because the board and the FPGA design teams did not have the I/O pin-out synchronized.
- To make a layout more routable, the designer needs to adjust the pin FPGA assignment.
- The problem is how to back-annotate this modified BGA pin assignment to the FPGA design tools.
- I/O optimization tools can provide parallel paths of FPGA and PCB design, trimming days from the design process and delivery schedules and providing significant overall long-term cost benefits. **DESIGN007**

Resources

1. Beyond Design: "FPGA-PCB Design Challenges" by Barry Olney
2. "FPGA I/O Features Help Lower Overall PCB Costs" by Dave Brady, Siemens EDA

Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software, incorporating the iCD Stackup, PDN, and CPW Planner. You can download the software at www.icd.com.au. To read past columns, click here.

THE NEW CHAPTER

The Impact of Parasitics on PCB Design

by Hannah Grace

There are many considerations when planning and designing a board layout, and factors that include signal integrity, electromagnetic interference, and power integrity must be considered. Newer board designers often forget one factor crucial to a PCB's performance and reliability, namely board parasitics, which usually refers to an unintended electrical effect in electronic components and interconnections. This can often lead to significant changes in physical characteristics of board performance and reliability. Typically, signal integrity, power integrity, frequency response, timing, and delay, as well as EMI/EMC considerations, rely on parasitic management for certain design traits. A simulation without parasitics can compromise the design and ultimately cause it not to perform as intended.

The impact of parasitics on signal integrity, and parasitic elements such as capacitance and inductance, can lead to signal degradation, additional undesirable noise, and those potential unwanted ta transmission. High-frequency signals are particularly susceptible to the effects of parasitics on signal integrity.

Parasitics can also influence the distribution and integrity of power through a PCB, potentially causing loss of power and instability in power-sensitive applications, as well as inefficient energy transference throughout the board.

Typically, in board design, parasitic look similar to the length of a trace o a wire. Each trace is slightly resistive, slightly inductive, and slightly capacitive. These are commonly known as parasitic capacitance, parasitic inductance, and parasitic resistance.

The Impact of Managing Parasitics

Managing parasitics in board design can have a significant impact on the

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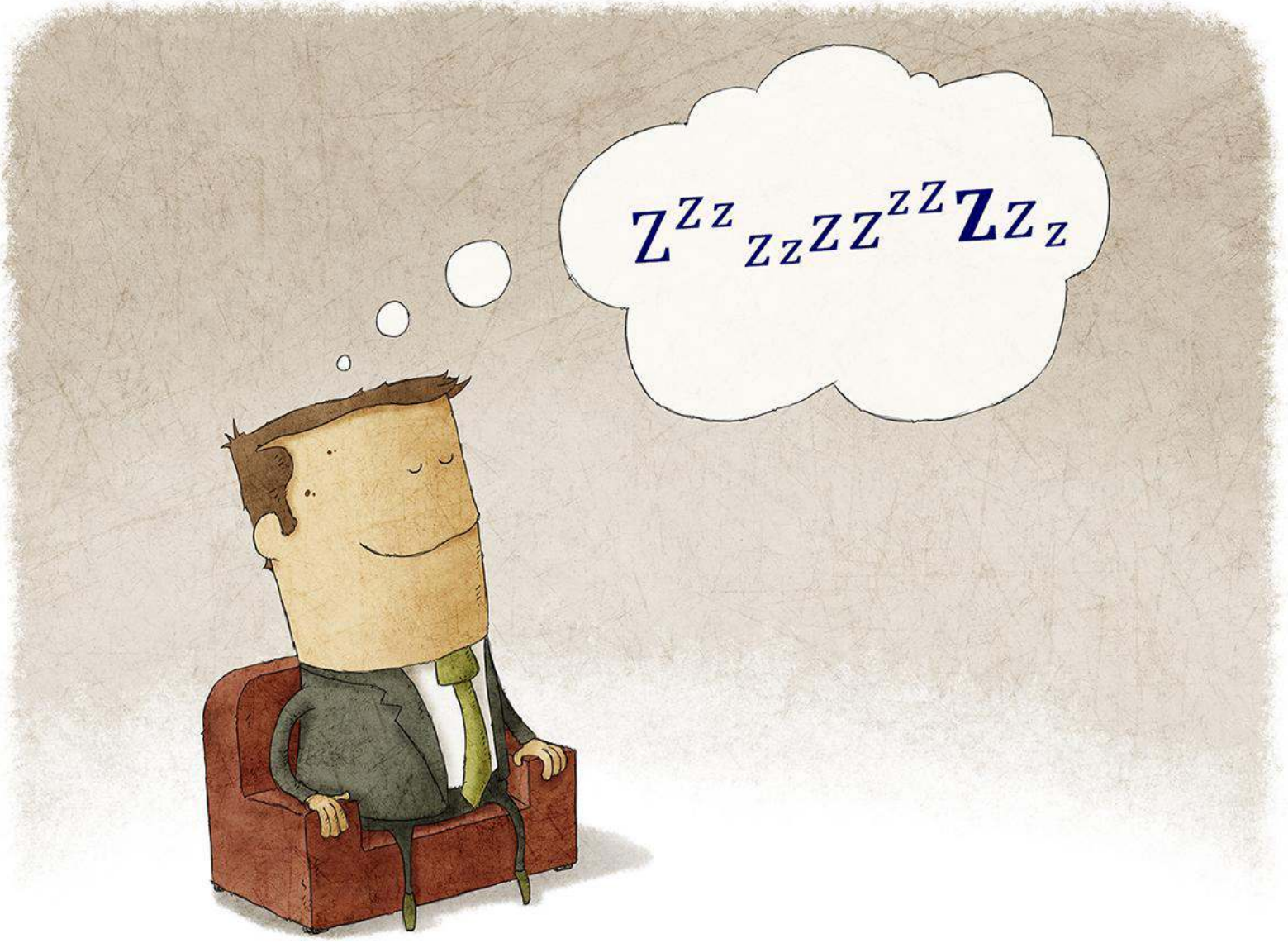

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