Fast and Accurate Transmission Line Modeling

Beyond Design

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The ability to simulate complex PCB design has become a critical factor in the success of a project. Today's high-speed processors and SERDES interfaces coupled with sometimes unrealistic time-to-market requirements are pushing design teams toward more nimble development processes. However, there is no point in completing a design on time if it does not work!

To ensure the prototype has first-pass success, designers need to perform accurate board-level simulation, throughout the entire design process. But the challenge is how do you quickly perform the simulation if all the models for the board are not available and if the simulation setup time is prohibitive? Enter the I/O Buffer Information Specification (IBIS). This specification is a fast and accurate behavioral method of modeling input/output buffers based on I-V curve data derived from measurements or full circuit simulation.

Figure 1 depicts the Ibis (bird). With its greedy, little black eyes and its long, trash-probing beak, the Ibis has readily adapted to its environment. We Australians colloquially call it "the bin chicken" since its six-inch curved beak has been sculptured by evolution to effortlessly reach to the bottom of a Macca's (MacDonald's) fries container.

Getting back to simulation, before the release of the IBIS specification, SPICE transistor-level models were the only consistent method by which circuit models could be created. However, transistor-level models are not well suited to simulate an entire multilayer PCB containing several hundred nets and drivers. Also, semiconductor vendors that generate the models for their integrated circuits do not readily give these models out since they can disclose proprietary information that is confidential, including circuit nodal connections and underlying fabrication processes parameters. Meanwhile, the IBIS model does not require propri-

Figure 1: The Ibis. (Source: Australian Geographic)

etary information about the modeled circuit since no process or circuit design information is disclosed.

The IBIS models are accurate since nonlinear aspects of I/O structures as well as package parasitics, on-die termination (ODT), and ESD structures are considered in the model parameters. More recently, power-aware models have been specified to combine signal integrity (SI) and power integrity (PI) simulation. Since the IBIS is behavioral, the simulation time for a model can run some 25 times faster than a structural model such as that used in SPICE. In addition, IBIS does not have non-convergence issues encountered in SPICE models that prevent the simulator from reaching a valid solution within a certain number of iterations. Now, most EDA vendors support the IBIS specification as the defacto simulation standard.

IBIS models for many devices are available as free downloads from IC vendor support pages. IBIS provides the following:

- Faster simulation speed
- A large variety of I/Os in a single IBIS file so that easy system model simulation is possible
- The inclusion of signal integrity specifications, such as input logic thresholds, overshoots, etc.
- Power-aware properties introduced to provide simultaneous SI/PI analysis
- Elimination of non-convergence
- Strong support from virtually all EDA vendors
- Backward compatibility with models created under previous IBIS standards

At its core, a CMOS IBIS model (Figure 2) uses only a few tables of data to represent the behavioral characteristics of a buffer. Two sets of I-V tables represent the I_{DS} versus V characteristics of the pull-down and pull-up transistors, showing the dynamic impedance of the buffer. The switching behavior of the buffer is revealed through a set of V-T tables that capture the rising and falling edge transitions of the buffer driving resistive test loads. The capacitance of the buffer and the package RLC are also quantified. This information, plus the transmission line characteristics, provides an accurate model for SI simulation, but it lacks behavioral characteristics necessary for PI simulation. One of the major upgrades in the IBIS version 5.0 specification was the introduction of additional data tables to model buffer power characteristics (not shown). Models containing these data are known as power-aware IBIS models.

Let's look at a practical example of how to implement a transmission line simulation

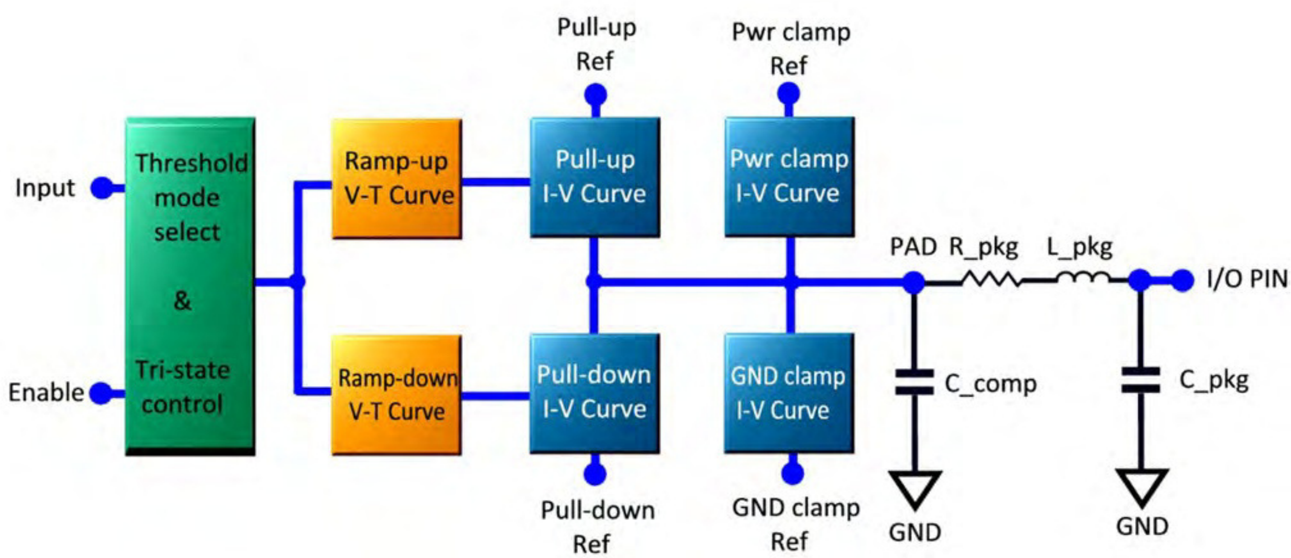

Figure 2: Building blocks of a CMOS buffer IBIS model.

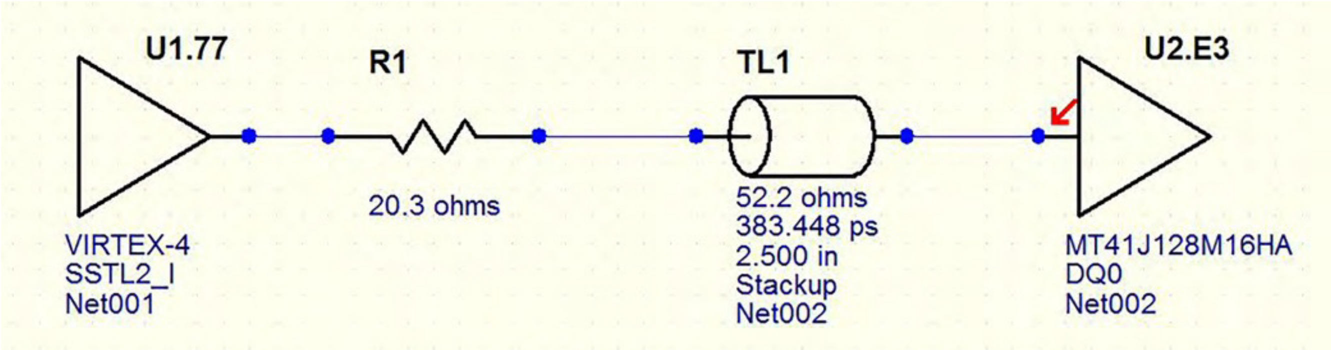

Figure 3: DDR2 data signal with a series terminator. (Source: HyperLynx)

using the IBIS model. I/O buffer and drive strength selection can be analyzed in pre-layout simulation. A vendor-provided IBIS model should contain all available drivers for each model, and may, for example, include buffer models with 8 mA, 12 mA, and 16 mA drive current. The mid-level 12-mA driver is generally required unless there is a long transmission line with multiple loads. This may be the case on a motherboard when driving a number of DIMM modules, for instance.

The schematic description that includes the stackup definition, arrangement of a network, its nodes, sequence, connecting transmission lines and vias is generically referred to as the interconnect topology. To avoid signal quality and timing issues and minimize manufacturing costs, thorough topology analysis is critical to the successful implementation of a high-speed interconnect. Ideally, this analysis should be done up-front before placement and routing.

Topology optimization involves:

- Selecting an optimal topology style for signal integrity, timing, and EMC
- Shortening traces and stubs to their critical length or shorter where possible

The most basic topology is a simple point-to-point interconnection between a driver and a receiver (Figure 3). This topology is commonly used for busses or otherwise grouped traces. A good example of this would be the data banks of DDRx memory. Left unterminated, these traces may be too long (more than 1/10 rise time), and reflections become problematic. Figure 3 also illustrates a Xilinx, Virtex 4 transceiver driving a DDR2 data signal into a long, 52.2-ohm transmission line. Initially, the signal was simulated with no series termination, resulting in the red waveform in Figure 4. The green waveform represents the terminated transmission line.

The impedance of the trace is extremely important, as any mismatch along the transmission path will result in a reduction in signal

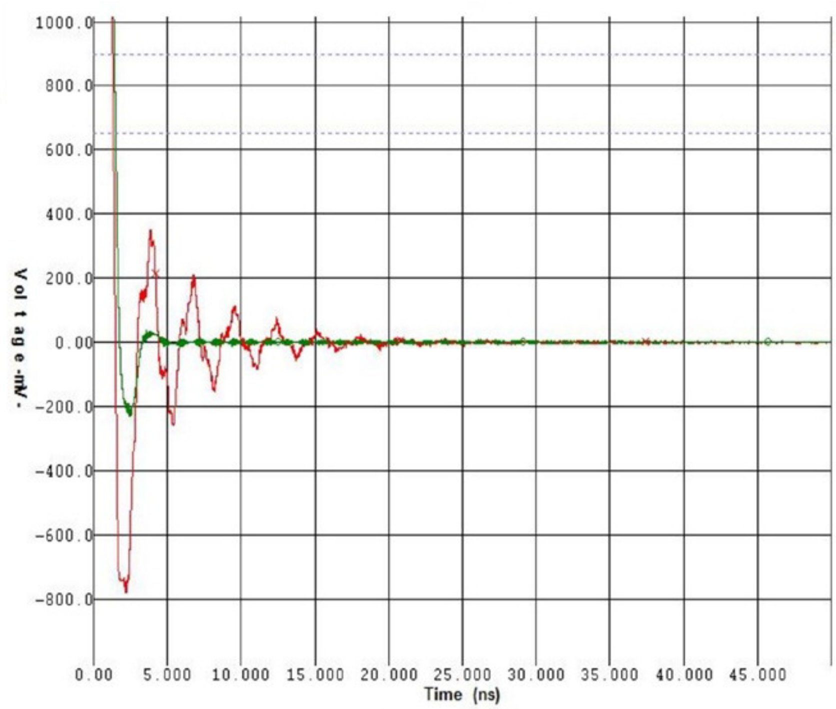

Figure 4: Ringing of the data signal due to reflections. (Source: HyperLynx)

quality and possibly the radiation of noise. Mismatched impedance causes signals to reflect back and forth along the transmission line, which results in ringing at the load (Figure 4). The ringing reduces the dynamic range of the receiver, eats into the noise budget, and can cause false triggering due to non-monotonic edges.

Reflections occur whenever the impedance of the transmission line changes along its length. This can be caused by unmatched drivers/loads, layer transitions, different dielectric materials, stubs, vias, connectors, and IC packages. By understanding the causes of these reflections and eliminating the source of the mismatch, a design can be engineered with reliable performance. For the perfect transfer of energy and to eliminate reflections, the impedance of the source must equal the impedance of the transmission line.

It is one thing to perfectly match the impedance and delay of the transmission lines, but using mainstream PCB layout software, unfortunately, one really has no idea what the driver impedance is, let alone the capability to match the driver to the impedance of the transmission line. The iCD Termination Planner addresses this issue (Figure 5).

First, the attributes required to determine the source impedance of the driver are extracted from an IBIS model I-V curves. Then, the required series termination resistance is calculated based on a distributed system to match the transmission line impedance for the selected stackup layer. The number of loads on the transmission line also has an impact on the required value of series termination, as the IC input inductance and capacitance tend to roll off the signal rise time. This can be adjusted from 1–6 loads and automatically compensated for in the calculation. If you do not have access to a board-level simulator, then this is a good option to easily avert ringing.

Modeling complex PCB designs does not have to be time-consuming and difficult. The topology can generally be automatically extracted from the PCB layout into a free-form schematic, providing all the transmission line, via, and stackup information required. The designer only needs to select the IBIS driver and load models plus a stimulus in the form of a set frequency or a pseudorandom bit stream (PRBS) to simulate

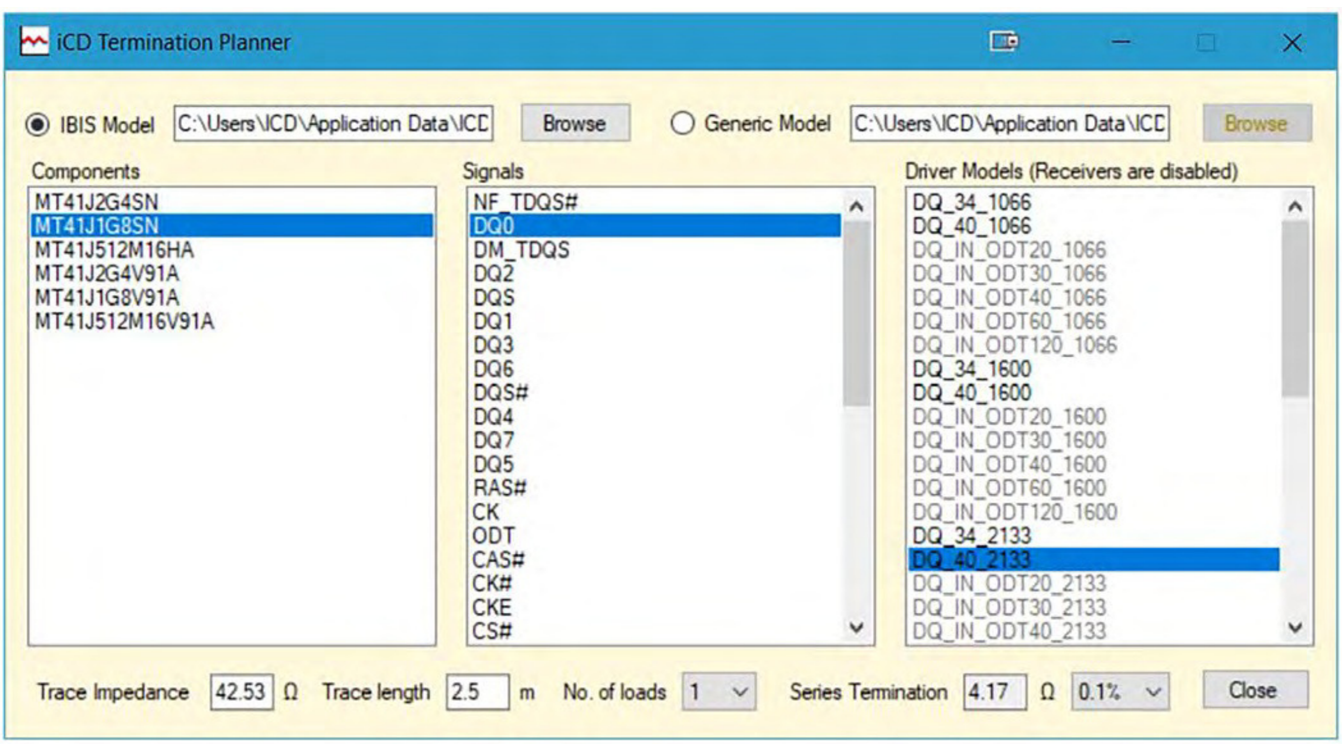

Figure 5: Matching a DDR3 driver IC to the transmission line. (Source: iCD Termination Planner)

the entire interconnect. The IBIS specification is a fast and accurate behavioral method of modeling high-speed transmission lines throughout the entire design process.

Key Points

- To ensure the prototype has first-pass success, designers need to perform intensive and accurate board-level simulation
- The IBIS specification is a fast and accurate behavioral method of modeling input/output buffers based on I-V curve data derived from measurements or full circuit simulation
- SPICE models are not well suited to simulating an entire multilayer PCB containing several hundred nets and drivers
- SPICE models can disclose substantial information that is confidential, including circuit nodal connections and underlying fabrication processes parameters
- The IBIS model does not require proprietary information about the modeled circuit since no process or circuit design information is disclosed
- Since the IBIS is behavioral, the simulation time for a model can run some 25 times faster than a structural model, such as that used in SPICE
- A CMOS IBIS model uses only a few tables of data to represent the behavioral characteristics of a buffer
- One of the major upgrades in the IBIS version 5.0 specification was the introduction of power-aware models
- The interconnect topology includes the stackup definition, arrangement of a network, its nodes, sequence, and connecting transmission lines and vias
- The impedance of the trace is extremely important, as any mismatch along the transmission path will result in a ringing, reduced signal quality, and possibly the radiation of noise
- Using mainstream PCB layout software, one really has no idea what the driver impedance is, let alone the capability to match the driver to the impedance of the transmission line **DESIGN007**

Further Reading

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Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded from www.icd.com.au. To read past columns or contact Olney, click here.