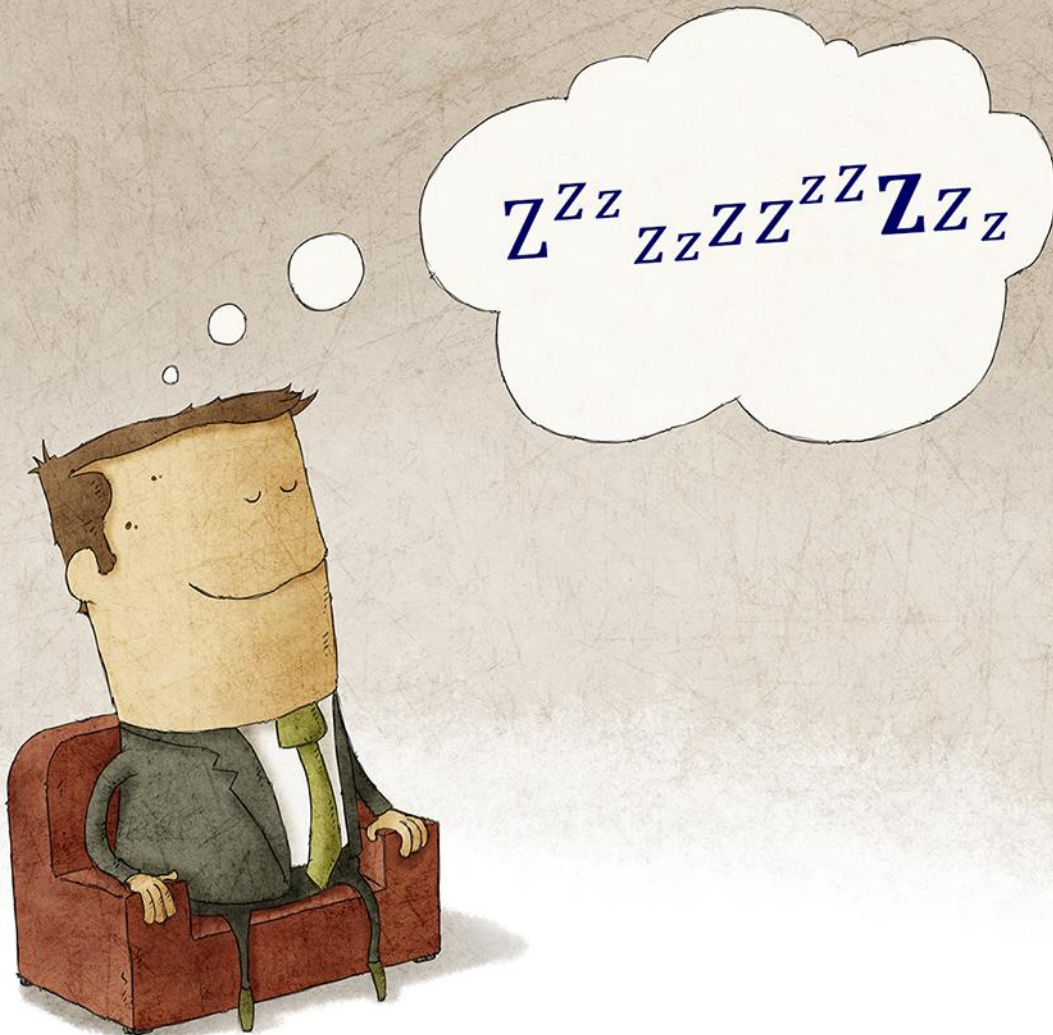


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A Review of HyperLynx DRC

Beyond Design

by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

There is an old saying, “You get what you pay for.” Does this mean that you should not expect too much from free software? After all, free software usually comes at a price: the results might be inaccurate, the software might be time-consuming to set up and use, and the tool might overlook issues that require a revision to mitigate.

But HyperLynx DRC is the exception to the rule. In this month’s column, I will review Mentor’s new HyperLynx DRC Free Edition, which provides analysis tools that complement any PCB layout tool that can export ODB++ or IPC-2581B formats.

Amazingly enough, this software is free. You’ll need to confirm registration annually, but that is not a problem; the tool remains free.

There is also a more comprehensive, affordably priced Gold Edition.

HyperLynx DRC is an electrical design rule checking (DRC) tool that can automate the verification of complex digital design rules that are not easily detected, such as rules for traces crossing split planes and electromagnetic compliance (EMC). It does not require expert knowledge and can literally save hours of manual inspection. The tool helps one avoid costly errors and oversights, directing the novice high-speed PCB designer to the source of signal integrity (SI), power integrity (PI) and EMC issues.

Even experienced designers make mistakes and overlook small issues that can become major headaches further down the design,

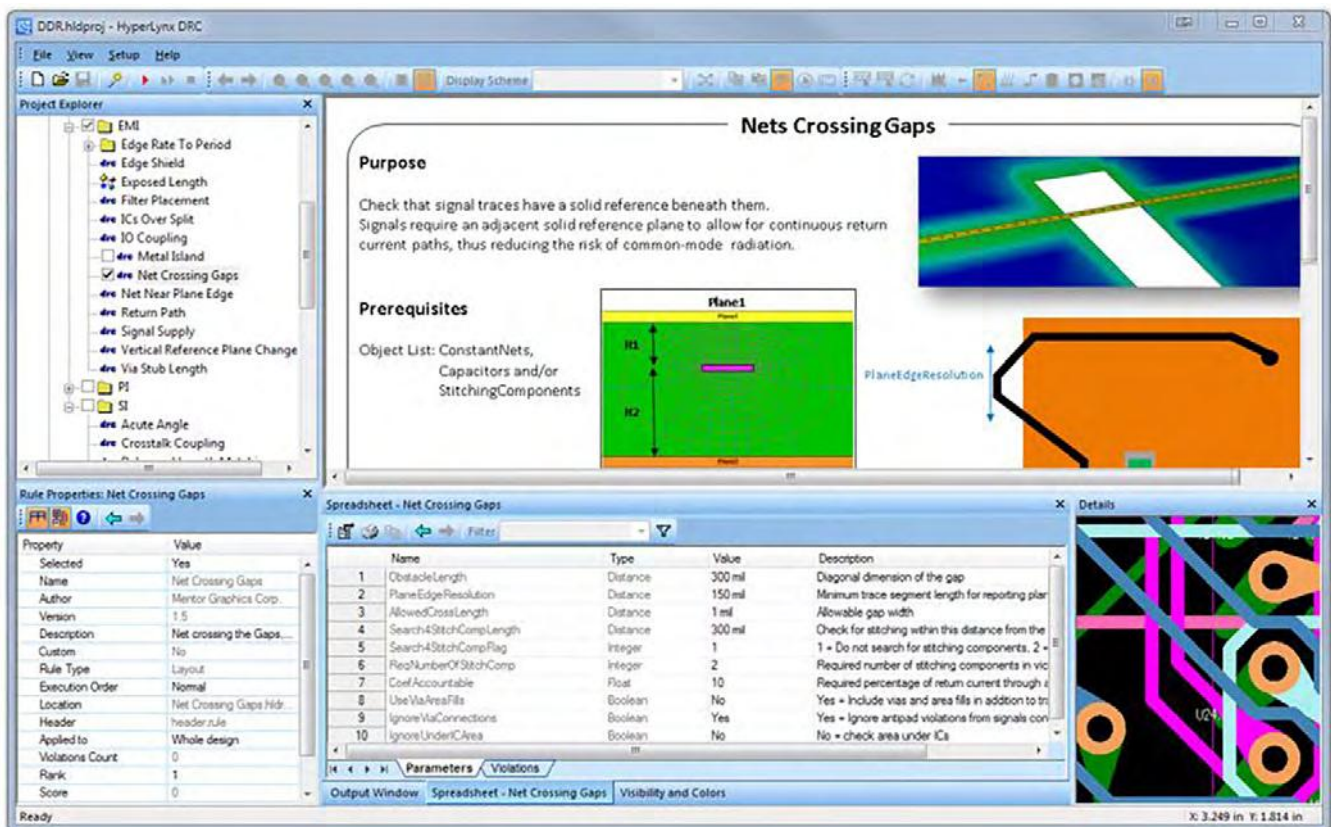


Figure 1: Setting up EMI rules for nets crossing gaps in HyperLynx DRC.

assembly, test or production processes. This is particularly true with complex, high-speed designs that have multiple planes and return paths, requiring elaborate constraints on every class of technology. Sure, we can enter hundreds of rules to constrain copper pours, placement and routing, but there is always some manual adjustment that needs to be made as each design is different and has specific requirements. Online DRCs in EDA tools are a great safeguard, but they do slow the design process somewhat. They warn you when a physical or electrical rule is violated and allow the designer to steer clear of common obstacles.

Although the complete list of design rules is very broad, one must manage the following constraints at a minimum:

- Placement
- Clearance
- Routing
- High-speed signals–impedance and differential pairs
- Plane and copper pours
- Test points (if required)
- Manufacturing

Impedance discontinuities and crosstalk can be controlled to some extent by PCB designers during the routing phase if they understand these concepts, which many, unfortunately, do not. Although pre-layout analysis detects issues before they occur, signal integrity, power integ-

ry and EMC issues cannot be properly evaluated until the design has been completed and a post-layout analysis is implemented.

For instance, the most common cause of radiation from a multilayer PCB is a deviation or break in the return current path of a signal as in Figure 1. Electromagnetic fields couple the signal trace to the reference plane(s), and a gap in the return path will increase the loop area which typically causes radiated emissions. Nets crossing split planes can be examined manually but it is a very error-prone process particularly when there are multiple power supplies on multiple layers. Additionally, the gap in the plane area or the break in the return path may not necessarily be in the nearest stackup layer. If poorly designed, the return path may be in a faraway layer.

Many independent designers find it difficult to check their own work. They become blind to crucial design details. When you assess your own work, your brain already knows your intention and subconsciously skips the detail. Critiquing someone else's work is much easier because looking through another's eyes brings a fresh perspective. What is needed is a totally unbiased, automated check that considers only the established high-speed design rules.

This is where HyperLynx DRC can complement your EDA layout tools. It specifically scans for violations of signal integrity, power integrity and EMI rules. And, let's face it, these

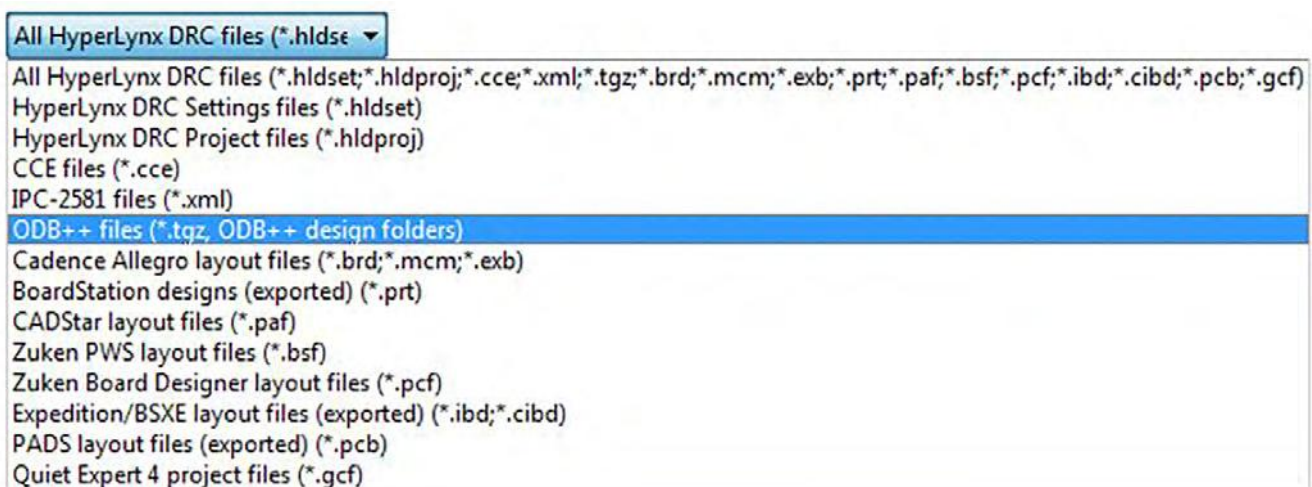


Figure 2: Available import formats to HyperLynx DRC.

are the issues that most of us do not understand. Many enterprise-level EDA tools feature an expert system that performs this function. HyperLynx DRC Free Edition brings some of those capabilities to everyone's desktop. It is like having an SI engineer sitting next to you, nudging you in the ribs whenever he notices that you have missed an aspect of the design that you may want to reconsider.

One would assume that an export to HyperLynx DRC would be streamlined in Mentor's own PCB layout tools, Xpedition and PADS, so for this exercise I exported the ODB++ format from Altium Designer. This creates an ODB directory in the current folder. The available import formats are listed in Figure 2.

Once the database has been loaded, the design rule parameters need to be set. One might think this to be a daunting task. However, HyperLynx DRC was specifically devel-

oped for the novice designer, so the guys at Mentor have done all the hard work for you.

The Project Setup Wizard walks you through, and explains in detail, the entire setup, which you can adjust to on the fly, if you have the knowledge. Alternatively, you can just accept the defaults, which seem to work fine unless there are specific requirements.

You also need to verify that the software correctly recognized the components, signals and stackup data. There are filters already set up for components by reference designator and differential pairs, single-ended signals and power nets by their naming convention. These can easily be modified by substituting an "IC" for "U," etc. But, my design had no such issues—too easy!

Now that the layout database is loaded, verified and all the rules have been set up, the DRC

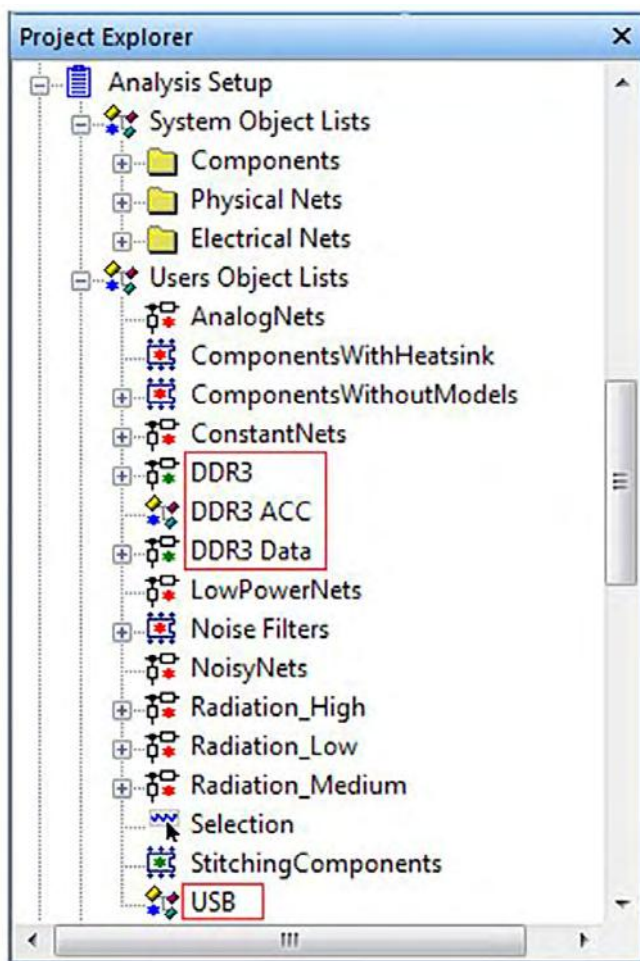


Figure 3: Analysis setup.

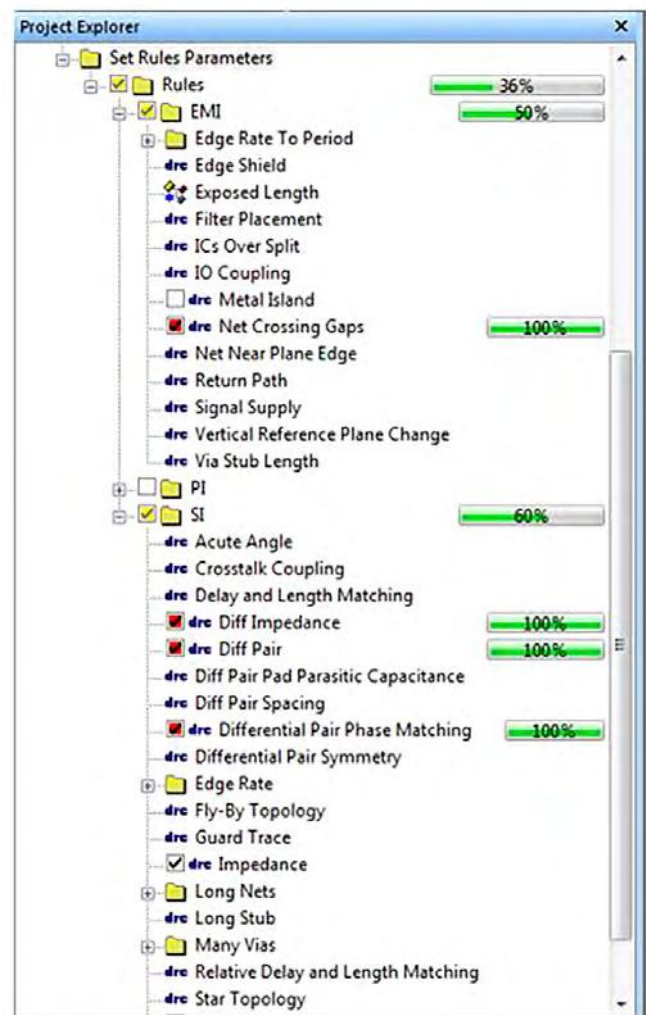


Figure 4: Executing batch mode DRCs.

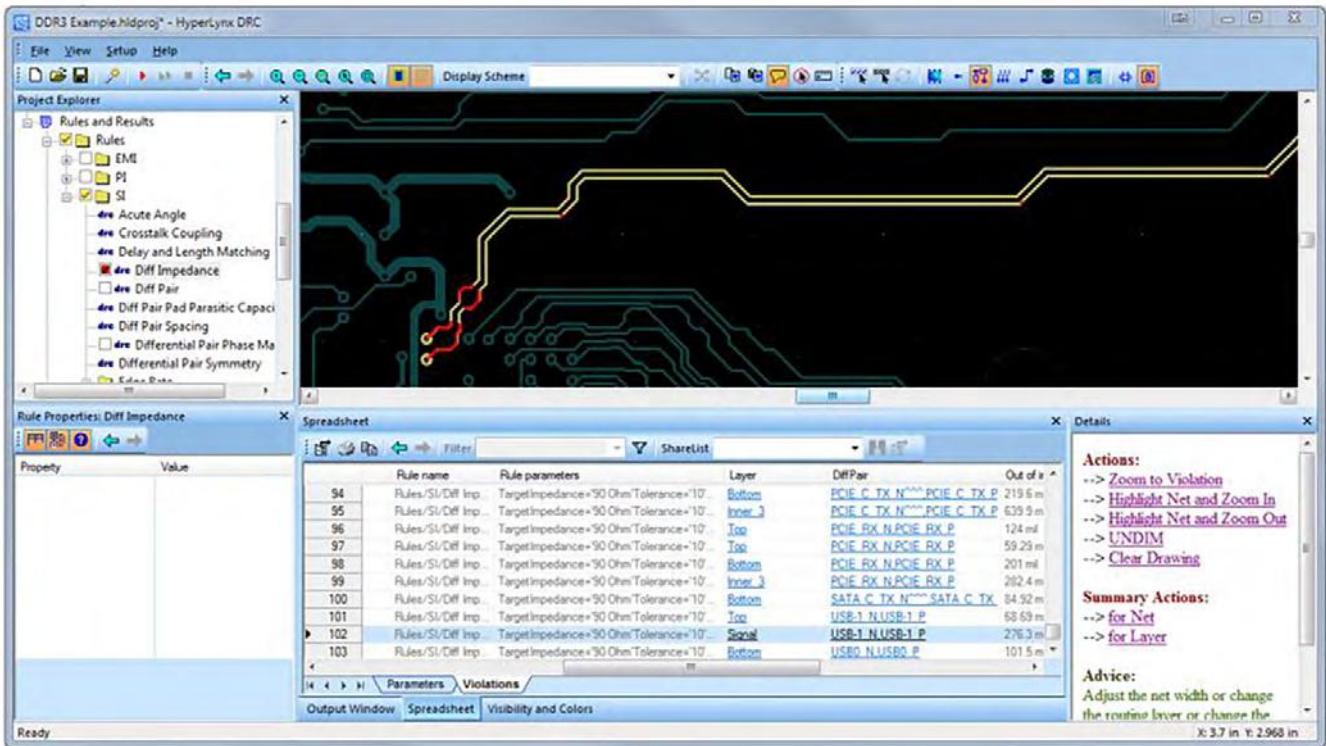


Figure 5: Uncoupled length of differential pairs.

can be launched. However, in order to avoid producing a large number of violations in batch mode, the number of enabled rules can be initially limited. Further rules can be gradually added to increase the scope as violations are eliminated.

The scope of the checks can be defined using a specific group of design objects. I set up “User Objects” for DDR3, DDR3 ACC, DDR3 Data and USB which are similar to Net Classes in EDA tools (Figure 3). Then a DRC can be run on that particular group of signals, so that the violations can be checked in subsets, which simplifies the process.

Alternatively, all DRCs can be run in batch mode and each violation can then be evaluated in succession (Figure 4). However, the individual lists present more control over the parameters. For instance, the differential impedance can be modified from 80ohms for DDR3 to 90ohms for USB between checks.

Figure 5 shows the results of the uncoupled length check for differential pairs. This image highlights where the USB pair loses coupling and increases in impedance, so you can visualize where the variations occur. In this case, it

is an acceptable violation.

Keep in mind that the flagged violations are not necessarily errors. In this age of design complexity and limited time to market, there are always compromises that one has to accept due to schedule and other restrictions. HyperLynx DRC identifies violations of the established rules enabling the designer to quickly make a decision on the acceptability or not of the violation.

Once DRCs are completed, the errors can be selected individually, from the violation listing, for viewing. In addition, Sharelist reports containing the image, violation details, coordinates and user comments can be generated in HTML for broader team review.

Additionally, customers have free access to the [HyperLynx DRC Community](#). This forum provides the benefit of trouble shooting technical issues and discussing ideas, with fellow designers, regardless of your layout tool, or level of expertise.

HyperLynx DRC complements most EDA layout tools and does not require high-speed design expertise. It quickly identifies and highlights possible design inconsistencies and puts

the novice high-speed designer in control of common SI, PI and EMC issues. Even experienced designers can benefit. I will certainly use the software to analyze my future designs and I believe it would be an invaluable addition to any PCB designer's tool box. In this case, you absolutely do get something, extremely useful, for nothing—it's a no brainer. **DESIGN007**

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1. Design Rule Checks for High-Speed PCB Design, by Patrick Carrier.
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3. Mentor Graphics' HyperLynx DRC software and documentation.



Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN and CPW Planner. The software can be downloaded from www.icd.com.au. To contact Olney, or read past columns, [click here](#).

New Device Modulates Light and Amplifies Tiny Signals

By taking clever advantage of the interplay between light, electrons on the surface of metals, and heat, researchers at the National Institute of Standards and Technology (NIST) have for the first time created a plasmomechanical oscillator (PMO), so named because it tightly couples plasmons—the collective oscillations of electrons at the surface of a metal nanoparticle—to the mechanical vibrations of the much larger device it's embedded in.

The device consists of a gold nanoparticle, about 100 nanometers in diameter, embedded in a tiny cantilever—a miniature diving board—made of silicon nitride. An air gap lies sandwiched between these components and an underlying gold plate; the width of the gap is controlled by an electrostatic actuator—a thin gold film that sits atop the cantilever and bends toward the plate when a voltage is applied. The nanoparticle acts as a single plasmonic structure that has a natural, or resonant, frequency that varies with the size of the gap, just as tuning a guitar string changes the frequency at which the string reverberates.

When a light source, in this case laser light, shines on the system, it causes electrons in the resonator to oscillate, raising the temperature of the resonator. This sets the stage for a complex interchange between light, heat and mechanical vibrations in the PMO, endowing the system with several key properties.

The team also demonstrated for the first

time that if the electrostatic actuator delivers a small mechanical force to the PMO that varies in time while the system undergoes these self-sustaining oscillations, the PMO can lock onto that tiny variable signal and greatly amplify it. The researchers showed that their device can amplify a faint signal from a neighboring system even when that signal's amplitude is as small as ten trillionths of a meter. That ability could translate into vast improvements in detecting small oscillating signals.

