

# How Signals Survive the Hostile PCB

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**M**odern digital signals exhibit behavior more characteristic of RF waveforms than the slow logic transitions of the past. With fast rise times, a PCB is no longer a collection of copper traces, but a distributed electromagnetic system. Successful design isn't about routing signals anymore; it's about engineering transmission lines, preserving uninterrupted return

current paths, and controlling the resonant structures that naturally form within the multilayer PCB.

Rise time, not clock frequency, is the real driver of signal behavior, dictating when reflections, ringing, and RF-like effects emerge. At fast edge speeds, every trace becomes a transmission line with its own characteristic impedance and propagation behavior. Understanding these interactions

is essential for optimizing high-speed digital designs, ensuring reliable performance, and minimizing electromagnetic interference. This approach shifts the design paradigm from simple routing to sophisticated electromagnetic management, crucial for modern high-speed electronic systems.

Arguably, the most critical factor in high-speed PCB design is the impedance of the interconnect. Controlled impedance is the foundation of the design's integrity. It forms the essential baseline, as reflections, terminations, return-current behavior, and even plane interactions all assume a stable, controlled impedance along the interconnect.

Impedance is at the core of the methodology that is used to solve signal integrity issues:

1. Signal quality issues arise because voltage signals reflect and are distorted whenever the impedance changes along a transmission line.
2. Crosstalk arises from the coupling of electric and magnetic fields between adjacent traces or between traces and return paths. The inductance and capacitance between the traces establish an impedance that determines the amount of coupling.
3. Differential-mode propagation can be converted to common mode by parasitic capacitance or by any imbalance caused by impedance variation, signal skew, rise/fall-time mismatch, or channel asymmetry. Common-mode currents are the main source of electromagnetic radiation.

The iCD Stackup Planner, in Figure 1, illustrates the three most common transmission line structures of a multilayer PCB. For embedded microstrip (solder mask-coated microstrip), the electromagnetic field propagates partially in the dielectric material, the solder mask, and the air. Whereas, in both stripline structures, the electromagnetic field propagates in the dielectric material sandwiched between the planes.

A characteristic impedance of 40–60 ohms is typically used for a digital design. However, this value becomes more critical as the edge rates become faster. Also, different technologies have their specific impedance requirements. For example, Ethernet is 100 ohms differential, USB is 90 ohms differential, DDR2 memory is 50/100 ohms single-ended/differential impedance, and DDR3-5 is 40/80 ohms single-ended/differential impedance. So, controlling impedance simultaneously across each signal layer with multiple technologies can be challenging. Also, as operating voltages are reduced, the associated noise margins are also reduced, making it even more important to match the impedance.

Once we define the characteristic impedance, the next challenge is ensuring the signal actually sees that impedance along its entire path. When a transmission line is perfectly matched to the driver and load, the signals propagating electromagnetic (EM) energy are totally absorbed by the load. This is the perfect scenario that all electronics designers strive for.

UNITS: mil		12/2/2019										Total Board Thickness: 44.2 mil			
Layer No.	Via Span & Hole Diameter	Description	Layer Name	Material Type	Differential Pairs >		Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)
					50/100 Digital	40/80 DDR3									
		Soldermask		PSR-4000 HFX Satin / CA-40 HF LPI ...	3.5	0.5									
1	8 8 4 4	Signal	Top	Conductive			3.97	2.9	2.2	12	4	0.43	51.67	98.65	Embedded Microstrip
		Prepreg		370HR : 1080 ; Rc= 66% (1GHz)											
2		Plane	GND	Conductive					1.4						
		Core		370HR: 1-7628; Rc=42% (1GHz)	4.4	7									Asymmetric Stripline
3		Signal	Inner 3	Conductive			4.19	8	1.4	10	4	0.31	53.26	99.85	
		Prepreg		370HR; 7628; Rc= 50% (1GHz)											
4		Plane	PWR	Conductive					1.4						
		Core		370HR : 1-1652 ; Rc=43% (1GHz)	4.4	5									
5		Signal	Inner 5	Conductive			4.14	4.8	1.4	16	4	0.31	51.23	99.63	Dual 48.89
		Prepreg		370HR : 2116 ; Rc= 56% (1GHz)											Symmetric Stripline 48.89
6		Signal	Inner 6	Conductive			4.4	5	1.4	16	4	0.31	51.23	99.63	
		Core		370HR : 1-1652 ; Rc=43% (1GHz)											
7		Plane	GND	Conductive					1.4						

Figure 1: Microstrip, asymmetric and dual symmetric stripline configuration. (Source: iCD Design Integrity)

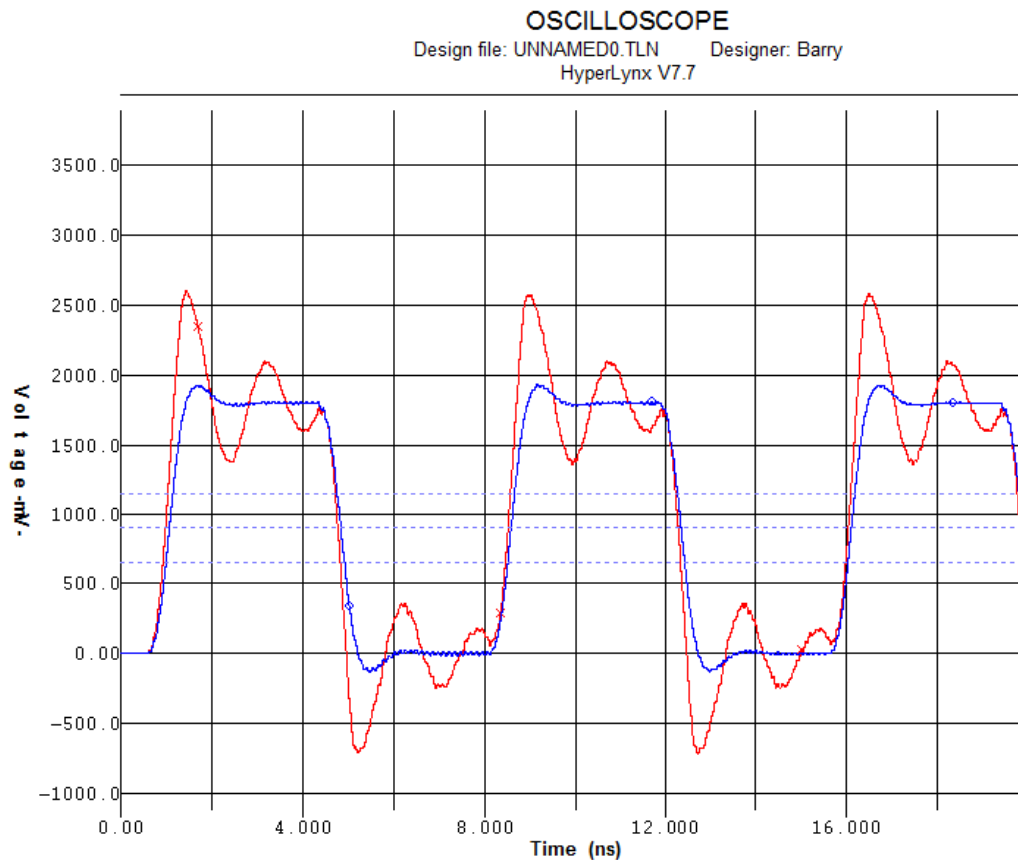


Figure 2: Unmatched (red) vs. matched (blue) transmission lines.

Unfortunately, drivers do not have the same impedance as the transmission line (typically 10–35  $\Omega$ ), so series terminations are used to balance the impedance, match the line, and minimize reflections, particularly on long traces where on-die termination is not provided. Impedance matching slows down the rise and fall times, reduces the ringing (over-/undershoot) of signal drivers, and enhances the quality of a high-speed signal. The ringing is dramatically reduced by adding a series terminator as in Figure 2. From this, we can see that the impedance has to be matched, but to what value?

In Figure 3, using a 12 mA LVCMOS 1.8V driver of a Spartan 6 FPGA, an 18.7  $\Omega$  series resistor is required to match the driver to the 51.67  $\Omega$  trace on the outer layer. This is automatically derived from the IV curves of the Spartan 6 IBIS model by the iCD Termination Planner.

When a signal's electromagnetic energy propagates from the driver to the receiver along a transmission line, it changes along its length. The original signal will be received with varying degrees of distortion and degradation. This signal

distortion happens due to factors such as impedance mismatch, reflections, ringing, crosstalk, dielectric loss, jitter, and ground bounce. The PCB designer's primary objective should be to minimize these issues at the source, so that any signal distortion is eliminated. But unfortunately, even with perfect impedance and termination, a signal can still be corrupted if its return current is forced to take a detour.

Another culprit is crosstalk, particularly on long parallel trace segments. Crosstalk arises as a result of the unintentional coupling of electromagnetic fields and causes both forward and reverse reflections. The easiest way to reduce crosstalk from a nearby aggressor signal is, of course, by increasing the spacing between the signals in question. Crosstalk falls off very rapidly with distance, plummeting roughly quadratically with increased separation. Doubling the spacing cuts the crosstalk to roughly a quarter of its original level. A good rule of thumb for this is  $\text{Gap} = 3x \text{ trace width}$ . However, in today's complex designs, it is not always possible to use up valuable real estate to satisfy the

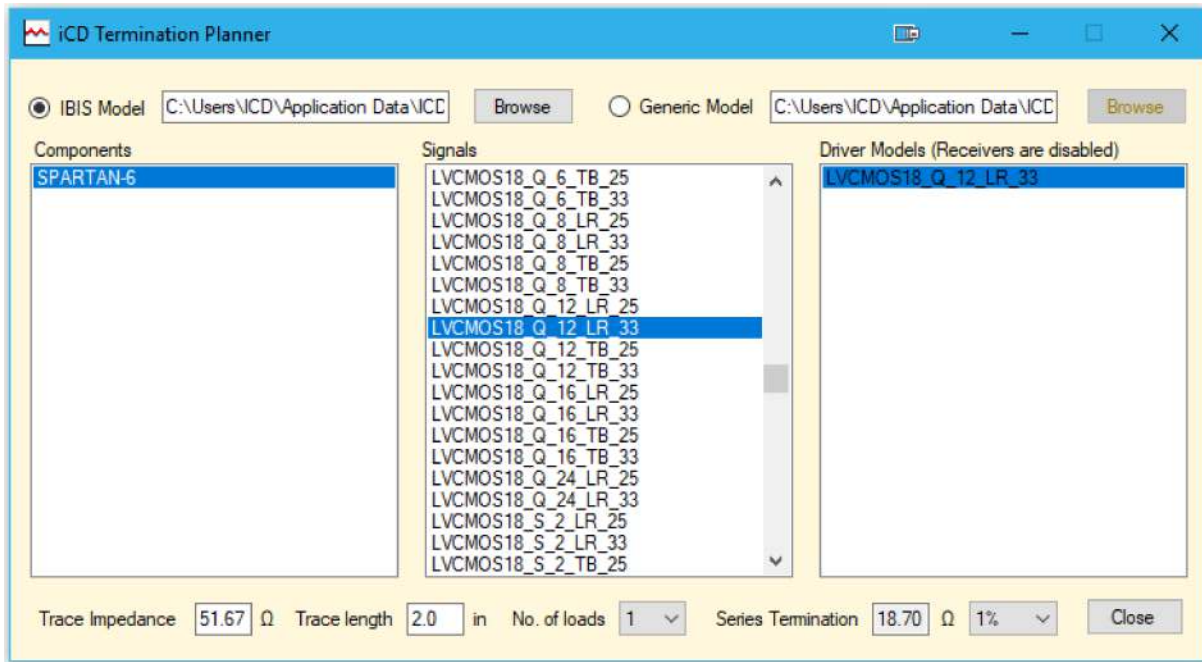


Figure 3: Matching the Spartan 6 driver to the transmission line. (Source: iCD Termination Planner)

above. Reducing the signal trace to reference plane dielectric thickness can also reduce crosstalk while not requiring additional space. Also, different technologies should not be mixed as higher voltages create higher crosstalk, and long parallel trace segments should be avoided.

Crosstalk also depends on the load, which may vary considerably when driving banks of memory modules, for example. Keep in mind that the total crosstalk on a victim trace is the sum of the crosstalk from each of several nearby aggressors.

Small discontinuities, such as vias and non-uniform return paths on a bus, are also becoming an important factor for the signal integrity and timing of high-speed systems. They produce impedance discontinuities due to the local return inductance and capacitive changes. Impedance discontinuities create reflected noise, contribute to differential channel-to-channel noise, and may promote mode conversion. In the case of differential pairs, the transformation from differential-mode to common-mode typically occurs on bends and non-symmetrical routing, near via and pin obstructions, but can also be caused by small changes in impedance due to return path issues.

One must also understand the importance of referencing and how to control the return displace-

ment current flow of a signal. Each signal layer should be adjacent to and closely coupled to a reference plane, creating a clear, uninterrupted return path and eliminating broadside crosstalk. As the layer count increases, this concept becomes easier to implement, but decisions regarding returning current paths become more challenging.

The return current of a high-speed, fast-rise time digital signal will always follow the path of least inductance, which is directly beneath the signal path, as in Figure 4. However, discontinuities tend to divert the return current, increasing the loop area, inductance, and delay. The best way to identify the discontinuities is to follow the signal path and imagine the return path closely coupled on the nearest plane. If multiple planes are present in the layer stack, the displacement current will still take the path of least inductance and closely follow the signal trace. If a discontinuity (e.g., split plane) interrupts this return flow, then the return current will be forced into a distant plane where it has a clear run, creating increased loop area and hence more inductance.

A via that connects signal traces referenced to different planes also creates discontinuities. In other words, the return current has to jump between the planes to close the current loop, which

in turn increases the inductance of the current loop, affecting the signal integrity. This return current also excites the parallel plate mode of the planes, causing significant EMI. If the reference planes are at the same DC potential, then they can be connected by stitching vias near the signal via transition to provide shorter paths for return currents. However, if the planes are at different DC potentials, then decoupling capacitors must be connected across the planes at these points to create a path. In addition, some of the return current flows through the interplane capacitance to close the loop.

Unfortunately, discontinuities can never be totally eliminated, but we can take steps to minimize their effects significantly. It is all about inductance! If the return path loop area is increased in any way, then the inductance will also increase. When return currents are disrupted, the energy they shed doesn't disappear; it often couples into the planes themselves.

Plane pairs in multilayer PCBs are essentially unterminated transmission lines, just not the usual traces or cables we may be accustomed to. They also provide a very low impedance path, which means they can present logic devices with a stable reference voltage at high frequencies. But as with signal traces, if the transmission line is mismatched or unterminated, there will be standing waves (ringing). The bigger the mismatch, the larger the standing waves, and the more the impedance will be location-dependent.

When the cavity has open-end boundary conditions, resonances arise when a multiple of half-wavelengths can fit between the ends of the cavity. When the clock or data harmonics overlap with the cavity resonant frequencies, there is the potential for long-range coupling between any signals that run through the cavity, thus affecting signal integrity as a consequence of inadequate power integrity.

High-speed signals behave like RF, turning the PCB into a distributed electromagnetic system. Rise time is the real driver of signal behavior, as every trace becomes a transmission line with its

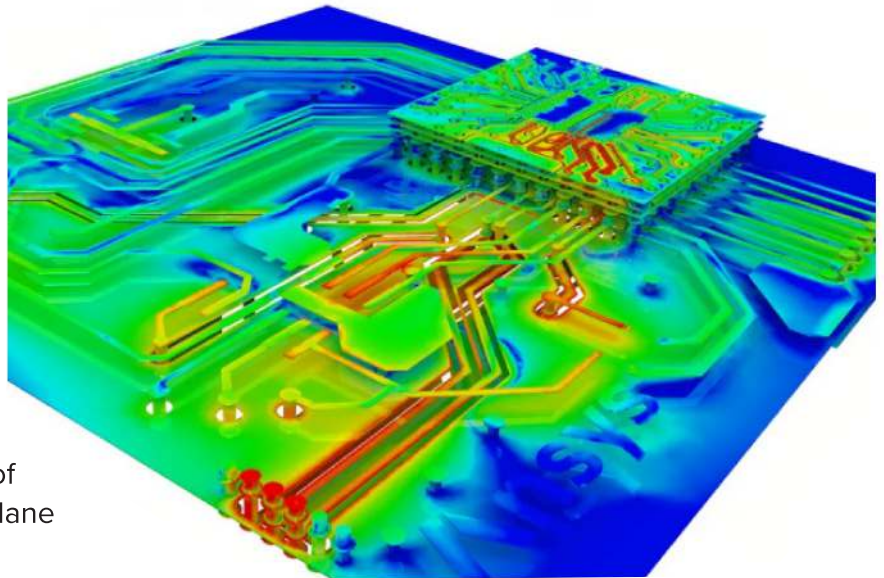


Figure 4: HFSS simulation of return paths. (Source: Ansys)

own characteristic impedance and propagation behavior. Variations in impedance, crosstalk, and disrupted return paths distort signals and can excite resonances in the power-ground cavity, making stable impedance, proper termination, and continuous return paths essential for reliable performance. With all these interactions, SI is not a set of isolated problems. It's a system of controlling electromagnetic energy. **I-CONNECT007**

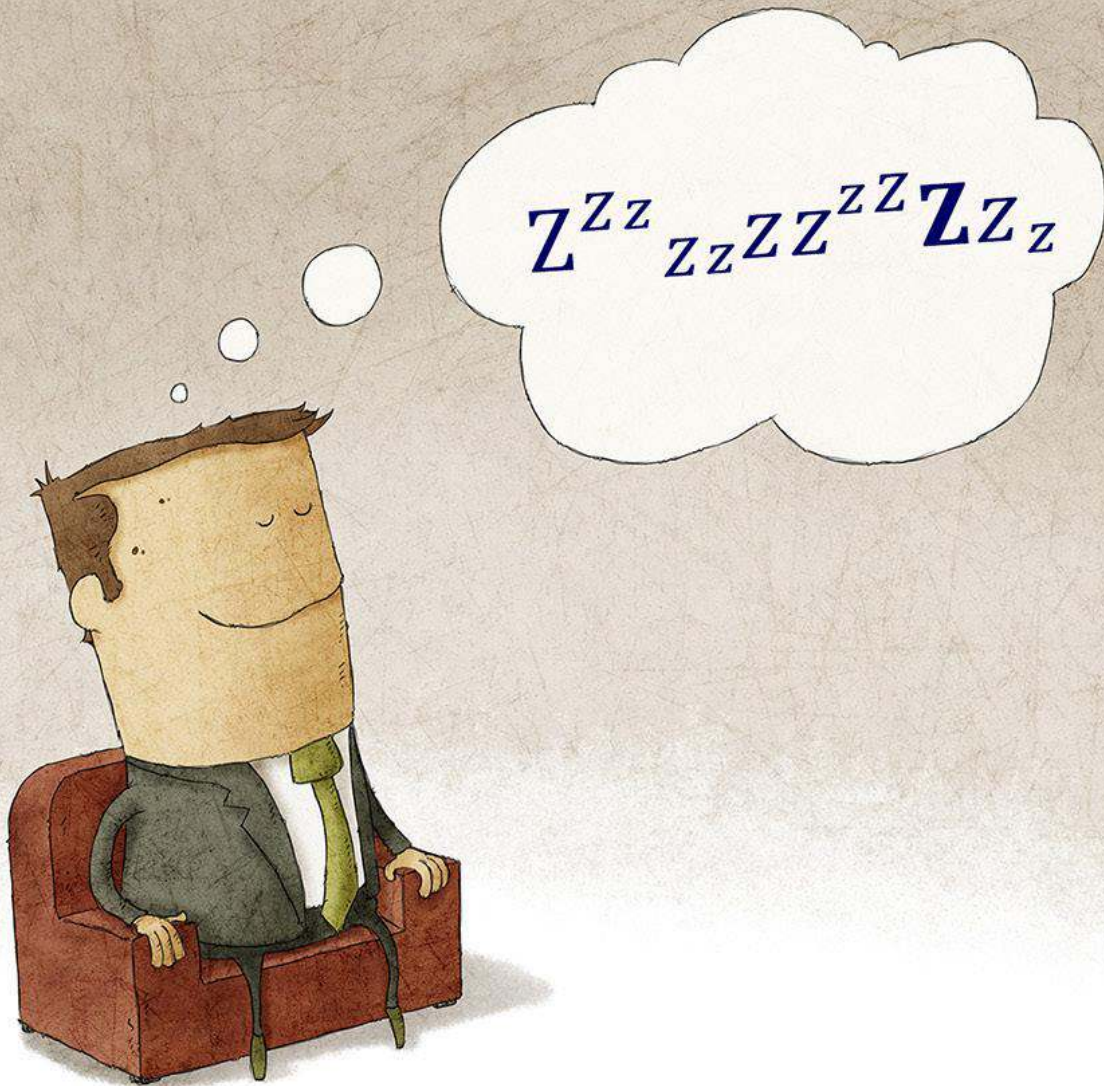
### Resources

- **Beyond Design** by Barry Olney: Interconnect Impedance, Controlled Impedance Design, The Fundamental Rules of High-Speed PCB Design Part 2, Reflecting on Reflections, Return Path Optimization.



**Barry Olney** is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded at [www.icd.com.au](http://www.icd.com.au). To read past columns, [click here](#).

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