10 Fundamental Rules of High-speed PCB Design, Part 3

Beyond Design

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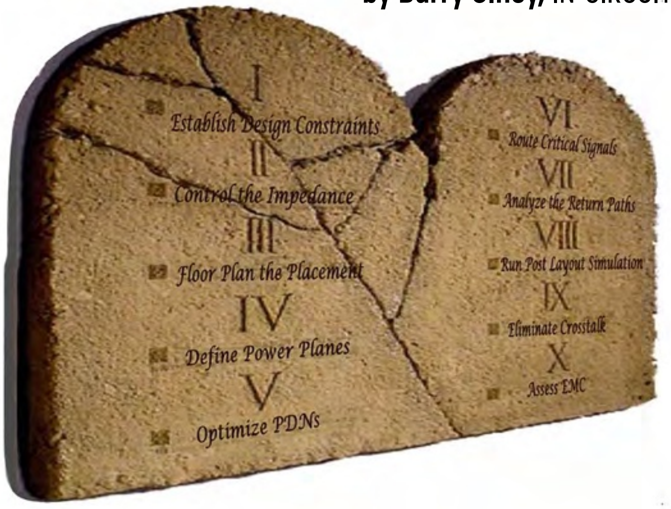


Figure 1: The 10 fundamental rules of high-speed PCB design.

Today's high-performance processors have fast rise times, low driver output impedance, and simultaneously switching of busses, which create high transient currents in the power and ground planes that degrade the performance and reliability of the product. Inadequate power delivery can exhibit intermittent signal integrity issues.

Continuing from my previous columns (Parts 1 and 2), I will elaborate on power distribution networks (PDNs) and define power planes and paths.

IV. Define the Power Delivery Planes and Paths:

Define the power/ground regions and plane layers. Partition (not split) the ground planes.

The power and ground planes in a high-speed, multilayer PCB perform six crucial functions:

1. Allow the routing of controlled impedance transmission lines in both microstrip and stripline configurations
2. Provide a reference voltage for the exchange of digital signals
3. Distribute stable power to all logic devices
4. Control crosstalk between switching signals
5. Provide planar capacitance to decouple high frequencies
6. Present a shield for electromagnetic radiation on internal layers

For these reasons, planes are essential in today's high-speed multilayer PCBs. Unfortunately, the number of power supplies required is increasing dramatically with IC complexity. Now, accounting for them all has become a real challenge. The high number of supplies generally leads to higher layer count substrates. In the past, we used to have more signal routing layers than planes; the opposite is now the case when the majority of stackup layers are reserved for power distribution. Although this increases the cost, it may be a godsend because it provides segregation of critical signals to avoid crosstalk and reduces radiation due to close coupling of signal traces to the reference planes.

In a recent complex design that I completed, I counted over 10 individual power supplies

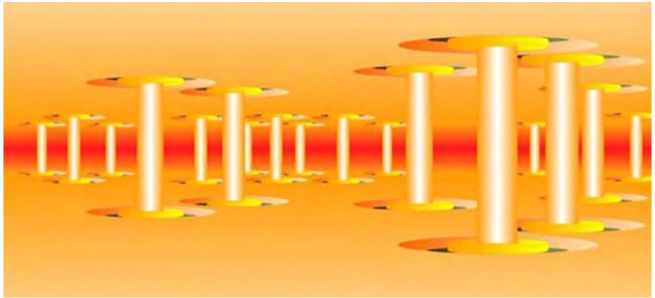


Figure 2: Enlarged 3D cross-sectional view of a plane cavity with a transparent core.

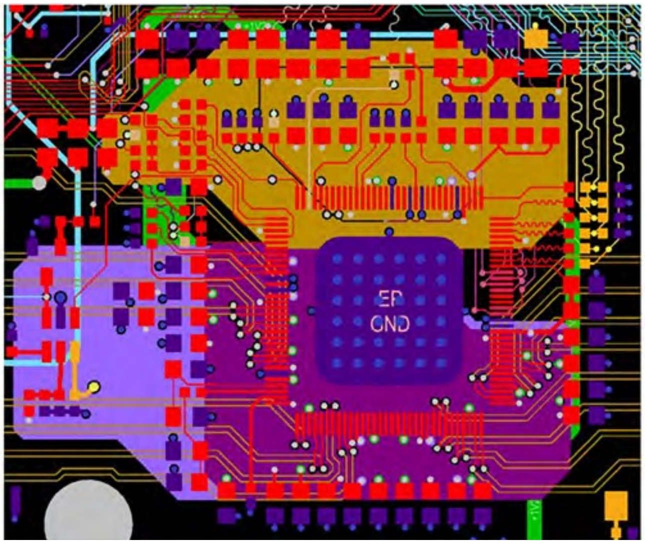


Figure 3: Supplies poured under an IC on multiple layers separated by ground planes.

ranging from the 5V input power to the board to 0.75V DDR3 VTT reference voltage. These supplies required six layers (including ground) of the 10-layer stackup, which left only four layers for signal routing.

The methodology I follow to define the planes is as follows. First, it is beneficial to define the power supply regions in conjunction with placement. Group all components by functionality and their common power supply. Second, work on the critical circuits first and ensure there is a contiguous ground plane on one side and the corresponding power plane on the other. This creates a minimum loop area and a low-inductance return current path. Third, segregate critical circuits with ground planes. For example, the top portion of a symmetrical stackup can be used for one circuit and the bottom for another.

Fourth, arrange the power regions so that they do not overlap on adjacent layers because coupling between different supplies can transfer plane noise. A ground plane in between power planes prevents this and also adds valuable planar capacitance. Next, keep the regions as square as possible because a long, rectangular shape plane can create rogue waves in the plane cavities. Lastly, ensure that no signal crosses a split in the ground plane into a different domain.

Power planes can be split into many different power areas (Figure 3). And since digital circuits are normally referenced to the same ground, there is no real need to split a ground plane. As mentioned in Part 2, route fences (keep-outs) can be used to control the routing and prevent signals from crossing over into different logic domains. Split ground planes create discontinuities of impedance, crosstalk, and EMI, and should not be used. Controlled routing is the key to a successful mixed-signal design. The ground planes should not be split; instead, they should be partitioned, and a pass-through gap should be left in the route keep-out so that control signals can enter and leave the sensitive areas.

V. Optimize the Power Distribution Networks (PDNs): Create a low AC impedance delivery path by optimizing the bypass and decoupling capacitors, and mount inductance and plane resonance from DC to the maximum required frequency (including harmonics).

The PDN must accommodate variances of switching current with as little change in power supply voltage as possible (a 5% voltage ripple is a typical requirement). The goal of PDN planning is to design a stable power source for all the required power supplies. Ideally, the effective impedance of the PDN should be kept as low as possible up to the maximum operating frequency.

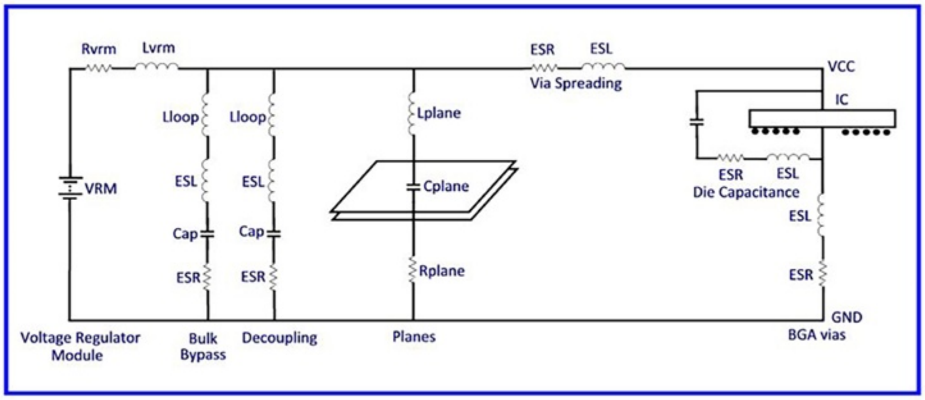


Figure 4: Typical PDN topology.

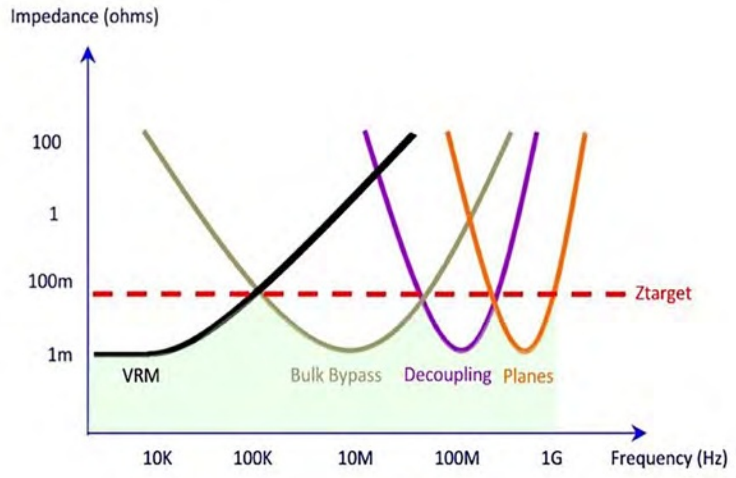


Figure 5: Target impedance, VRM, capacitor, and plane profiles of a PDN.

Figure 4 shows the topology of a typical PDN, which includes the voltage regulator module (VRM), bulk bypass and decoupling capacitors, plane, die capacitance, BGA via, and via spreading inductance. Each of these components has a specific resonant frequency where the impedance will be low. However, these components interact to create anti-resonance peaks that may occur at undesirable frequencies and wreak havoc on an otherwise stable supply.

The target impedance (Ztarget) of the PDN is the combination of the worst-case transient current and the voltage noise specification, which act together to set the maximum allowable PDN impedance with an assured performance. Target impedance is the most crucial metric when evaluating PDN performance. The further the PDN impedance is above the target impedance, the greater the risk of intermittent operation or even complete product failure.

Taking the VRM and planes into consideration, selected values of bypass and decoupling capacitors are added to the PDN to lower the impedance at a particular frequency (Figure 5). Capacitors reach their minimum impedance at their resonant frequency, which is determined by the capacitance, equivalent series resistance (ESR), and the equivalent series inductance (ESL) together with the mounting inductance. To meet the target impedance at a particular frequency, a capacitance value is chosen so that when mounted on the PCB, it will resonate at the desired frequency and have an impedance that is equal to its ESR. Then, a sufficient number of those capacitors are placed in parallel so that the combined parallel ESRs approach the desired target impedance.

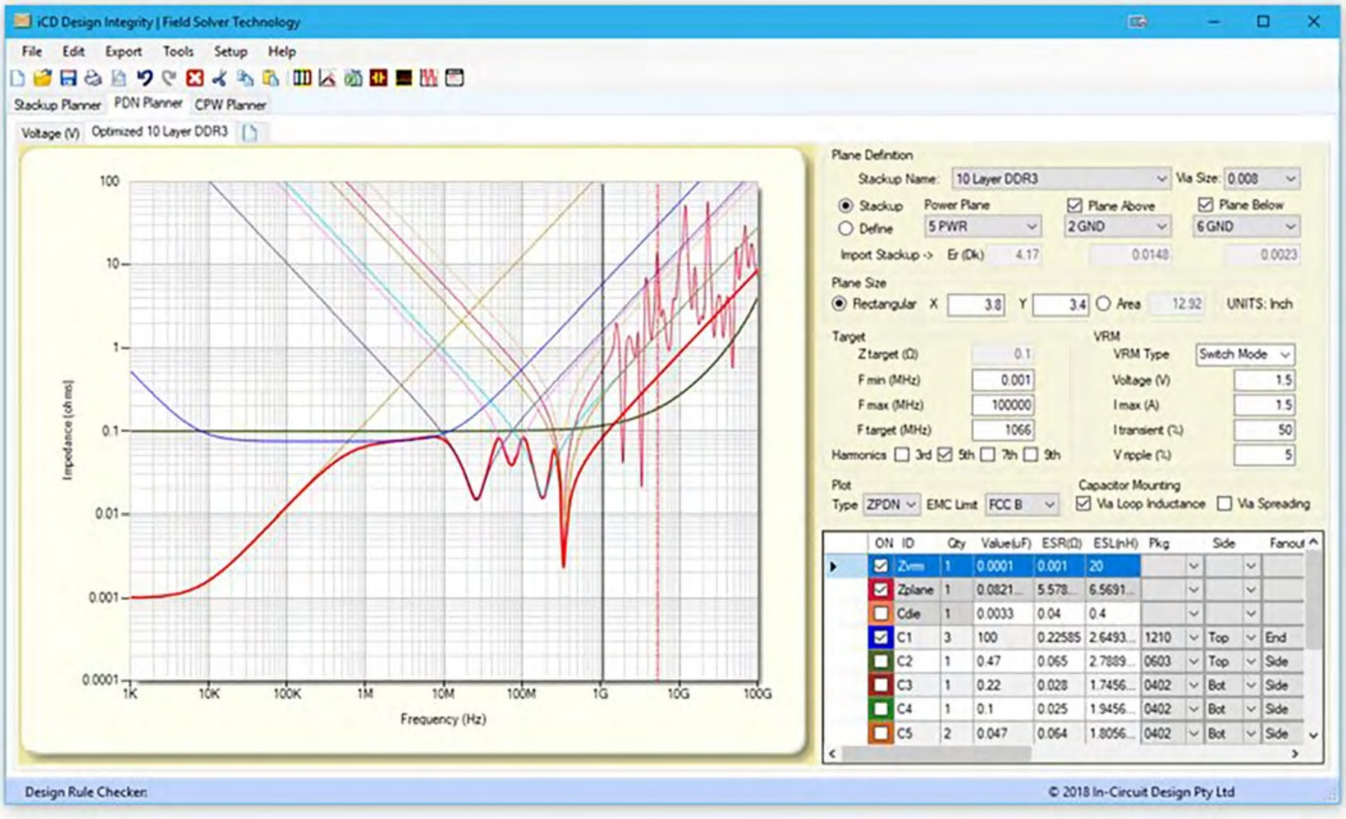
As one can see from Figure 6, each value capacitor has a different resonant frequency depression. Thus, one would assume that by placing many different values of capacitors on the board, the entire frequency range would be covered or have minimal impedance from DC to maximum frequency. Unfortunately, it is not as simple as that.

Decoupling capacitors are only effective up to about 200 MHz; above that, only on-die capacitance or planar capacitance can reduce the PDN impedance significantly. In Figure 6, I used a thin core dielectric of 2.3 mils between the planes to lower the effective impedance at high frequency. This is relatively easy to accomplish with multiple plane layers in the stackup—another bonus! This strategy provides low impedance up to 1.58 GHz, in this case.

Providing a balance of capacitors selected at the right frequencies and combined with planar capacitance can lower the anti-resonance peaks to the target impedance up to the maximum operating frequency.

Key Points:

- The power and ground planes in a high-speed, multilayer PCB perform six crucial functions
- The high number of power supplies generally leads to higher layer count substrates
- These days, the majority of stackup layers of a complex design are reserved for power distribution
- Power planes can be split into many different power areas, but digital circuits are normally referenced to the same ground, so there is no real need to split a ground plane



Plane Definition

Stackup Name: 10 Layer DDR3 Via Size: 0.008

● Stackup ○ Define Power Plane: 5 PWR ☑ Plane Above: 2 GND ☑ Plane Below: 6 GND

Import Stackup -> Er (Dk) 4.17 0.0148 0.0023

Plane Size

● Rectangular X 3.8 Y 3.4 ○ Area 12.92 UNITS: Inch

Target

Z target (Ω) 0.1

F min (MHz) 0.001

F max (MHz) 100000

F target (MHz) 1066

Harmonics ☐ 3rd ☑ 5th ☐ 7th ☐ 9th

VRM

VRM Type Switch Mode

Voltage (V) 1.5

I max (A) 1.5

I transient (%) 50

V ripple (%) 5

Plot

Type ZPDN EMC Limit FCC B

Capacitor Mounting

☑ Via Loop Inductance ☐ Via Spreading

ON	ID	Qty	Value(uF)	ESR(Ω)	ESL(nH)	Pkg	Side	Fanout
☑	Zvrm	1	0.0001	0.001	20			
☑	Zplane	1	0.0821...	5.578...	6.5691...			
☐	Cdie	1	0.0033	0.04	0.4			
☑	C1	3	100	0.22585	2.6493...	1210	Top	End
☐	C2	1	0.47	0.065	2.7889...	0603	Top	Side
☐	C3	1	0.22	0.028	1.7456...	0402	Bot	Side
☐	C4	1	0.1	0.025	1.9456...	0402	Bot	Side
☐	C5	2	0.047	0.064	1.8056...	0402	Bot	Side

Figure 6: Optimized PDN for a 1066 MHz DDR3 (iCD PDN Planner).

- Split ground planes create discontinuities of impedance, crosstalk, and EMI, and should not be used
- The ground planes should not be split, but partitioned instead
- The goal of PDN planning is to design a stable power source for all the required power supplies
- Each component of the PDN has a specific resonant frequency where the impedance will be low
- PDN components interact to create anti-resonance peaks that may occur at undesirable frequencies
- The further the PDN impedance is above the target impedance, the greater the risk of intermittent operation or even complete product failure
- Decoupling capacitors are only effective up to about 200 MHz; above that, only on-die capacitance or planar capacitance can reduce the PDN impedance significantly

Further Reading

- Beyond Design: Power Distribution Network Planning by Barry Olney, *The PCB Magazine*, May 2012.
- Beyond Design: Plane Crazy, Part 1 by Barry Olney, *The PCB Design Magazine*, December 2015.
- Beyond Design: The Target Impedance Approach to PDN Design by Barry Olney, *Design007 Magazine*, February 2018.
- *High-Speed Digital Design: A Handbook of Black Magic, First Edition* by Howard Johnson and Martin Graham, Prentice Hall, 1993.

Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded from www.icd.com.au. To read past columns or contact Olney, click here.